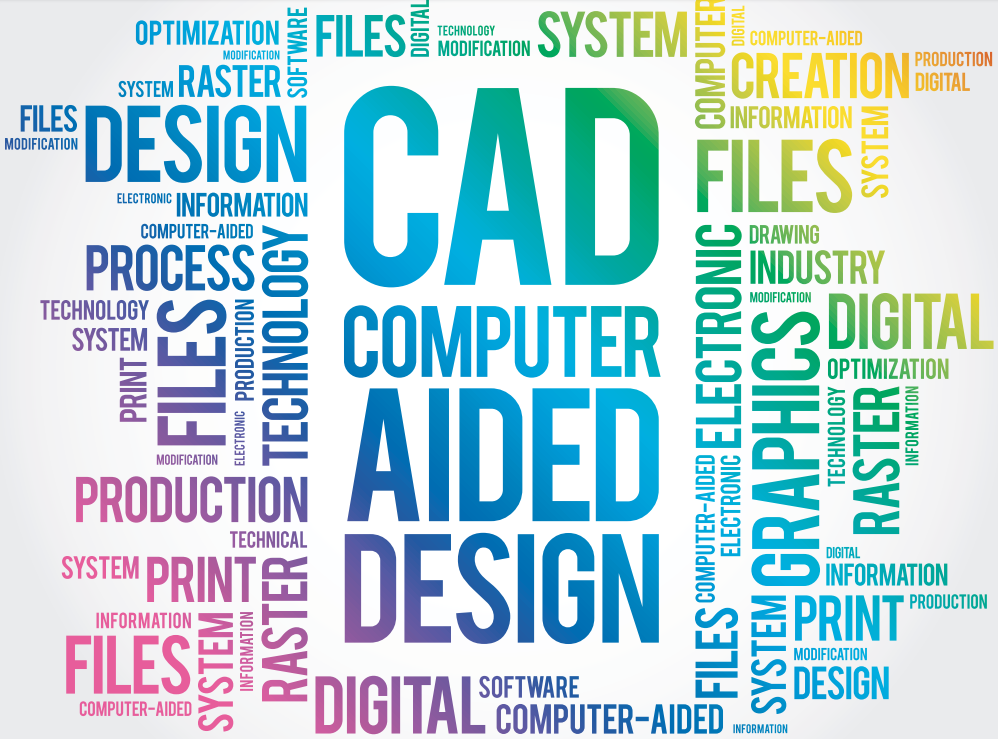
IEEE/ACM

ICCAD

2020 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

39th Edition

ICCAD 2020 VIRTUAL EVENT



NOVEMBER 2 – 5, 2020

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WELCOME TO THE 39TH ICCAD

FROM YUAN XIE

ICCAD GENERAL CHAIR

Welcome to the 39th edition of the International Conference on Computer-Aided Design! This year, due to the global COVID-19 pandemic, many conferences are forced to make the event work in the online world. Consequently, the ICCAD 2020 Executive Committee decided to move forward with a Virtual Conference due to the continued uncertainty surrounding the COVID-19 situation. Nevertheless, we are very excited to test out this new online edition for the first time in ICCAD's 39-year history. Even though the virtual events lack the kind of interpersonal communications attendees get from in-person events, a much lower registration fee with no travel overheads may boost the number of participants. A carefully tuned schedule with a virtual platform can make it a true "global" event for anyone around the world to attend ICCAD. We hope you will enjoy this unique virtual experience with the first-ever online ICCAD.

Jointly sponsored by IEEE and ACM, ICCAD is the premier forum to explore emerging technology challenges in electronic design automation, present leading-edge R&D solutions, and identify future roadmaps for design automation research areas. The members of the executive committee, the technical program committee, and numerous volunteers have spent the past several months preparing an exciting program for you!

This was another strong year for ICCAD in terms of the number of regular paper submissions. We received more than 470 regular paper submissions. They were divided into 17 tracks and reviewed by 144 outstanding technical program committee members from both industry and academia worldwide. For the first time, the TPC meeting was held online without compromising the quality of the double-blind review process. Finally, the program committee has selected 127 papers spread over 35 sessions on diverse topics. We also had a record number of special session proposals submitted to ICCAD this year. Altogether, we have 11 special sessions and two embedded tutorials on topics that complement the regular sessions.

We are delighted to host several distinguished keynote speakers: the Monday morning keynote on AI for enterprises will be given by IBM Fellow Dr. Ruchir Puri. On Tuesday, Professor Birgit Vogel-Heuser from the Technical University of Munich will present the IEEE CEDA Luncheon Distinguished Lecture on Cyber Physical Systems. Finally, Professor Yao-Wen Chang from National Taiwan University will present the Wednesday keynote on EDA for More-Moore and More-than-Moore Designs. We hope you will find these keynotes exciting and informative.

On Thursday, we have five interesting workshops planned, on a variety of both new and established topics. Some of these workshops are long-time staples of ICCAD, while others test the waters for the first time. Additionally, a workshop addressing System-level interconnect problems is co-located with ICCAD. All these workshops have exciting programs themselves, so we hope that many of you will take advantage of them.

Once again, ICCAD promises to be an ultimate destination for those working on cutting edge EDA research. We hope that you will be able to join us in making this first-ever virtual event a great and memorable one. Finally, we are grateful to our ICCAD 2020 sponsors and numerous supporters for making this year's conference another successful event.

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BEST PAPER CANDIDATES

IEEE/ACM William J. McCalla ICCAD Best Paper Award Candidates

MONDAY, NOVEMBER 2

***1B.1 Electromigration Checking Using a Stochastic Effective Current Model**

Adam Issa - *Univ. of Toronto*
Valeriy Sukharev - *Mentor, A Siemens Business*
Farid N. Najm - *Univ. of Toronto*

***2C.1 Energy-Efficient Control Adaptation with Safety Guarantees for Learning-Enabled Cyber-Physical Systems**

Yixuan Wang - *Northwestern Univ.*
Chao Huang - *Northwestern Univ.*
Qi Zhu - *Northwestern Univ.*

TUESDAY, NOVEMBER 3

***8C.1 HyperFuzzing for SoC Security Validation**

Sujit Kumar Muduli - *Indian Institute of Technology Kanpur*
Gourav Takhar - *Indian Institute of Technology Kanpur*
Pramod Subramanyan - *Indian Institute of Technology Kanpur*

WEDNESDAY, NOVEMBER 4

***9C.1 Optimally Approximated and Unbiased Floating-Point Multiplier with Runtime Configurability**

Chuangtao Chen - *Zhejiang Univ.*
Sen Yang - *Zhejiang Univ.*
Weikang Qian - *Shanghai Jiao Tong Univ.*
Mohsen Imani - *Univ. of California, Irvine*
Xunzhao Yin - *Zhejiang Univ.*
Cheng Zhuo - *Zhejiang Univ.*

***10C.3 DISQ: A Novel Quantum Output State Classification Method on IBM Quantum Computers using OpenPulse**

Tirthak Patel - *Northeastern Univ.*
Devesh Tiwari - *Northeastern Univ.*

***12B.1 GridNet: Fast Data-Driven EM-Induced IR Drop Prediction and Localized Fixing for On-Chip Power Grid Networks**

Han Zhou - *Univ. of California, Riverside*
Wentian Jin - *Univ. of California, Riverside*
Sheldon Tan - *Univ. of California, Riverside*

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BEST PAPER AWARD COMMITTEES

IEEE/ACM William J. McCalla ICCAD Best Paper Award Selection Committee

Paolo Ienne (Chair) - *École Polytechnique Fédérale de Lausanne*
Chuck Alpert - *Cadence Design Systems*
Ingrid Verbauwhede - *KU Leuven*
Niraj Jha - *Princeton Univ.*
Petru Eles - *Linköping Univ.*
Puneet Gupta - *Univ. of California, Los Angeles*

Ten-Year Retrospective Most Influential Paper Award Selection Committee

Martin Wong (Chair) - *Univ. of Illinois at Urbana-Champaign and Chinese Univ. of Hong Kong*
Deming Chen - *Univ. of Illinois at Urbana-Champaign*
Evangeline Young - *Chinese Univ. of Hong Kong*
Zhuo Feng - *Stevens Institute of Technology*

EMBEDDED TUTORIAL/SPECIAL SESSION COMMITTEE

Evangeline Young (Chair) - *The Chinese Univ. of Hong Kong*
Laleh Behjat - *Univ. of Calgary*
Tony Givargis - *Univ. of California, Irvine*
Iris Hui-Ru Jiang - *National Taiwan Univ.*
Hai (Helen) Li - *Duke Univ.*
Sachin Sapatnekar - *Univ. of Minnesota*
Sheldon Tan - *Univ. of California, Riverside*
Yu Wang - *Tsinghua Univ.*

MONDAY SCHEDULE

6:30 - 7:00am

Opening Session & Awards

7:00 - 8:00am

KEYNOTE: Engineering the Future of AI for the Enterprises

Ruchir Puri - IBM Research.

8:00 - 8:30am

1A: Routing Strategies for 2D/2.5/3D ICs

1B: Electromigration and Circuit Yield: Efficient Verification Techniques

1C: Securing Embedded and IoT Platforms

Special Session 1D: How Machine Leaning can Reshape Technology, Manufacturability, Performance and Power

8:30 - 9:00am

2A: Machining Learning Techniques for Routing and Hotspot Detection

2B: Exploring Optimal Mask Patterns

2C: Safety and Energy Optimizations for Cyber-Physical Systems

Special Session 2D: AIoT: The Powerful Convergence of AI and the IoT – An Industrial Perspective

9:00 - 9:30am

3A: Brain-inspired, Bio-engineering, and Emerging Computing

3B: Novel Techniques for Improving Reliability and Manufacturability

3C: Secure Architectures and Systems Design

Special Session 3D: Hardware/Software Co-Design for Machine Learning in Medicine

9:30 - 10:00am

Delivering Improved Design Performance by Applying Machine Learning to EDA

9:30 - 11:30am

ACM Student Research Competition at ICCAD 2020

Note Agenda time zone is PST (UTC-8)

Opening Session and Awards

Time: 6:30 -7:00am

Start off the conference with opening remarks from the ICCAD Executive Committee members and hear the highlights of the conference. The IEEE/ACM William J. McCalla ICCAD Best Paper award will be announced along with other award presentations from IEEE CEDA and ACM. .

IEEE/ACM WILLIAM J. MCCALLA ICCAD BEST PAPER AWARD

This award is given in memory of William J. McCalla for his contributions to ICCAD and his CAD technical work throughout his career.

Front-End Award:

8C.1: HyperFuzzing for SoC Security Validation

Sujit Kumar Muduli, Gourav Takhar and Pramod Subramanayan - *Indian Institute of Technology Kanpur*

Back-End Award:

1B.1: Electromigration Checking Using a Stochastic Effective Current Model

Adam Issa - *Univ. of Toronto*
Valeriy Sukharev - *Mentor, A Siemens Business*
Farid N. Najm - *Univ. of Toronto*

TEN YEAR RETROSPECTIVE MOST INFLUENTIAL PAPER AWARD

This award is being given to the paper judged to be the most influential on research and industrial practice in computer-aided design over the ten years since its original appearance at ICCAD.

2010 Paper Titled: 3D-ICE: Fast Compact Transient Thermal Modeling for 3D Ics with Inter-Tier Liquid Cooling

A. Sridhar, A. Vincenzi, M. Ruggiero, T. Brunschwiler and D. Atienza, ICCAD 2010 pp. 463-470, doi:10.1109/ICCAD.2010.5653749.

IEEE FELLOWS

Partha Pratim Pande - *Washington State Univ.*
For contributions to network-on-chip architectures for manycore computing.

Maciej Ciesielski - *Univ. of Massachusetts*
For contributions to logic synthesis and formal verification of arithmetic circuits.

IEEE CEDA OUTSTANDING SERVICE RECOGNITION

David Pan - *The Univ. of Texas at Austin*
For outstanding service to the EDA community as ICCAD General Chair in 2019.

IEEE CEDA ERNEST S. KUH EARLY CAREER AWARD

Prof. Yier Jin - Univ. of Florida
For contributions to hardware security.

Opening Session and Awards

Time: 6:30am - 7:00am

Keynote: Engineering the Future of AI for the Enterprises

Time: 7:00am - 8:00am

Speaker:

Ruchir Puri - *IBM Research*

Recent advances in AI are starting to transform every aspect of our society from healthcare, manufacturing, environment, and beyond. The future of AI for enterprises will be engineered with success along three foundational dimensions. We will dive deeper along these dimensions - Automation of AI; Trust of AI; and Scaling of AI - and conclude with the opportunities and challenges of AI for businesses.

Biography: Dr. Ruchir Puri is the Chief Scientist of IBM Research and an IBM Fellow. He led IBM Watson as its CTO and Chief Architect from 2016-19 and has held various technical, research, and engineering leadership roles across IBM's AI and Research businesses. Dr. Puri is a Fellow of the IEEE, and has been an ACM Distinguished Speaker, an IEEE Distinguished Lecturer, and was awarded 2014 Asian American Engineer of the Year. Dr. Puri has been an adjunct professor at Columbia Univ., NY, and a visiting scientist at Stanford Univ., CA. He was honored with John Von-Neumann Chair at The Institute of Discrete Mathematics at Bonn Univ., Germany. Dr. Puri is an inventor of over 60 United States patents and has authored over 100 scientific publications on software-hardware automation methods, microprocessor design, and optimization algorithms. He is the chair of 2020 AAAI-IAAI conference that focused on industrial applications of AI. Ruchir's technical opinions on the adoption of AI by society and businesses have been featured across New York Times, Wall Street Journal, Forbes, Fortune, IEEE spectrum among other.

1A - Routing Strategies for 2D/2.5/3D ICs

Time: 8:00am - 8:30am

Moderator:

Jianli Chen - *Fuzhou Univ.*

This session covers various novel techniques in routing. The first paper conducts wire segment routing for 2D global routing. The second one optimizes pin-access in 3D designs. The third paper improves the coupling extraction for heterogeneous 2.5D chiplet-package co-designs. The last one presents an optimization flow for heterogeneous monolithic 3D designs.

1A.1 COALA: Concurrently Assigning Wire Segments to Layers for 2D Global Routing
Yun-Jhe Jiang, Shao-Yun Fang - *National Taiwan Univ. of Science and Technology*

1A.2 Routability-Driven Pin-Access Optimization for Monolithic 3D IC Designs
Run-Yi Wang, **Yao-Wen Chang** - *National Taiwan Univ.*

1A.3 Coupling Extraction and Optimization for Heterogeneous 2.5D Chiplet-Package Co-Design
MD Arafat Kabir - *Univ. of Arkansas*
Dusan Petranovic - *Mentor, A Siemens Business*
Yarui Peng - *Univ. of Arkansas*

1A.4 Pin-3D: A Physical Synthesis and Post-Layout Optimization Flow for Heterogeneous Monolithic 3D ICs
Sai Surya Kiran Pentapati, Kyungwook Chang - *Georgia Institute of Technology*
Vassilios Gerousis, Rwik Sengupta - *Samsung Semiconductor, Inc.*
Sung Kyu Lim - *Georgia Institute of Technology*

1B - Electromigration and Circuit Yield: Efficient Verification Techniques

Time: 8:00am - 8:30am

Moderator:

Ing-Chao Lin - *National Cheng Kung Univ.*

Continuing scaling of integrated circuits has made the active devices as well as interconnections even smaller, which greatly improved circuit performance, while device parameter variation and current density of wires increased significantly. The yield of the manufactured circuit and its long-term reliability have become a major concern in designing circuits. In this session, we discuss efficient electromigration immortality check methods considering current density fluctuation and Joule heating, and a fast Monte Carlo method that uses non-Gaussian adaptive importance sampling technique for accelerating the yield analyses.

***1B.1 Electromigration Checking Using a Stochastic Effective Current Model**
Adam Issa - *Univ. of Toronto*
Valeriy Sukharev - *Mentor, A Siemens Business*
Farid N. Najm - *Univ. of Toronto*

1B.2 Electromigration Immortality Check considering Joule Heating Effect for Multisegment Wires
Mohammadamir Kavousi, Liang Chen, Sheldon X. Tan - *Univ. of California, Riverside*

1B.3 A Non-Gaussian Adaptive Importance Sampling Method for High-Dimensional and Multi-Failure-Region Yield Analysis
Xiao Shi - *Univ. of California, Los Angeles*
Hao Yan, Chuwen Li - *Southeast Univ.*
Jianli Chen - *Fudan Univ.*
Longxing Shi - *Southeast Univ.*
Lei He - *Univ. of California, Los Angeles & Fudan Univ.*

1C - Securing Embedded and IoT Platforms

Time: 8:00am - 8:30am

Moderator:

Partha Pande - *Washington State Univ.*

This session focuses on new approaches to secure embedded and IoT platforms. The first paper explores a crowd-based explosion detection system. The second paper proposes an adaptive anomaly detection in distributed IoT platforms. The third paper explores a Bloom filter-based mechanism for low overhead address space protection in IoT blockchain systems. The last paper proposes a mechanism for protecting embedded neural networks from Trojan attacks.

1C.1 A Crowd-Based Explosive Detection System with Two-Level Feedback Sensor Calibration
Chengmo Yang, Patrick T. Cronin - *Univ. of Delaware*
Agamyrat Agambayev, Sule Ozev - *Arizona State Univ.*
Ahmet E. Cetin - *Univ. of Illinois at Chicago*
Alex Orailoglu - *Univ. of California, San Diego*

1C.2 IoT-CAD: Context-Aware Adaptive Anomaly Detection in IoT Systems Through Sensor Association
Rozhin Yasaei, Felix Hernandez, Mohammad Abdullah Al Faruque - *Univ. of California, Irvine*

1C.3 ABACUS: Address-partitioned Bloom filter on Address Checking for UniquenesS in IoT Blockchain
Tianyu Wang - *Chinese Univ. of Hong Kong*
Wenbin Zhu, Qun Ma, Zhaoyan Shen - *Shandong Univ.*
Zili Shao - *Chinese Univ. of Hong Kong*

1C.4 CLEANN: Accelerated Trojan Shield for Embedded Neural Networks
Mojan Javaheripi, Mohammad Samragh, Gregory Fields, Tara Javidi, Farinaz Koushanfar - *Univ. of California, San Diego*

Special Session 1D - How Machine Leaning can Reshape Technology, Manufacturability, Performance and Power

Time: 8:00am - 8:30am

Moderators:

Ertugrul Demircan - *NXP Semiconductors*
Mark Johnstone - *NXP Semiconductor*

Organizers:

Sheldon Tan - *Univ. of California*
Hussam Amrouch - *Karlsruhe Institute of Technology*

Recently machine learning, especially deep learning is gaining much attention due to the breakthrough performance in various cognitive applications. Machine learning for electronic design automation (EDA) is also gaining significant traction as it provides new computing and optimization paradigms for many challenging design automation problems with complex nature. Today's chip designer and EDA developers faces several many challenges in advanced technologies from technology and physical levels to the circuit and multi-core chip levels such as designing robust circuits with high manufacturability and yield, excessive voltage IR drops, thermally constrained multi-core processor design and runtime thermal/power/reliability management and excessive on-chip power density and efficiency limitations due to fundamental restrictions in voltage scaling etc. Given the complex nature of those EDA problems, this special session focuses on complicated lithography modeling, efficient IR drop estimation, fast full-chip thermal/power modeling, design-technology co-optimization in advanced technologies and demonstrates the potentials in using latest advances in machine learning to tackle those hard problems towards developing intelligent EDA algorithms. This special session consists of four presentations ranging from machine Learning for VLSI manufacturability and yield, fast machine learning based IR drop estimation, data-driven full-chip thermal/power modeling, machine learning for modeling emerging technologies.

1D.1 Re-examining VLSI Manufacturing and Yield through the Lens of Deep Learning
Mohamed Mohamed Baker Alawieh, Wei Ye - *Univ. of Taxes at Austin*
David Z. Pan - *Univ. of Texas at Austin*

1D.2 Fast IR Drop Estimation with Machine Learning
Zhiyao Xie, **Hai Li** - *Duke Univ.*
Xiaoqing Xu - *Arm, Ltd.*
Jiang Hu - *Texas A&M Univ.*
Yiran Chen - *Duke Univ.*

1D.3 Full-Chip Thermal Map Estimation for Commercial Multi-Core CPUs with Generative Adversarial Learning
Wentian Jin - *Univ. of California, Riverside*
Sheriff Sadiqbatcha - *Univ. of California, Riverside*
Jinwei Zhang, **Sheldon Tan** - *Univ. of California, Riverside*

1D.4 Modeling Emerging Technologies using Machine Learning: Challenges and Opportunities
Florian Klemme, Jannik Prinz, Victor van Santen, Joerg Henkel - *Karlsruhe Institute of Technology*
Hussam Amrouch - *Univ. of Stuttgart*

2A - Machining Learning Techniques for Routing and Hotspot Detection

Time: 8:30am - 9:00am

Moderator:

David Chinnery - *Mentor, A Siemens Business*

This session builds different machining learning frameworks to improve the routability. The first paper presents a hot-spot detection flow through deep layout metric learning. The second one is a plug-in framework to improve the routing. The last one is a detailed router for analog-mixed-signal designs.

2A.1 Hotspot Detection via Attention-based Deep Layout Metric Learning
Hao Geng, Haoyu Yang, Lu Zhang - *Chinese Univ. of Hong Kong*
Jin Miao - *Synopsys, Inc.*
Fan Yang, Xuan Zeng - *Fudan Univ.*
Bei Yu - *Chinese Univ. of Hong Kong*

2A.2 PROS: A Plug-in for Routability Optimization applied in the State-of-the-art commercial EDA tool using deep learning
Jingsong Chen - *Chinese Univ. of Hong Kong*
Jian Kuang, Guowei Zhao, Dennis J.-H. Huang - *Cadence Design Systems, Inc.*
Evangeline F.Y. Young - *Chinese Univ. of Hong Kong*

2A.3 Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits
Hao Chen, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, David Z. Pan - *Univ. of Texas at Austin*

All speakers are denoted in bold | * denotes Best Paper Candidate | Note Agenda time zone is PST (UTC-8)

2B - Exploring Optimal Mask Patterns

Time: 8:30am - 9:00am

Moderator:

Takashi Sato - *Kyoto Univ.*

Optical proximity correction (OPC) is a process that is widely applied in advanced nodes for manufacturability optimization. It is also the most expensive and difficult process in terms of computational efforts. The first paper in this session tackles this issue with a full chip scale, high-performance and salable OPC system based on deep learning. The second paper proposes an OPC framework that uses a neural network to perform end-to-end pattern prediction and inverse lithography-technology (ILT) based OPC framework. The third paper suggests improved printability through Lammellar directed self-assembly (DSA) with guiding template design.

2B.1 DAMO: Deep Agile Mask Optimization for Full Chip Scale
Guojin Chen, Wanli Chen, Yuzhe Ma, Haoyu Yang, Bei Yu - *Chinese Univ. of Hong Kong*

2B.2 Neural-ILT: Migrating ILT to Neural Networks for Mask Printability and Complexity Co-optimization
Bentian Jiang, Lixin Liu, Yuzhe Ma - *Chinese Univ. of Hong Kong*
Hang Zhang - *Cornell Univ.*
Bei Yu, Evangeline F.Y. Young - *Chinese Univ. of Hong Kong*

2B.3 Guiding Template Design for Lamellar DSA with Multiple Patterning and Self-Aligned Via Process
An-Jie Shih, Shao-Yun Fang, Yi-Yu Liu - *National Taiwan Univ. of Science and Technology*

2C - Safety and Energy Optimizations for Cyber-Physical Systems

Time: 8:30am - 9:00am

Moderator:

Mahdi Nikdast - *Colorado State Univ.*

This session focuses on optimizing safety-criticality, energy and performance in cyber-physical systems (CPS). The first paper proposes control adaptations for energy-efficient safety guarantees in machine learning-based CPS. The second paper explores the trade-off between the image generation accuracy of a GAN model and the energy consumed in mobile platforms. The third paper lays the foundation for applying probabilistic techniques in safety-critical platforms while ensuring that the functional correctness is not being violated. The last paper proposes an approach for reducing energy and improving performance in 3D resistive memories in a variety of CPS platforms.

***2C.1 Energy-Efficient Control Adaptation with Safety Guarantees for Learning-Enabled Cyber-Physical Systems**
Yixuan Wang, Chao Huang, Qi Zhu - *Northwestern Univ.*

2C.2 SETGAN: Scale and Energy Trade-off GANs for Image Applications on Mobile Platforms
Nitthilan Kannappan Jayakodi, Jana Doppa, Partha Pratim Pande - *Washington State Univ.*

2C.3 The Safe and Effective Application of Probabilistic Techniques in Safety-Critical Systems
Kunal Agrawal, Sanjoy Baruah - *Washington Univ. in St. Louis*
Zhishan Guo - *Univ. of Central Florida*
Jing Li - *New Jersey Institute of Technology*

2C.4 Accelerating 3D Vertical Resistive Memories with Opportunistic Write Latency Reduction
Wen Wen, Youtao Zhang, Jun Yang - *Univ. of Pittsburgh*

Special Session 2D - AIoT: The Powerful Convergence of AI and the IoT - An Industrial Perspective

Time: 8:30am - 9:00am

Moderator:

Yiran Chen - *Duke Univ.*

Organizers:

Yiran Chen - *Duke Univ.*
Yung-Hsiang Lu - *Purdue Univ.*

IoT (Internet of Things) is a disruptive technology that extends data collection to almost everything around us and enables them to react through intelligent data processing. Gartner estimates that the number of connected things will grow to over 20 billion by 2020. With recent innovative network and chip technologies, devices are becoming smarter with increasing compute power, bandwidth, and storage available on the device. This enables intelligent decision making and information transferring through the devices. Insights derived from data generated by IoT devices power new business scenarios and ensure long term success of existing business. Major IT solution providers have been investing in building IoT data platform to support customers to develop IoT solutions in different industry sectors such as smart cities, manufacturing, health care and transportation. These business scenarios impose both technical challenges and opportunities in building intelligent cloud and edge solutions.

The proposed special session includes three talks from both industry and academia, focusing on giving an integrated view about AIoT (AI for IoT) across three different levels – Devices, Software/Hardware Codesign, and System. The topics are also carefully selected to cover the areas that either are fully covered by regular submissions to ICCAD or the opinions from industry are not fully expressed in the past. All the speakers also have 10-20 years' experience in the relevant areas.

2D.2 Challenges for Building a Cloud Native Scalable and Trustable Multi-tenant AIoT Platform
Jinjun Xiong - *IBM Corp.*
Huamin Chen - *Red Hat, Inc.*

2D.3 Ambient Intelligence and Privacy
Vikram Tank, Alison Lentz, Carlos Mendonca, Marco Zamarato - *Google, Inc.*

3A - Brain-inspired, Bio-engineering, and Emerging Computing

Time: 9:00am - 9:30am

Moderator:

Debashis Sahoo - *Univ. of California, San Diego*

The emerging field of brain-inspired computing and bio-engineering computing has the potential to revolutionize the technology world. This session will showcase the state-of-the-art developments relevant to this fast-developing world of emerging computing. The first paper proposes an in-storage computing (ISC) solution that performs hyperdimensional computing (HDC). The second paper presents the near-data-processing accelerator for *k*-mer counting. The third paper develops a practical synthesis flow called PathDriver for the design automation of microfluidic biochips. The fourth paper introduces a Cascaded Echo State Network (CESN) to accelerate the detection efficiency and increase the robustness for MIMO-OFDM systems.

3A.1 THRIFTY: Training with Hyperdimensional Computing across Flash Hierarchy
Saransh Gupta, Justin L. Morris - *Univ. of California, San Diego & San Diego State Univ.*
Mohsen Imani - *Univ. of California, San Diego & Univ. of California, Irvine*
Ranganathan Ramkumar, Jeffrey Yu, Aniket Tiwari - *Univ. of California, San Diego*
Baris Aksanli - *San Diego State Univ.*
Tajana Rosing - *Univ. of California, San Diego*

3A.2 NEST: DIMM based Near-Data-Processing Accelerator for K-mer Counting
Wenqin Huangfu - *Univ. of California, Santa Barbara*
Krishna T. Malladi - *Samsung Semiconductor, Inc.*
Shuangchen Li, Peng Gu, Yuan Xie - *Univ. of California, Santa Barbara*

3A.3 PathDriver: A Path-Driven Architectural Synthesis Flow for Continuous-Flow Microfluidic Biochips
Xing Huang - *Tech. Univ. of Munich*
Youlin Pan - *Fuzhou Univ.*
Li Zhang, Bing Li - *Tech. Univ. of Munich*
Wenzhong Guo - *Fuzhou Univ.*
Tsung-Yi Ho - *National Tsing Hua Univ.*
Ulf Schlichtmann - *Tech. Univ. of Munich*

3A.4 Detection through Deep Neural Networks: A Reservoir Computing Approach for MIMO-OFDM Symbol Detection
Kangjun Bai, Lingjia Liu, Zhou Zhou, **Yang (Cindy) Yi** - *Virginia Polytechnic Institute and State Univ.*

3B - Novel Techniques for Improving Reliability and Manufacturability

Time: 9:00am - 9:30am

Moderator:

Yu Cao - *Arizona State Univ.*

CMOS scaling has made circuit design as well as mask layout design extremely difficult. The exploration covering broad ranges of techniques, from traditional CAD algorithms to machine learning techniques is actively carried out. The first paper in this session applies a feed-forward neural network for estimating aged gate delays of standard cells in a design library. The second paper proposes to apply generative learning models, by learning the inherent distribution of a given set of layouts, to the synthesis of layout patterns and their legalization. The third paper proposes an algorithm for accurate layout pattern matching through line sweep.

3B.1 Aadam: A Fast, Accurate, and Versatile Aging-Aware Cell Library Delay Model using Feed-Forward Neural Network

Seyed Milad Ebrahimipour - *Shahid Bahonar Univ.*
Behnam Ghavami - *Simon Fraser Univ.*
Hamid Mousavi - *Shahid Bahonar Univ.*
Mohsen Raji - *Shiraz Univ.*
Zhenman Fang, Lesley Shannon - *Simon Fraser Univ.*

3B.2 Layout Pattern Generation and Legalization with Generative Learning Models

Xiaopeng Zhang - *Chinese Univ. of Hong Kong*
James Shiely - *Synopsys, Inc.*
Evangeline F.Y. Young - *Chinese Univ. of Hong Kong*

3B.3 An Algorithm for Rule-based Layout Pattern Matching

Sheng-Hao Wang, Yen-Jong Chen, **Ting-Chi Wang** - *National Tsing Hua Univ.*
Oscar Chen - *AnaGlobe Technology, Inc.*

3C - Secure Architectures and Systems Design

Time: 9:00am - 9:30am

Moderator:

Michel Kinsy - *Texas A&M Univ.*

This session focuses on the design of secure architectures to mitigate among others cache-based side-channel attacks, secure embedded systems explorations using RISC-V and ARM ISAs, tightly integrated post-quantum algorithms accelerators, and securing neural network accelerators against certain classes of attack.

3C.1 RIMI: Instruction-level Memory Isolation for Embedded Systems on RISC-V
Haeyoung Kim, Jinjae Lee, Derry Pratama, Asep Muhamad Awaludin, Howon Kim, Donghyun Kwon - *Pusan National Univ.*

3C.2 Efficient Hardware/Software Co-Design for Post-Quantum Crypto Algorithm SIKE on ARM and RISC-V based Microcontrollers
Debapriya Basu Roy, Tim Fritzmann - *Tech. Univ. of Munich*
Georg Sigl - *Technische Univ. München*

3C.3 Hybrid-Shield: Accurate and Efficient Cross-Layer Countermeasure for Run-Time Detection and Mitigation of Cache-Based Side-Channel Attacks
Han Wang - *Univ. of California, Davis*
Hossein Sayadi, Avesta Sasan, Setareh Rafatirad, Houman Homayoun - *George Mason Univ.*

3C.4 Concurrent Weight Encoding-based Detection for Bit-Flip Attack on Neural Network Accelerators
Qi Liu, Wujie Wen - *Lehigh Univ.*
Yanzhi Wang - *Northeastern Univ.*

Embedded Tutorial 3D - Hardware/Software Co-Design for Machine Learning in Medicine

Time: 9:00am - 9:30am

Moderator:

Wujie Wen - *Lehigh Univ.*

Organizer:

Jingtong Hu - *Univ. of Pittsburgh*

Machine learning in healthcare is one area which is seeing rapid technology development and acceptance in the healthcare industry. Machine Learning (ML) in healthcare helps to analyze thousands of different data points and suggest outcomes, provide timely risk scores, precise resource allocation, and has many other applications. The increasingly growing number of applications of machine learning in healthcare allows us to glimpse at a future where data, analysis, and innovation work hand-in-hand to help countless patients without them ever realizing it. Soon, it will be quite common to find ML-based applications embedded with real-time patient data available from different healthcare systems, thereby increasing the efficacy of new treatment options which were unavailable before. In this tutorial, we will invite three speakers to talk about the latest development of applications of machine learning in healthcare, and how they stand to change the way we visualize the healthcare industry in the future.

In the first talk, the speaker will present a neural architecture search technique to automatically generate personalized deep neural networks for life-threatening ventricular arrhythmias (VA) detection in implantable cardioverter defibrillators. In the second talk, the speaker will present novel application of CNN in mobile devices in medical domain. In the third talk, the speaker will introduce new hardware platforms and neural network architecture design co-exploration techniques for fast and accurate magnetic resonance imaging (MRI) in various cardiac interventions.

3D.1 Personalized Deep Learning for Ventricular Arrhythmias Detection on Medical IoT Systems

Zhenge Jia, Zhepeng Wang - *Univ. of Pittsburgh*
Feng Hong, Lichuan Ping - *Singular Medical*
Yiyu Shi - *Univ. of Notre Dame*
Jingtong Hu - *Univ. of Pittsburgh*

3D.2 New Passive and Active Attacks on Deep Neural Networks in Medical Applications

Cheng Gongye, Hongjia Li, Xiang Zhang - *Northeastern Univ.*
Majid Sabbagh -
Geng Yuan, Xue Lin, Thomas Wahl, **Yunsi Fei** - *Northeastern Univ.*

3D.3 Towards Cardiac Intervention Assistance: Hardware-aware Neural Architecture Exploration for Real-time 3D Cardiac Cine MRI Segmentation

Dewen Zeng, Weiwen Jinag, Tianchen Wang - *Univ. of Notre Dame*
Xiaowei Xu - *Guangdong General Hospital*
Haiyun Yuan - *Harvard Medical School*
Meiping Huang, Jian Zhuang - *Guangdong General Hospital*
Jingtong Hu - *Univ. of Pittsburgh*
Yiyu Shi - *Univ. of Notre Dame*

Delivering Improved Design Performance by Applying Machine Learning to EDA

Time: 9:30am - 10:00am

Thank you to our Sponsor:

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Speaker:

Dr. Venkat Thanvantri

As advanced process nodes become ever smaller, design performance goals always seem to increase, not just for clock frequency, but also power and area. To meet these challenging requirements, Cadence continually research new, innovative, technologies which will help deliver the latest high performance silicon devices. Machine learning is a good example, and shows great potential to further improve digital design automation. During this paper Cadence will discuss how Machine Learning can being used within digital implementation tools, and as part of flow optimization, to deliver better productivity and design performance

Bio: Dr Venkat Thanvantri is VP of R&D at Cadence where he leads the AI/ML development for the Digital and Signoff Products. Venkat holds a PhD from University of Florida and a Master's from Indian Institute of Sciences. He has over 20 years of experience in developing, managing, and deploying multiple EDA tools in the areas of timing, extraction, characterization, power and place & route.

ACM Student Research Competition at ICCAD 2020

Time: 9:30am - 11:30am

The ACM Student Research Competition (SRC), sponsored by Microsoft, offers a unique forum for undergraduate and graduate students to present their original research at well-known ACM sponsored and co-sponsored conferences before a panel of judges and attendees. The ICCAD-edition of SRC features the following students and topics which are presented within three parallel sessions:

Session 1:

- Chuangtao Chen: Optimally Approximated Floating-Point Multiplier
- Sergi Alcaide, Leonidas Kosmidis, Carles Hernandez and Jaume Abella: Scheduling policies to enable GPUs for Critical Real-Time Automotive Systems
- Alejandro Calderón and Leonidas Kosmidis: GMAI: An Open Source Tool for Inspecting the Internals of GPU Memory Allocators
- Ivan Rodiguez-Ferrandez and Leonidas Kosmidis: An On-board Algorithm Implementation on an Embedded GPU: A Space Case Study
- Marc Benito and Leonidas Kosmidis: Evaluation of Graphics-based General Purpose Computation Solutions for Safety Critical Systems: An Avionics Case
- Namiko Matsumoto, Anthony Thomas and Tajana Rosing: Hyperdimensional Computing and Spectral Learning
- Anish Krishnakumar: An Intelligent Scheduling Paradigm for Heterogeneous Systems-on-Chip
- Chen Chen, Zirui Tao and Joshua San Miguel: Bufferless NoCs with Scheduled Deflection Routing information
- Mahabubul Alam and Swaroop Ghosh: Analysis and Optimization Methodologies for Quantum Approximate Optimization Algorithm
- Yuan-Hung Tsai, Jie-Hong R. Jiang and Chiao-Shan Jhang: Bit-Slicing the Hilbert Space: Scaling Up Accurate Quantum Circuit Simulation to a New Level
- Thomas Grurl and Robert Wille: Realistic and Efficient Simulation of Quantum Circuits Using Decision Diagrams

Session 2:

- Hao Geng and Bei Yu: Feature Learning in VLSI CAD
- Mingfei Yu and Masahiro Fujita: Parallel Scheduling Modern Deep Learning Implementations
- Bentian Jiang AIDA: Artificial Intelligence and Design Automation with Case Study on Layout-level Optimizations
- Sumit K. Mandal: Towards Efficient Hardware Architecture with Optimized Interconnect for DNNs
- Jiaqi Gu and David Z. Pan: Light in Artificial Intelligence: Efficient Neuromorphic Computing with Optical Neural Networks
- Mojan Javaheripi, Mohammad Samragh and Farinaz Koushanfar: Accelerated Shields for Safe and Robust Embedded Deep Learning
- Aryan Chaudhary and Saikat Mukhopadhyay: Artificial Intelligence in Health Sector

All speakers are denoted in bold | * denotes Best Paper Candidate | Note Agenda time zone is PST (UTC-8)

- Zihao Yuan and Ayse Coskun: Energy-Efficient Cooling Optimization Framework via Deep Learning
- Jun-Shen Wu, Chi-En Wang and Ren-Shuo Liu: Value-Aware Error Detection and Correction for SRAM Buffersin Low-Bitwidth, Floating-Point CNN Accelerators

Session 3:

- Xing Zhang and Xiaotong Cui: Use Graph-theoretic Models to Build and Optimize Trustworthy SoCs
- Lilas Alrahis and Hani Saleh: Novel Attack and Defense Strategies for Enhanced Logic Locking Security
- Debayan Das: Generic Low-overhead Electromagnetic and Power Side-Channel Attack Protection through Ground-Up Root-cause Analysis
- Mark Tressler and Kevin Sipple: A Flexible Framework for Attack and Defense Optimality in Split Manufacturing
- Nimisha Limaye: Security Assessment of Scan Locking Techniques for Design IP Protection
- Nithyashankari Gummidipoondi Jayasankaran, Adriana Sanabria-Borbon, Edgar Sanchez-Sinencio, Jiang Hu and Jeyavijayan Rajendran: Analog IP Protection and Evaluation
- Ai Quoc Dao: Gate-level Verification and ECO for Functional Safety
- Muhammad Usama Sardar: Formal Foundations for Remote Attestation in Intel SGX
- Shu-Ting Cheng: NBTI-Aware Heterogeneous Multi-Core System Design: An Energy-Efficient Standby-Sparing System Approach
- Alvaro Jover-Alvarez and Leonidas Kosmidis: Evaluation of the Computational Capabilities of High-Performance Heterogeneous Embedded Platforms for Safety Critical Systems
- Shreyas Kolala Venkataramanaiah and Jae-Sun Seo FPGA-based Energy-Efficient CNN Training Accelerator

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All speakers are denoted in bold | * denotes Best Paper Candidate | Note Agenda time zone is PST (UTC-8)

TUESDAY SCHEDULE

6:30 - 7:00am

4A: New Techniques for NoC Design and Optimization to Beat Handcrafting

4B: Deep Learning Acceleration: Bridging the Gap Between Software and Hardware

4C: EDA for Security

Special Session 4D: Computer-Aided Analog and Mixed-Signal Design from System to Layout

7:00 - 8:00am

IEEE CEDA Keynote: Interplay of Design and Operation to Enable Adaptive and Robust Cyber Physical (Production) Systems

Birgit Vogel-Heuser - Tech. Univ. of Munich

8:00 - 8:30am

5A: Integrating Novel Memory Technologies to Optimize System Performance or Area

5B: DNN Acceleration on GPGPU and FPGA Platforms

5C: Side Channel Attacks and Defenses

Special Session 5D: 2020 CAD Contest at ICCAD

8:30 - 9:00am

6A: How to Exploit FPGA Platforms for Application-Specific Acceleration

6B: Safeguarding Deep Learning Towards Secure and Robust Artificial Intelligence

6C: Logic Locking: Arms Race

Special Session 6D: Design Automation for Autonomous Systems: Uncertainty-Aware Behavior Assurance

All speakers are denoted in bold | * denotes Best Paper Candidate | Note Agenda time zone is PST (UTC-8)

TUESDAY SCHEDULE

9:00 - 9:30am

7A: Emerging Technologies and Innovative Applications in Synthesis

7B: Efficient Deep Learning Inference and Training Towards Green AI

7C: In-Memory Computing for Hardware Acceleration

Special Session 7D: Opensource Tools and Platforms for Agile Development of Specialized Architectures

9:30 - 10:00am

8A: Cross-layer Design for Timing Resilient Embedded Systems

8B: ReRAM-based Accelerators for Neural Networks

8C: Safety and Security Validation

Special Session 8D: Taking Open-Source EDA to the Next Level: From Research to Production IC Design

All speakers are denoted in bold | * denotes Best Paper Candidate | Note Agenda time zone is PST (UTC-8)

4A - New Techniques for NoC Design and Optimization to Beat Handcrafting

Time: 6:30am - 7:00am

Moderator:

Theocharis Theocharides - *Univ. of Cyprus*

This session covers new EDA techniques for NoC design and optimization. The first paper proposes a new NoC synthesis tool to create custom NoC designs optimized for power, performance and area that outperform handcrafted designs using behavior specifications and relying on traffic conflict graphs and combinatorial optimization techniques. The second paper presents a novel analytical approach to estimate the end-to-end latency of priority-aware NoC designs with deflection routing under different traffic types. The third paper presents a new EDA-based approach for wavelength routed optical NoC designs to minimize laser power.

4A.1 Automated Synthesis of Custom Networks-on-Chip for Real World Applications
Anup Gangwar, Nitin Kumar Agarwal, Ravishankar Sreedharan, Ambica Prasad, Sri Harsha Gade - *Arm, Ltd.*
Zheng Xu - *Consultant*

4A.2 Performance Analysis of Priority-Aware NoCs with Deflection Routing under Traffic Congestion
Sumit K. Mandal, Anish Krishnakumar - *Univ. of Wisconsin, Madison*
Raid Ayoub, Michael Kishinevsky - *Intel Corp.*
Umit Y. Ogras - *Univ. of Wisconsin, Madison*

4A.3 PSION 2: Optimizing Physical Layout of Wavelength-Routed ONoCs for Laser Power Reduction
Alexandre Truppel, Tsun-Ming Tseng, Ulf Schlichtmann - *Tech. Univ. of Munich*

4B - Deep Learning Acceleration: Bridging the Gap Between Software and Hardware

Time: 6:30am - 7:00am

Moderator:

Andrea Calimera - *Politecnico di Torino*

The ubiquitous adoption of AI technologies passes through an efficient implementation of Deep Learning. While algorithmic advances enabled highly accurate Deep Neural Networks (DNNs), there is still an urgent need to push down the cost for processing them. This session proposes four papers dealing with the acceleration of DNNs and their training, introducing new HW/SW design & optimization strategies where energy and throughput are the main objectives. The first paper describes GAMMA, a domain-specific genetic algorithm for the optimal mapping of the DNN layers into spatial neural accelerators. The design of a Convolutional Neural Networks (CNNs) accelerator featuring logarithmic data representation and three-dimensional organization of tightly coupled processing elements is the focus of the second paper. In contrast, the third paper proposes a many-core chip with a specialized Network-on-Chip for efficient Deep Reinforcement Learning (DRL). The fourth paper introduces an architecture for a new approximate DRAM refresh mechanism, which achieves high energy efficiency while not affecting the quality of the training stage.

4B.1 GAMMA: Automating the HW Mapping of DNN Models on Accelerators via Genetic Algorithm
Sheng-Chun Kao, Tushar Krishna - *Georgia Institute of Technology*

4B.2 NeuroMAX: A High Throughput, Multi-Threaded, Log-Based Accelerator for Convolutional Neural Networks
Mahmood Azhar Qureshi, Arslan Munir - *Kansas State Univ.*

4B.3 A Many-Core Accelerator Design for On-Chip Deep Reinforcement Learning
Ying Wang - *Chinese Academy of Sciences & State Key Laboratory of Computer Architecture*
Mengdi Wang - *Chinese Academy of Sciences & Univ. of Chinese Academy of Sciences*
Bing Li - *Capital Normal Univ.*
Huawei Li - *Chinese Academy of Sciences & State Key Laboratory of Computer Architecture*
Xiaowei Li - *Chinese Academy of Sciences & State Key Laboratory of Computer Architecture*

4B.4 DRAMA: An Approximate DRAM Architecture for High-performance and Energy-efficient Deep Training System
Duy-Thanh Nguyen, Chang-Hong Min - *Kyung Hee Univ.*
Nhut-Minh Ho - *National Univ. of Singapore*
Ik-Joon Chang - *Kyung Hee Univ.*

4C - EDA for Security

Time: 6:30am - 7:00am

Moderator:

Jeyavijayan Rajendran - *Texas A&M Univ.*

This session covers a variety of EDA for security research works focusing on hardware security assessment and defense techniques. The first paper presents a CAD framework to assess the learnability of physical unclonable functions automatically. The second paper develops a method for generating synthetic hardware security benchmarks. The third paper introduces a benchmark suite for laser fault injection attacks. The fourth paper explores Boolean masking of neural network hardware design to defend against power side-channel attacks.

4C.1 PUF-G: A CAD Framework for Automated Assessment of Provable Learnability from Formal PUF Representations
Durba Chatterjee, Debdeep Mukhopadhyay, Aritra Hazra - *Indian Institute of Technology Kharagpur*

4C.2 Adaptable and Divergent Synthetic Benchmark Generation for Hardware Security
Sarah Amir, Domenic Forte - *Univ. of Florida*

4C.3 Laser Attack Benchmark Suite
Burin Amornpaisannon, Andreas Diavastos, Li-Shiuan Peh, Trevor E. Carlson - *National Univ. of Singapore*

4C.4 BoMaNet: Boolean Masking of an Entire Neural Network
Anuj Dubey - *North Carolina State Univ.*
Rosario Cammarota - *Intel Corp. & IEEE*
Aydin Aysu - *North Carolina State Univ.*

Special Session 4D - Computer-Aided Analog and Mixed-Signal Design from System to Layout

Time: 6:30am - 7:00am

Moderators:

Mark Po-Hung Lin - *National Chiao Tung Univ.*
Sachin Sapatnekar - *Univ. of Minnesota*

Organizers:

Mark Po-Hung Lin - *National Chiao Tung Univ.*
Sachin Sapatnekar - *Univ. of Minnesota*

Analog and mixed-signal (AMS) integrated circuits (ICs) are essential in many system-on-chip (SoC) and internet-of-thing (IoT) applications. Although design automation for AMS ICs has been researched for decades, modern AMS design still requires much designers' effort with limited qualified computer-aided design (CAD) tools. Consequently, it usually takes a long design cycle from system to layout design. The proposed special session addresses the state-of-the-art computer-aided AMS design, which consists of four presentations on current progress and new advancement. The topics cover modeling and simulation of statistical characteristics for an AMS system, structural synthesis and modeling of various operational amplifiers, a newly developed open-source analog layout generator and its roadmap, and a layout synthesis methodology through learning and migration.

4D.1 Modeling and Simulation of NAND Flash Memory Sensing Systems with Cell-to-Cell Vth Variations
Nayoung Choi - *Seoul National Univ., Samsung Electronics*
Jaeha Kim - *Seoul National Univ.*

4D.2 Structural Synthesis of Operational Amplifiers Based on Functional Block Modeling
Inga Abel, Helmut Graeb - *Tech. Univ. of Munich*

4D.3 The ALIGN Open-Source Analog Layout Generator: v1.0 and Beyond
Tonmoy Dhar, Kishor Kunal - *Univ. of Minnesota*
Yaguang Li, Yishuang Lin - *Texas A&M Univ.*
Meghna Madhusudan, Jitesh Poojary, Arvidd K. Sharma - *Univ. of Minnesota*
Steven M. Burns - *Intel Corp.*
Ramesh Harjani - *Univ. of Minnesota*
Jiang Hu - *Texas A&M Univ.*
Parijat Mukherjee, Soner Yaldiz - *Intel Corp.*
Sachin Sapatnekar - *Univ. of Minnesota*

4D.4 Achieving Analog Layout Integrity through Learning and Migration
Mark Po-Hung Lin, Hao-Yu Chi, Abhishek Patyal - *National Chiao Tung Univ.*
Zheng-Yao Liu, Jun-Jie Zhao - *National Chung Cheng Univ.*
Chien-Nan Jimmy Liu, Hung-Ming Chen - *National Chiao Tung Univ.*

Keynote IEEE CEDA: Interplay of Design and Operation to Enable Adaptive and Robust Cyber Physical (Production) Systems

Time: 7:00am - 8:00am

Speaker:

Birgit Vogel-Heuser - *Tech. Univ. of Munich*

Data-Driven Model and System Evolution enable adaptive and robust Cyber Physical (Production) Systems for example by continuously increasing simulation accuracy during design and a more coarse grained simulation during operation to fulfill real-time requirements. Capturing and analyzing data throughout the entire life cycle of a CPPS will allow drawing conclusions about the benefits and weaknesses of CPPS designs as well as its configuration during operation. The status and future challenges of design automation and optimization for CPPSs will be covered.

Biography: Prof. Vogel-Heuser received her Dipl. Ing. degree in electrical engineering in 1987 and her Dr.-Ing. degree in mechanical engineering in 1990 from the RWTH Aachen, Germany. She acquired industrial experience over ten years, including a position as manufacturing director for the Siempelkamp Group. After various professorship positions in Hagen, Wuppertal, and Kassel, she was appointed to the Chair of Automation and Information Systems at TUM in 2009. She is speaker of the DFG Collaborative Research Centre 768 “Managing cycles in innovation processes”, member of the coordination board of the DFG Priority Program 1593 “Design for Future” and member of the National Academy of Science and Engineering (acatech).

5A - Integrating Novel Memory Technologies to Optimize System Performance or Area

Time: 8:00am - 8:30am

Moderator:

Marina Zapater - *Univ. of Applied Sciences and Arts Western Switzerland*

This session presents different approaches to exploit novel memory technologies for new applications to optimize performance, area or resilience at the system level. The first paper proposes a genome read mapping accelerator using approximate Ternary Content Addressable Memories (TCAM). The second paper presents Automatic-SSD, a new controller design for new non-volatile memories, such as phase change or 3D Xpoint, that can reduce latency and power consumption due to currently used firmware for such memories. The third paper proposes a novel machine learning technique using a small artificial neural network to dynamically partition the SSD cache based on an analysis of the level of reuse within each stream. The fourth paper in this session presents the benefits of a small on-chip ECC cache to improve performance during the insertion and deletion of entries in contrast to the verify-after-write approach used today to tackle stuck-at faults in phase change memories.

5A.1 Seed-and-Vote based In-Memory Accelerator for DNA Read Mapping
Ann Franchesca Laguna - *Univ. of Notre Dame*
Hasindu Gamaarachchi - *Univ. of New South Wales*
Xunzhao Yin - *Zhejiang Univ.*
Michael T. Niemier - *Univ. of Notre Dame*
Sridevan Parameswaran - *Univ. of New South Wales*
Xiaobo Sharon Hu - *Univ. of Notre Dame*

5A.2 Automatic-SSD: Full Hardware Automation over New Memory for High Performance and Energy Efficient PCIe Storage Cards
Gyuyoung Park, Myoungsoo Jung - *Korea Advanced Institute of Science and Technology*

5A.3 MLCache: A Space-Efficient Cache Scheme based on Reuse Distance and Machine Learning for NVMe SSDs
Weiguang Liu, Jinhua Cui, Junwei Liu, Laurence T. Yang - *Huazhong Univ. of Science & Technology*

5A.4 ECC Cache: A Lightweight Error Detection for Phase-Change Memory Stuck-At Faults
Chao Zhang, Khaled Abdelaal, Angel Chen, Xinhui Zhao, Wujie Wen, Xiaochen Guo - *Lehigh Univ.*

5B - DNN Acceleration on GPGPU and FPGA Platforms

Time: 8:00am - 8:30am

Moderator:

Tinoosh Mohsenin - *Univ. of Maryland, Baltimore County*

GPGPU and FPGA have been widely used to accelerate computations of Deep Neural Networks (DNNs). This session introduces three papers tackling state-of-the-art challenges in DNN acceleration on GPGPU and FPGA platforms: The first paper presents a technique to accelerate graph convolutional neural network training on GPGPU. The second paper introduces a framework to model and explore DNN accelerator design on FPGA. The third paper discusses a systematic optimization method to encode, model and architect FPGA acceleration of spiking neural networks.

5B.1 fuseGNN: Accelerating Graph Convolutional Neural Network Training on GPGPU

Zhaodong Chen, Mingyu Yan - *Univ. of California, Santa Barbara & Univ. of California, Santa Barbara*
Maohua Zhu, Lei Deng - *Univ. of California, Santa Barbara*
Guoqi Li - *Tsinghua Univ.*
Shuangchen Li - *Alibaba Group*
Yuan Xie - *Univ. of California, Santa Barbara*

5B.2 DNNExplorer: A Framework for Modeling and Exploring a Novel Paradigm of FPGA-based DNN Accelerator

Xiaofan Zhang, Hanchen Ye - *Univ. of Illinois at Urbana-Champaign*
Junsong Wang, Yonghua Lin - *E-Vision AI*
Jinjun Xiong - *IBM Research*
Wen-mei Hwu, Deming Chen - *Univ. of Illinois at Urbana-Champaign*

5B.3 Encoding, Model, and Architecture: Systematic Optimization for Spiking Neural Network in FPGAs

Haowen Fang, Zaidao Mei, Amar Shrestha, Ziyi Zhao, Yilan Li, Qinru Qiu - *Syracuse Univ.*

5C - Side Channel Attacks and Defenses

Time: 8:00am - 8:30am

Moderator:

Hossein Sayadi - *California State Univ. Long Beach*

This session covers side-channel attack and defense techniques under a variety of hardware security scenarios. The first paper introduces two new information leakage attacks targeting the FPGA routing and logic elements. The second paper develops a quantitative defense framework to mitigate the attacks against power distribution networks on multi-tenant FPGAs. The third paper proposes an online defense mechanism to detect voltage drops due to power side-channel attacks in power grids. The fourth paper presents a systematic methodology to develop fault templates of Boolean circuits that can attack a popular defense against side-channel analysis.

5C.1 Information Leakage from FPGA Routing and Logic Elements
Ilias Giechaskiel - *Independent Researcher*
Jakub Szefer - *Yale Univ.*

5C.2 A Quantitative Defense Framework against Power Attacks on Multi-tenant FPGA
Yukui Luo, Xiaolin Xu - *Northeastern Univ.*

5C.3 Power Side Channel Attack Analysis and Detection
Navyata Gattu, Mohammad Nasim Imtiaz Khan, Asmit De, **Swaroop Ghosh** - *Pennsylvania State Univ.*

5C.4 Faultless to a Fault? The Case of Threshold Implementations of Crypto-systems vs Fault Template Attacks
Debdeep Mukhopadhyay - *Indian Institute of Technology Kharagpur*

Special Session 5D - 2020 CAD Contest at ICCAD

Time: 8:00am - 8:30am

Moderators:

Tsung-Wei Huang - *Univ. of Utah*
Mark Po-Hung Lin - *National Chiao Tung Univ.*

Organizers:

Ing-Chao Lin - *National Cheng Kung Univ.*
Ulf Schlichtmann - *Technical Univ. of Munich*
Tsung-Wei Huang - *Univ. of Utah*
Mark Po-Hung Lin - *National Chiao Tung Univ.*

The CAD Contest at ICCAD (https://iccad-contest.org/2020/) is a challenging, multi-month, research & development competition, focusing on advanced, real-world problems in the field of Electronic Design Automation (EDA). Contestants can participate in one or more problems provided by EDA/IC industry. The winners will be awarded at an ICCAD special session dedicated to this contest. Since 2012, the CAD Contest at ICCAD has been attracting more than a hundred teams per year, fostering productive industry-academia collaborations, and leading to hundreds of publications in top-tier conferences and journals. The contest keeps enhancing its impact and boosts EDA research.

5D.1 Overview of 2020 CAD contest at ICCAD
Ing-Chao Lin - *National Cheng Kung Univ.*
Ulf Schlichtmann - *Tech. Univ. of Munich*
Tsung-Wei Huang - *Univ. of Utah*
Mark Po-Hung Lin - *National Chiao Tung Univ.*

5D.2 ICCAD-2020 CAD Contest in X-value Equivalence Checking and Benchmark Suite
Jacky (Chih-Jen) Hsu, Rocky (Chi-An) Wu, Ching-Yi Huang, Kei-Yong Khoo - *Cadence Design Systems, Inc.*

5D.3 ICCAD-2020 CAD Contest in Routing with Cell Movement
Kai-Shun Hu, Ming-Jen Yang, Tao-Chun Yu, Guan-Chuen Chen - *Synopsys, Inc.*

5D.4 Problem C: GPU Accelerated Logic Re-simulation
Yanqing Zhang, Haoxing Ren, Ben Keller, Brucek Khailany - *Nvidia Corp.*

5D.5 DATC RDF-2020: Strengthening the Foundation for Academic Research in IC Physical Design
Jianli Chen - *Fudan Univ. & Fuzhou Univ.*
Iris Hui-Ru Jiang - *National Taiwan Univ.*
Jinwook Jung - *IBM Research*
Andrew B. Kahng - *Univ. of California, San Diego*
Victor N. Kravets - *IBM Research*
Yi-Lang Li, Shih-Ting Lin - *National Chiao Tung Univ.*
Mingyu Woo - *Univ. of California, San Diego*

6A - How to Exploit FPGA Platforms for Application-Specific Acceleration

Time: 8:30am - 9:00am

Moderator:

Marco Santambrogio - *Polytechnic Univ. of Milan*

This session covers new approaches to exploit FPGA platforms in the context of application-specific acceleration and performance improvement. The first paper presents LegoGNN, a new framework that generates and optimizes automatically graph network accelerators on FPGA platforms. The second paper proposes SuSy, a new framework to generate FPGA-based implementations of systolic arrays using uniform recurrence equations. The third paper presents an FPGA accelerator with high bandwidth HBM2 memory for training CNNs in a low batch number to improve performance and energy efficiency.

6A.1 DeepBurning-GL: an Automated Framework for Generating Graph Neural Network Accelerators

Shengwen Liang - *Chinese Academy of Sciences & Univ. of Chinese Academy of Sciences*
Cheng Liu - *Chinese Academy of Sciences & Univ. of Chinese Academy of Sciences*
Ying Wang - *Chinese Academy of Sciences & Univ. of Chinese Academy of Sciences*
Huawei Li - *Chinese Academy of Sciences & Univ. of Chinese Academy of Sciences*
Xiaowei Li - *Chinese Academy of Sciences & Univ. of Chinese Academy of Sciences*

6A.2 SuSy: A Programming Model for Productive Construction of High-Performance Systolic Arrays on FPGAs

Yi-Hsiang Lai - *Cornell Univ.*
Hongbo Rong - *Intel Corp.*
Size Zheng - *Peking Univ.*
Weihao Zhang - *Tsinghua Univ.*
Xiuping Cui, Yunshan Jia - *Peking Univ.*
Jie Wang - *Univ. of California, Los Angeles*
Brendan Sullivan, Zhiru Zhang - *Cornell Univ.*
Yun (Eric) Liang - *Peking Univ.*
Youhui Zhang - *Tsinghua Univ.*
Jason Cong - *Univ. of California, Los Angeles*
Nithin George, Jose Alvarez, Christopher J Hughes, Pradeep K. Dubey - *Intel Corp.*

6A.3 FPGA-based Low-Batch Training Accelerator for Modern CNNs Featuring High Bandwidth Memory

Shreyas Kolala Venkataramanaiah, Han-Sok Suh, Shihui Yin - *Arizona State Univ.*
Eriko Nurvitadhi, Aravind Dasu - *Intel Corp.*
Yu Cao, Jae-sun Seo - *Arizona State Univ.*

6B - Safeguarding Deep Learning Towards Secure and Robust Artificial Intelligence

Time: 8:30am - 9:00am

Moderator:

Wei Yan - *Clarkson Univ.*

Despite their versatile capabilities and widespread applications, deep learning models are known to be susceptible to adversarial attacks and accuracy degradations, compromising the reliability of the artificial intelligence systems they enable. In this session, we will introduce several intelligent techniques to deal with such challenges: The first paper presents a SW/HW co-design approach to achieve anomalous feature suppression against bit-error propagation; followed by an algorithmic approach detailed in the second paper that leverages the Hessian of the weight matrix to identify and protect sensitive parameters against process variations in emerging non-volatile memory-based Processing-in-Memory (PIM) architecture. The final paper of the session devises a lightweight implementation to embed XOR cipher to protect DNN models inside Compute-in-Memory (CIM) SRAM architecture.

6B.1 **Just Say Zero: Containing Critical Bit-Error Propagation in Deep Neural Networks With Anomalous Feature Suppression**
Elbruz Ozen, Alex Orailoglu - *Univ. of California, San Diego*

6B.2 **Hessian-Driven Unequal Protection of DNN Parameters for Robust Inference**
Saurabh Dash, Saibal Mukhopadhyay - *Georgia Institute of Technology*

6B.3 **XOR-CIM: Compute-in-Memory SRAM Architecture with Embedded XOR Encryption**
Shanshi Huang, Hongwu Jiang, Xiaochen Peng, Wantong Li, Shimeng Yu - *Georgia Institute of Technology*

6C - Logic Locking: Arms Race

Time: 8:30am - 9:00am

Moderator:

Xiaolin Xu - *Northeastern Univ.*

Logic locking techniques aim to address the important security concerns in the IC supply chain, such as piracy. In this session, we have three papers on the recent developments of logic locking research. The first paper introduces a canonical prune-and-SAT attack for breaking the state-of-the-art routing-based obfuscation techniques. The second paper discusses a neural network guided SAT attack against logic locked complex structures. The third paper demonstrates two SAT modeling techniques that can speed up the attacks on logic locking.

6C.1 **InterLock: An Intercorrelated Logic and Routing Locking**
Hadi Mardani Kamali, Kimia Zamiri Azar - *George Mason Univ.*
Houman Homayoun - *Univ. of California, Davis*
Avesta Sasan - *George Mason Univ.*

6C.2 **NNgSAT: Neural Network guided SAT Attack on Logic Locked Complex Structures**
Kimia Zamiri Azar, **Hadi Mardani Kamali** - *George Mason Univ.*
Houman Homayoun - *Univ. of California, Davis*
Avesta Sasan - *George Mason Univ.*

6C.3 **Modeling Techniques for Logic Locking**
Joseph P. Sweeney, Marijn J.H. Heule, Lawrence Pileggi - *Carnegie Mellon Univ.*

Special Session 6D - Design Automation for Autonomous Systems: Uncertainty-Aware Behavior Assurance

Time: 8:30am - 9:00am

Moderator:
Xin Li - *Duke Univ.*

Organizer:
Shiyan Hu - *Univ. of Southampton*

Autonomous systems are self-governed and self-adaptive systems that comply with high assurance correctness and safety criteria. They rely on a collection of intelligent components to sense their environment for operations. Those sensing components often manifest significant uncertainties due to noise from system inputs as well as disturbances from environment interferences, system faults, malicious attacks, etc. It is imperative to test and verify the goal-driven autonomous behavior considering various sources of uncertainties. This special session consists of four talks tackling the challenge of autonomous behavior assurance. The first talk gives an overview on the challenge to assure safe autonomous behavior at design time using appropriate architectures, supervision, and online tools. The second talk discusses how formal methods can be developed to ensure the safe application of machine learning techniques, modelling techniques, and design techniques in autonomous systems. The third talk focuses on the development of a new data analytics technique for counteracting adversarial attacks in stereo vision based autonomous driving systems. The fourth talk describes an industrial experience on preliminary evaluation of machine learning assurance technologies that have been integrated into aerospace autonomous platforms.

6D.1 EDA for Autonomous Behavior Assurance
Selma Saidi - *TU Dortmund*
Jyotirmoy Deshmukh - *USC*
Dirk Ziegenbein - *Bosch Research*
Rolf Ernst - *TU Braunschweig*

6D.2 Know the Unknowns: Addressing Disturbances and Uncertainties in Autonomous Systems
Qi Zhu - *Northwestern Univ.*
Wenchao Li - *Boston Univ.*
Hyoseung Kim, Yecheng Xiang - *Univ. of California, Riverside*
Kacper Wardega - *Boston Univ.*
Zhilu Wang, Yixuan Wang, Hengyi Liang, Chao Huang - *Northwestern Univ.*
Jiameng Fan - *Boston Univ.*
Hyunjong Choi - *Univ. of California, Riverside*

6D.3 Counteracting Adversarial Attacks in Autonomous Driving
Qi Sun, Arjun Ashok Rao - *Chinese Univ. of Hong Kong*
Xufeng Yao, Bei Yu - *CUHK*
Shiyan Hu - *Univ. of Southampton*

6D.4 Towards Assurance Evaluation of Autonomous Systems
Steven Beland, Isaac Chang, Alexander Chen, Matthew Moser, James Paunicka, Douglas Stuart, John Vian, Christina Westover, **Huafeng Yu** - *Boeing*

7A - Emerging Technologies and Innovative Applications in Synthesis

Time: 9:00am - 9:30am

Moderator:

Christian Pilato - *Polytechnic Univ. of Milan*

This session is devoted to emerging technologies and innovative applications in synthesis. The first paper presents a novel retiming formulation for superconductive circuits. The second paper leverages Boolean reasoning for mining biochemical circuits from enzyme databases. The third paper introduces a neural network-based FPGA delay prediction method for high-level synthesis.

7A.1 Retiming for High-performance Superconductive Circuits with Register Energy Minimization
Ting-Ru Lin, Massoud Pedram - *Univ. of Southern California*

7A.2 Mining Biochemical Circuits from Enzyme Databases via Boolean Reasoning
Yu-Chou Lin, **Jie-Hong Roland Jiang** - *National Taiwan Univ.*

7A.3 Accurate Operation Delay Prediction for FPGA HLS Using Graph Neural Networks
Ecenur Ustun, Chenhui Deng, Debjit Pal, Zhijing Li, Zhiru Zhang - *Cornell Univ.*

7B - Efficient Deep Learning Inference and Training Towards Green AI

Time: 9:00am - 9:30am

Moderator:

Yingyan Lin - *Rice Univ.*

Recent breakthroughs of deep learning have motivated a tremendous demand for bringing deep learning-powered intelligence into numerous resource-constrained daily life devices. However, powerful deep learning often comes with prohibitive costs, limiting their more extensive applications and raising various environmental concerns. As such, recently, there have been explosive research efforts aiming to address these limitations and concerns towards ubiquitous green AI. This session will present solutions for efficient deep learning inference and training from various aspects.

7B.1 HyperTune: Dynamic Hyperparameter Tuning for Efficient Distribution of DNN Training Over Heterogeneous Systems
Ali HeydariGorji, Siavash Rezaei - *Univ. of California, Irvine*
Mahdi Torabzadehkashi, Hossein Bobarshad, Vladimir Alves - *NGD Systems, Inc*
Pai Chou - *Univ. of California, Irvine*

7B.2 SynergicLearning: Neural Network-Based Feature Extraction for Highly-Accurate Hyperdimensional Learning
Mahdi Nazemi, Amirhossein Esmaili, Arash Fayyazi, Massoud Pedram - *Univ. of Southern California*

7B.3 Optimizing Stochastic Computing for Low Latency Inference of Convolutional Neural Networks
Zhiyuan Chen, **Yufei Ma**, Zhongfeng Wang - *Nanjing Univ.*

7B.4 HAPI: Hardware-Aware Progressive Inference
Stefanos Laskaridis, **Stylianos I. Venieris**, Hyeji Kim - *Samsung AI Center Cambridge*
Nicholas D. Lane - *Samsung AI Center Cambridge & Univ. of Cambridge*

7C - In-Memory Computing for Hardware Acceleration

Time: 9:00am - 9:30am

Moderator:

Jae-sun Seo - *Arizona State Univ.*

Crossbar arrays with resistive random access memory (ReRAM) or static random access memory (SRAM) are common technologies for enabling in-memory computing. The first paper will discuss using a ReRAM crossbar for a Natural Language Processing (NLP) model acceleration. The second paper will present a programming protocol to precisely tune the ReRAM conductance for accurate computation. The third paper will discuss how to leverage the conventional 6-transistor SRAM to implement a binary neural network with negligible accuracy degradation.

7C.1 **ReTransformer: ReRAM-based Processing-in-Memory Architecture for Transformer Acceleration**
Xiaoxuan Yang, Bonan Yan, Hai Li, Yiran Chen - *Duke Univ.*

7C.2 **SWIPE: Enhancing Robustness of ReRAM Crossbars for In-memory Computing**
Sujan K. Gonugondla, Ameya D. Patil, Naresh R. Shanbhag - *Univ. of Illinois at Urbana-Champaign*

7C.3 **Energy-efficient XNOR-free In-Memory BNN Accelerator with Input Distribution Regularization**
Hyungjun Kim, Hyunmyung Oh, Jae-Joon Kim - *Pohang Univ. of Science and Technology*

Special Session 7D - Opensource Tools and Platforms for Agile Development of Specialized Architectures

Time: 9:00am - 9:30am

Moderator:

Antonino Tumeo - *Pacific Northwest National Lab*

Organizer:

Antonino Tumeo - *Pacific Northwest National Lab*

As new technology nodes have started to progressively provide diminishing returns in terms of power consumption and performance, we have entered a new golden era for domain-specific architectures at all system scales. However, developing specialized architectures currently requires substantial efforts and large teams, for both hardware and software. Several research initiatives are developing new tools, interfaces, intellectual properties, and platforms to enable small development teams to explore and implement specialized systems with quick, modularized, and fail fast (Agile). At the same time, there is a desire to provide opensource, community driven, and interoperable systems to maximize reuse and facilitate integration. The talks of this special session discuss openly available tools and platforms that allows to quickly transition the design of specialized architectures from the high-level algorithmic descriptions to their implementation.

7D.1 Your Agile Open Source HW Stinks (Because It Is Not a System)
Michael B. Taylor - *Univ. of Washington*

7D.2 Agile SoC Development with Open ESP
Paolo Mantovani, Davide Giri, Giuseppe Di Guglielmo, Luca Piccolboni, Joseph Zuckerman - *Columbia Univ.*
Emilio G. Cota, Michele Petracca, Christian Pilato, Luca P. Carloni - *Columbia Univ.*

7D.3 A Simulator and Compiler Framework for Agile Hardware-Software Co-designs Evaluation and Exploration
Tyler Sorensen - *UC Santa Cruz*
Aninda Manocha, Esin Tureci, Marcelo Orenes Vera - *Princeton Univ.*
Juan L. Aragón - *Univ. of Murcia*
Margaret Martonosi - *Princeton Univ.*

7D.4 SODA: a New Synthesis Infrastructure for Agile Hardware Design of Machine Learning Accelerators
Marco Minutoli, Vito Giovanni Castellana, Cheng Tan, Joseph Manzano, Vinay Amatya, Antonino Tumeo - *Pacific Northwest National Lab*
David Brooks, Gu-Yeon Wei - *Harvard Univ.*

8A - Cross-layer Design for Timing Resilient Embedded Systems

Time: 9:30am - 10:00am

Moderator:

Song Han - *Univ. of Connecticut*

For the design of many safety-critical systems, a key challenge is to meet the stringent timing requirements and ensure functional correctness with limited resources. The three papers in this session address this challenge with novel cross-layer methods, including co-designing sampling periods and poles of real-time controller to improve control performance and system schedulability for time-sensitive networking, scheduling mixed-criticality systems precisely on a varying-speed processor for guaranteeing the completion of every task, and relaxing traditional hard deadlines with weakly-hard constraints to improve system fault tolerance while ensuring schedulability and control stability.

8A.1 Fixed-Priority Scheduling and Controller Co-Design for Time-Sensitive Networks
Xiaotian Dai, Shuai Zhao - *Univ. of York*
Yu Jiang - *Tsinghua Univ.*
Xun Jiao - *Villanova Univ.*
Xiaobo Sharon Hu - *Univ. of Notre Dame*
Wanli Chang - *Univ. of York*

8A.2 F2VD: Fluid Rates to Virtual Deadlines for Precise Mixed-Criticality Scheduling on a Varying-Speed Processor
Kecheng Yang - *Texas State Univ.*
Ashikahmed Bhuiyan, Zhishan Guo - *Univ. of Central Florida*

8A.3 Leveraging Weakly-hard Constraints for Improving System Fault Tolerance with Functional and Timing Guarantees
Hengyi Liang, Zhilu Wang, Ruochen Jiao, Qi Zhu - *Northwestern Univ.*

8B - ReRAM-based Accelerators for Neural Networks

Time: 9:30am - 10:00am

Moderator:

Marco Donato - *Tufts Univ.*

ReRAM hardware accelerators provide high energy efficiency for data-intensive applications such as Deep Neural Network inference. However, device non-idealities pose significant challenges to the design of reliable and scalable ReRAM-based hardware. The papers in this session offer a range of solutions from circuit-level optimizations, new processing-in-memory architectures, and HW/SW co-design.

8B.1 Thermal-aware Optimization Framework for ReRAM-based Deep Neural Network Acceleration
Hyein Shin, Myeonggu Kang, Lee-Sup Kim - *Korea Advanced Institute of Science and Technology*

8B.2 Unlocking Wordline-level Parallelism for Fast Inference on RRAM-based DNN Accelerator
Yeonhong Park, Seung Yul Lee, Hoon Shin, Jun Heo, Tae Jun Ham, Jae W. Lee - *Seoul National Univ.*

8B.3 MobiLattice: A Depth-wise DCNN Accelerator with Hybrid Digital/Analog Nonvolatile Processing-In-Memory Block
Qilin Zheng, Xingchen Li, Zongwei Wang, Yimao Cai, Guangyu Sun, Ru Huang - *Peking Univ.*
Yiran Chen, Hai Li - *Duke Univ.*

8B.4 HitM: High-Throughput ReRAM-based PIM for Multi-Modal Neural Networks
Bing Li - *Capital Normal Univ.*
Ying Wang - *Chinese Academy of Sciences*
Yiran Chen - *Duke Univ.*

8C - Safety and Security Validation

Time: 9:30am - 10:00am

Moderator:

Abhijit Chatterjee - *Georgia Institute of Technology*

Automated validation of safety and security properties in modern processor designs is a challenging problem. The first presentation explores a unified hardware and firmware security property co-validation framework in the presence of adversarial behavior. The second presentation is on proving the safety properties of hardware and software using word-level as opposed to bit-level reasoning. The third presentation examines simulation-based functional verification, allowing the selection of inputs that permit a uniform selection of execution traces for verification coverage. The final presentation is on test generation for exposing embedded hardware Trojans in digital logic using delay-based side-channel analysis.

***8C.1 HyperFuzzing for SoC Security Validation**
Sujit Kumar Muduli, **Gourav Takhar**, Pramod Subramanyan - *Indian Institute of Technology Kanpur*

8C.2 Word Level Property Directed Reachability
Hari Govind V K - *Univ. of Waterloo*
Grigory Fedyukovich - *Florida State Univ.*
Arie Gurfinkel - *Univ. of Waterloo*

8C.3 On Uniformly Sampling Traces of a Transition System
Supratik Chakraborty - *Indian Institute of Technology Bombay*
Aditya A. Shrotri, Moshe Y. Vardi - *Rice Univ.*

8C.4 Test Generation using Reinforcement Learning for Delay-based Side Channel Analysis
Zhixin Pan, Jennifer Sheldon, Prabhat Mishra - *Univ. of Florida*

Special Session 8D - Taking Open-Source EDA to the Next Level: From Research to Production IC Design

Time: 9:30am - 10:00am

Moderator:

Andrew B. Kahng - *Univ. of California, San Diego*

Organizers:

Andrew Kahng - *Univ. of California, San Diego*
Tom Spyrou - *Univ. of California, Sand Diego and Precision Innovations, Inc.*

Two years have passed since the launch of the DARPA Electronics Resurgence Initiative (ERI) brought renewed attention to open-source EDA and hardware development. During this past summer (2020), many ERI-supported open-source projects have made their v1.0 releases. This session examines the next stage of the "life cycle" for open-source EDA in the digital RTL-to-GDS space: moving from the research context to production IC design. Diverse speakers and perspectives collectively highlight how "it takes a village" for open-source EDA to make real-world impact.

The session presents four distinct perspectives. (1) The first talk presents the experience of a commercial design service provider in building a production SOC tapeout methodology and flow based on open-source EDA. (2) The second talk presents the experience of "internal design advisors" who have functioned as the bridge between research tool code development and usability for production IC design. (3) The third talk examines essential aspects of, and the outlook for, open design and research enablement (PDKs, libraries, IPs, incentivization) that goes beyond open-source EDA itself. (4) The fourth talk presents the experience (engagement framework, logistics, incentives, academic rewards) and perspective of students who have contributed to an open-source EDA tool and flow development project from non-U.S. locations.

8D.1 Building OpenLANE: A 130nm OpenROAD-based Tapeout-Proven Flow
Mohamed Kassem, Tim Edwards - *eFabless.com*
Mohamed Shalan - *eFabless.com & American Univ. of Cairo*

8D.2 Bridging Academic Open-Source EDA to Real-World Usability
Austin Rovinski, Tutu Ajayi - *Univ. of Michigan*
Minsoo Kim - *Univ. of California, San Diego*
Guanru Wang, **Mehdi Saligane** - *Univ. of Michigan*

8D.3 The Missing Pieces of Open Design Enablement: A Recent History of Google Efforts
Tim Ansell - *Google*
Mehdi Saligane - *Univ. of Michigan*

8D.4 Contributions to OpenROAD from Abroad: Experiences and Learnings
Mateus Fogaca, Eder Monteiro - *UFRGS*
Marcelo Danigno - *FURG*
Isadora Oliveira, Paulo Butzen - *UFRGS & Federal Univ. of Rio Grande do Sul*
Ricardo Reis - *UFRGS*

WEDNESDAY SCHEDULE

6:30 - 7:00am

9A: Novel Frameworks for HLS and Accelerator Design and Optimization

9B: Neural Network Assisted Modeling of Analog Circuits

9C: Approximate Yet Dependable

Special Session 9D: The Future of Heterogeneous Integration and In-Memory Computing: Research Highlights of ERI Programs from US and Taiwan

7:00 - 8:00am

KEYNOTE: EDA for More-Moore and More-than-Moore Designs: Challenges and Opportunities

Yao-Wen Chang - National Taiwan Univ..

8:00 - 8:30am

10A: Advances in Boolean Reasoning, Representation and Optimization

10B: Methods and Applications of Analog Circuit Placement and Simulation

10C: EDA for Quantum Computing

Special Session 10D: Machine Learning and Hardware Security: Challenges and Opportunities

8:30 - 9:00am

11A: Modern and Domain Specific Placement

11B: Efficiency Improvement for Timing, Power Grid and Circuit Analysis

11C: EDA for Emerging Technologies based Computing Systems

Special Sessionl 11D: Robust Quantum Computers: Challenges, Solutions and Future Directions

9:00 - 9:30am

12A: Extreme Automation in Standard Cell Synthesis and ECO Optimization

12B: Deep Learning and Back-end Design

Special Session 12C: Towards Real-time Energy-efficient Mobile Robotics: From Algorithm to Hardware

Embedded Tutorial 12D: GPU Acceleration in CAD: Opportunities and Challenges

9A - Novel Frameworks for HLS and Accelerator Design and Optimization

Time: 6:30am - 7:00am

Moderator:

Hari Cherupalli - *Univ. of Minnesota*

This session covers new EDA techniques for design and optimization including NoC and AxC. The first paper proposes NASCaps, a new hardware-aware neural architecture search framework that uses a multi-objective genetic algorithm to search for an optimal architecture on both traditional deep neural networks and networks with specialized capsule layers and dynamic routing. The second paper presents an early detection methodology, ReconfAST, to identify computationally similar synthesizable kernels that are used to build shared accelerators. The third paper proposes a CAD tool to improve high-level synthesis based on the Roofline model. The fourth paper presents the application of design space exploration for hardware accelerators by taking advantage of approximate modules.

9A.1 NASCaps: A Framework for Neural Architecture Search to Optimize the Accuracy and Hardware Efficiency of Convolutional Capsule Networks
Alberto Marchisio - *Technische Univ. Wien*
Andrea Massa - *Politecnico di Torino*
Vojtech Mrazek - *Brno Univ. of Technology*
Beatrice Bussolino, Maurizio Martina - *Politecnico di Torino*
Muhammad Shafique - *New York Univ. Abu Dhabi*

9A.2 Early-stage Automated Accelerator Identification Tool for Embedded Systems with Limited Area
Parnian Mokri, Mark Hempstead - *Tufts Univ.*

9A.3 A CAD-based methodology to optimize HLS code via the Roofline model
Marco Siracusa - *Politecnico di Milano*
Marco Rabozzi - *Huxelerate SRL*
Emanuele Del Sozzo - *Politecnico di Milano*
Lorenzo Di Tucci - *Huxelerate SRL*
Samuel Williams - *Lawrence Berkeley National Lab*
Marco D. Santambrogio - *Politecnico di Milano*

9A.4 AxHLS: Design Space Exploration and High-Level Synthesis of Approximate Accelerators using Approximate Functional Units and Analytical Models
Jorge Castro-Godínez - *Karlsruhe Institute of Technology & Instituto Tecnológico de Costa Rica*
Julian Mateus-Vargas - *Instituto Tecnológico de Costa Rica*
Muhammad Shafique - *New York Univ. Abu Dhabi & New York Univ. Abu Dhabi*
Joerg Henkel - *Karlsruhe Institute of Technology*

9B - Neural Network Assisted Modeling of Analog Circuits

Time: 6:30am - 7:00am

Moderator:

Karthik Aadithya - *Sandia National Laboratories*

The session presents three papers on novel applications of neural networks to analog circuit modeling. The first paper addresses the early performance assertion of analog circuits using a convolutional neural network-based scheme. The second paper applies transfer learning and Bayesian optimization to enable efficient sampling for performance modeling of analog-mixed-signal circuits. The third paper adopts a graph neural network formulation to identify symmetry constraints for the layout of analog circuits.

9B.1 CEPA: CNN-based Early Performance Assertion Scheme for Analog and Mixed-Signal Circuit Simulation

Qiaochu Zhang, Shiyu Su, Juzheng Liu, Mike Shuo-Wei Chen - *Univ. of Southern California*

9B.2 Transfer Learning with Bayesian Optimization-Aided Sampling for Efficient AMS Circuit Modeling

Juzheng Liu, Mohsen Hassanpourghadi, Qiaochu Zhang, Shiyu Su, Mike Shuo-Wei Chen - *Univ. of Southern California*

9B.3 A general approach for identifying hierarchical symmetry constraints for analog circuit layout

Kishor Kunal, Jitesh Poojary, Tonmoy Dhar, Meghna Madhusudan, Ramesh Harjani - *Univ. of Minnesota*

Sachin S. Sapatnekar - *Univ. of Minnesota, Twin Cities*

9C - Approximate Yet Dependable

Time: 6:30am - 7:00am

Moderator:

Jie Gu - *Northwestern Univ.*

This session presents a collection of works focusing on various aspects of approximate and stochastic computing, ranging from the design of approximate hardware to mathematical foundations to number representations and error modeling. The first paper extends the state-of-the-art approximate functional unit design to reconfigurable modules. The second paper combines the logic function analysis with gate-level circuit optimization. The third paper leverages a new encoding technique to create low cost and high-performance approximate multipliers. The final paper presents practical models for designers to perform high precision accuracy analysis during the design cycle of stochastic logic.

***9C.1 Optimally Approximated and Unbiased Floating-Point Multiplier with Runtime Configurability**
Chuangtao Chen, Sen Yang - *Zhejiang Univ.*
Weikang Qian - *Shanghai Jiao Tong Univ.*
Mohsen Imani - *Univ. of California, Irvine*
Xunzhao Yin, Cheng Zhuo - *Zhejiang Univ.*

9C.2 Exploring Target Function Approximation for Stochastic Circuit Minimization
Chen Wang, Weihua Xiao - *Shanghai Jiao Tong Univ.*
John P. Hayes - *Univ. of Michigan*
Weikang Qian - *Shanghai Jiao Tong Univ.*

9C.3 Hybrid Binary-Unary Truncated Multiplication for DSP Applications on FPGAs
S. Rasoul Faraji, Kia Bazargan - *Univ. of Minnesota, Twin Cities*

9C.4 Bayesian Accuracy Analysis of Stochastic Circuits
Timothy J. Baker, John P. Hayes - *Univ. of Michigan*

Special Session 9D - The Future of Heterogeneous Integration and In-Memory Computing: Research Highlights of ERI Programs from US and Taiwan

Time: 6:30am - 7:00am

Moderator:

Tsung-Yi Ho - *National Tsing Hua Univ.*

Organizer:

Tsung-Yi Ho - *National Tsing Hua Univ.*

This special session is targeted towards Univ. researchers/professors, Ph.D. students, industry professionals, and computing system designers. This session will attract newcomers who want to learn about technologies and EDA challenges associated with heterogeneous integration and in-memory computing, as well as experienced researchers looking for exciting new directions in advanced packaging, monolithic 3D ICs, and memory-centric AI edge applications. This special session will also highlight cutting-edge research and future roadmap for both Electronics Resurgence Initiative (ERI) programs from US and Taiwan.

9D.1 Intelligent Design Automation for 2.5/3D Heterogeneous SoC Integration
Iris Hui-Ru Jiang, Yao-Wen Chang, Jiun-Lang Huang, Chung-Ping Chen - *National Taiwan Univ.*

9D.2 RTL-to-GDS Design Tools for Monolithic 3D ICs
Jinwoo Kim, Gauthaman Murali, Pruek Vanna-iampikul, Edward Lee, Daehyun Kim - *Georgia Institute of Technology*
Arjun Chaudhuri, Sanmitra Banerjee, Krishnendu Chakrabarty - *Duke Univ.*
Saibal Mukhopadhyay, **Sung-Kyu Lim** - *Georgia Institute of Technology*

9D.3 On EDA Solutions for Reconfigurable Memory-Centric AI Edge Applications
Hung-Ming Chen, Chia-Lin Hu, Kang-Yu Chang - *National Chiao Tung Univ.*
Alexandra Küster - *National Chiao Tung Univ. & RWTH Aachen Univ.*
Yu-Hsien Lin, Po-Shen Kuo, Wei-Tung Chao, Bo-Cheng Lai, Chien-Nan Liu, Shyh-Jye Jou - *National Chiao Tung Univ.*

9D.4 Fundamental Limits on the Precision of In-memory Architectures
Sujan K. Gonugondla, Charbel Sakr, Hassan R. Dbouk, **Naresh R. Shanbhag** - *Univ. of Illinois at Urbana-Champaign*

EDA for More-Moore and More-than-Moore Designs: Challenges and Opportunities

Time: 7:00am - 8:00am

Speaker:

Yao-Wen Chang - *National Taiwan Univ.*

As the process technology approaches the physics limit, the semiconductor industry faces severe manufacturing and design challenges. Though at a slower pace than ever before, on the one hand, Moore's Law continues to push the limits of process lithography into the deep nanometer regime for better area, performance, and power. On the other hand, More-than-Moore technologies add diverse devices and adopt 2.5D/3D heterogeneous integration to achieve better system-level power-performance-cost tradeoffs and higher design functionality. In this talk, we investigate most expected More-Moore patterning, interconnect, and transistor technologies and More-than-Moore system-level heterogeneous integration, address their implications and challenges for advanced circuit and system implementations, highlight current EDA solutions, and suggest future research opportunities for these emerging challenges from the perspectives of technology, heterogeneity, scalability, and multi-objective requirements.

Biography: Yao-Wen Chang received the B.S. degree from National Taiwan Univ. (NTU) in 1988, and the M.S. and Ph.D. degrees from the Univ. of Texas at Austin in 1993 and 1996, respectively, all in computer science. He is currently Distinguished Professor and the Dean of the College of Electrical Engineering and Computer Science, NTU. His current research interests lie in electronic design automation (EDA), with emphasis on physical design and manufacturability. He has co-authored one textbook on EDA and another book on routing and over 320 ACM/IEEE conference/journal papers, including highly cited papers on floorplanning, placement, routing, manufacturability, and FPGA design. His NTUplace3 placer was transferred as the popular Custom Digital Placer of SpringSoft, acquired by the #1 EDA vendor, Synopsys, for US $400 million in 2012. His NTUplace4 is a 3-time champion from the DAC'12, ICCAD'13, and ISPD'15 placement contests, then the core engine of the MaxPlace placer, a leading placer of the Maxeda Technology co-founded by Dr. Chang in 2015. Dr. Chang received four awards at the 50th DAC in 2013 for the 1st Most Papers in DAC's Fifth Decade (34 papers; #1 worldwide), etc. He is a winner of 21 top-3 place awards at ACM/IEEE EDA contests, 10 best paper awards (including DAC'17), and 23 best paper nominations from DAC (5 times), ICCAD (5 times), etc. He has received many research/teaching awards, such as the Distinguished Research Award from the Ministry of Science and Technology of Taiwan (three times, the limit), the IBM Faculty Awards (three times), and the MXIC Chair Professorship and two distinguished (highest honor) and nine excellent teaching awards from NTU.

Dr. Chang is an IEEE Fellow and currently the President of the IEEE CEDA. He has served on the editorial boards of IEEE TCAD, IEEE TVLSI, IEEE D&T, etc. He has also served as program/general chairs of ICCAD, program/general/steering committee chairs of ISPD, and program chairs of ASP-DAC and FPT. He has also served as an independent board director of Genesys Logic, a technical consultant of Faraday, MediaTek, and RealTek, and chair of the EDA Consortium of the MOE, Taiwan.

10A - Advances in Boolean Reasoning, Representation and Optimization

Time: 8:00am - 8:30am

Moderator:

Heinz Riener - *École Polytechnique Fédérale de Lausanne*

This session introduces the latest progress in Boolean methods, encompassing sampling, optimization, representation and mapping problems. The first paper describes a method to construct uniform and compact sampling circuits for a given Boolean space. The second paper proposes a multi-stage, multi-armed bandit framework for Boolean optimization. The third paper presents minimization strategies for Bi-Kronecker Functional Decision Diagrams. The last paper extends the concept of priority cuts to map dual-output LUTs.

10A.1 Symbolic Uniform Sampling with XOR Circuits

Yen-Ting Lin, **Jie-Hong Roland Jiang** - *National Taiwan Univ.*
Victor Kravets - *IBM Research*

10A.2 FlowTune: Practical Multi-armed Bandits in Boolean Optimization

Cunxi Yu - *Univ. of Utah*

10A.3 Dynamic Minimization of Bi-Kronecker Functional Decision Diagrams

Xuanxiang Huang - *Jinan Univ. & ANITI, Univ. of Toulouse*
Haipeng Che, Liangda Fang - *Jinan Univ. & Guilin Univ. of Electronic Technology*
Qingliang Chen, Quanlong Guan, Yuhui Deng - *Jinan Univ.*
Kaile Su - *Griffith Univ.*

10A.4 Dual-Output LUT Merging during FPGA Technology Mapping

Feng Wang, Liren Zhu, Jiaxi Zhang - *Peking Univ.*
Lei Li, Yang Zhang - *Huawei Technologies Co., Ltd.*
Guojie Luo - *Peking Univ.*

10B - Methods and Applications of Analog Circuit Placement and Simulation

Time: 8:00am - 8:30am

Moderator:

Eric Keiter - *Sandia National Laboratories*

The session presents four papers on the methods and applications of analog circuit placement and simulation. The first paper addresses an analytic placement utilizing signal flow information to improve the circuit performance. The second paper targets the placement of an adiabatic quantum-flux-parametron that claims to enjoy very low energy consumption and high-speed execution. The third paper adopts a graph neural network model to guide the simulated annealing placement process. The fourth paper presents a novel approach for simulating circuits with in-memory computing modules.

10B.1 Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow
Keren Zhu, Hao Chen, Mingjie Liu, Xiyuan Tang, Nan Sun, David Z. Pan - *Univ. of Texas at Austin*

10B.2 ASAP: An Analytical Strategy for AQFP Placement
Yi-Chen Chang - *National Tsing Hua Univ.*
Hongjia Li - *Northeastern Univ.*
Olivia Chen - *Yokohama National Univ.*
Yanzhi Wang - *Northeastern Univ.*
Nobuyuki Yoshikawa - *Yokohama National Univ.*
Tsung-Yi Ho - *National Tsing Hua Univ.*

10B.3 A Customized Graph Neural Network Model for Guiding Analog IC Placement
Yaguang Li, Yishuang Lin - *Texas A&M Univ.*
Meghna Madhusudan, Arvind Sharma - *Univ. of Minnesota*
Wenbin Xu - *Texas A&M Univ.*
Sachin S. Sapatnekar, Ramesh Harjani - *Univ. of Minnesota*
Jiang Hu - *Texas A&M Univ.*

10B.4 CCCS: Customized SPICE-level Crossbar-array Circuit Simulator for In-Memory Computing
Fan Zhang - *Arizona State Univ.*
Miao Hu - *Binghamton Univ.*

10C - EDA for Quantum Computing

Time: 8:00am - 8:30am

Moderator:

Daniel Große - *Johannes Kepler Univ. Linz*

Quantum computing is gaining interest and EDA needs to be ready for that. This session proposes recent advancements in this regard. The first two papers cover an important step in the compilation process of quantum algorithms, which aims to map an original quantum circuit onto a real architecture. Afterwards, a classification scheme for IBM quantum computers is proposed and, finally, how to efficiently simulate decoherence errors in quantum circuits is discussed.

10C.1 Optimal Layout Synthesis for Quantum Computing
Bochen Tan, Jason Cong - *Univ. of California, Los Angeles*

10C.2 A Monte Carlo Tree Search Framework for Quantum Circuit Transformation
Xiangzhen Zhou, Yuan Feng, Sanjiang Li - *Univ. of Technology Sydney*

***10C.3 DISQ: A Novel Quantum Output State Classification Method on IBM Quantum Computers using OpenPulse**
Tirthak Patel, Devesh Tiwari - *Northeastern Univ.*

10C.4 Considering Decoherence Errors in the Simulation of Quantum Circuits Using Decision Diagrams
Thomas Grurl, Jürgen Fuß - *Univ. of Applied Sciences Upper Austria*
Robert Wille - *Johannes Kepler Univ. Linz & Software Competence Center Hagenberg GmbH*

Special Session 10D - Machine Learning and Hardware Security: Challenges and Opportunities

Time: 8:00am - 8:30am

Moderator:

Shivam Bhasin - *Nanyang Technological Univ.*

Organizers:

Shivam Bhasin - *Nanyang Technical Univ.*
Francesco Regazzoni - *Univ. of Amstedam and ALaRI - USI*

Machine learning techniques have significantly changed our live. They helped improving several of our everyday applications, but they also have been demonstrated to be an extremely helpful tool for more advanced and complex applications. However, the implications on hardware security problems of a massive diffusion of machine learning techniques is still to be completely understood. This special session consists of 4 papers and addresses hardware security issues related with the use of machine learning and threats that classical attacks to hardware can cause to machine learning implementations. The topic is timely, and of interest of the attendees of ICCAD. Machine learning implementations are pervading every aspect of our lives, and their diffusion in IoT devices and Cyber-physical systems expose them to classical hardware security threats such as side channel attacks. Recent results demonstrated the feasibility of the approach. For instance, a recent attack demonstrated that a generic and practical reverse engineering of neural networks on embedded microcontrollers is indeed possible and these threat needs to be addressed in a proper way with dedicated countermeasures. On the other side, machine learning can be used also as a powerful tool to improve the resistance of hardware security or to improve the effectiveness of the attacks. It is thus of crucial importance that designers of future IoT devices and Cyber-physical systems, are aware of the most important security challenges caused by the massive use of machine learning techniques, which needs to be addressed a correct and effective way.

10D.1 Physically Unclonable Functions Extracted from Embedded Neural Networks
Ihab Alshaer - *Univ. Grenoble Alpes & TIMA Lab, CNRS/Grenoble INP/UJF*
Amir Ali Pour - *Grenoble INP*
David Hely - *Grenoble-INP*
Vincent Beroulle - *Grenoble INP*
Elena Ioana Vatajelu - *Univ. Grenoble Alps*
Giorgio Di Natale - *univ-grenoble-alpes*

10D.2 Breaking Side-Channel Countermeasures Through Deep Learning
Furkan Aydin, Priyank Kashyap, Seetal Potluri, Paul Franzon, **Aydin Aysu** - *North Carolina State Univ.*

10D.3 Model Extraction Attack on Practical BNN Hardware using EM Side-Channel Information
Ville Yli-Mayry, Akira Ito, Rei Ueno - *Tohoku Univ.*
Dirmanto Jap - *Temasek Laboratories, NTU*
Shivam Bhasin - *Temasek Laboratories, NTU Singapore*
Naofumi Homma - *Tohoku Univ.*

10D.4 Protections Against Physical Attacks on Machine Learning Hardware
Ilia Polian - *Univ. of Stuttgart*
Francesco Regazzoni - *Univ. of Amsterdam and ALaRI - USI*

11A - Modern and Domain Specific Placement

Time: 8:30am - 9:00am

Moderator:

Laleh Behjat - *Univ. of Calgary*

The placement process is an essential step in the physical design flow as the circuit performance, area and power consumption are highly dependent on the quality of the solution provided by the placement process. With shrinking size of transistors in modern technology processes, the placement problem has become ever more challenging due to a variety of intricate constraints and different design paradigms, such as asynchronous circuits. To address the arisen challenges, innovative approaches incorporating Machine Learning (ML)-based techniques and state-of-the-art analytic placement frameworks seem to be inevitable.

This session consists of 4 papers addressing these challenges. The first paper proposes a high-performance engine fully customized to address challenges arisen from the physical mapping of neural network workloads onto the largest commercial deep learning accelerator. The second paper presents a multi-electrostatic-based placement framework accounting for fence regions. The third paper proposes a deep reinforcement learning-based framework for VLSI placement parameter optimization, and finally, the fourth paper develops a placement framework for asynchronous circuits.

11A.1 CU.POKer: Placing DNNs on Wafer-Scale AI Accelerator with Optimal Kernel Sizing
Bentian Jiang, Jingsong Chen, Jinwei Liu, Lixin Liu, Fangzhou Wang, Xiaopeng Zhang, Evangeline F.Y. Young - *Chinese Univ. of Hong Kong*

11A.2 DREAMPlace 3.0: Multi-Electrostatics Based Robust VLSI Placement with Region Constraints
Jiaqi Gu, Zixuan Jiang - *Univ. of Texas at Austin*
Yibo Lin - *Peking Univ.*
David Z. Pan - *Univ. of Texas at Austin*

11A.3 VLSI Placement Parameter Optimization using Deep Reinforcement Learning
Anthony D. Agnesina, Kyungwook Chang, Sung Kyu Lim - *Georgia Institute of Technology*

11A.4 Dali: A Gridded Cell Placement Flow
Yihang Yang - *Yale Univ.*
Jiayuan He - *Univ. of Texas at Austin*
Rajit Manohar - *Yale Univ.*

11B - Efficiency Improvement for Timing, Power Grid and Circuit Analysis

Time: 8:30am - 9:00am

Moderator:

Kerim Kalfala - *IBM Corp.*

The session explores different approaches to improving timing, power grid design, and circuit analysis. The first paper applies dynamic programming to optimize the power distribution network to meet timing. The second paper shows how timing analysis can be accelerated by utilizing a GPU architecture. The third paper presents a new graph spectral sparsification technique to build a better conditioner for an iterative circuit solver. The last paper presents a novel stack about a design method by incorporating linear or dynamic programming methods.

11B.1 Power Distribution Network Generation for Optimizing IR-Drop Aware Timing
Wen-Hsiang Chang - *National Chiao Tung Univ. & Realtek Semiconductor Corp.*
Li-Yi Lin - *Realtek Semiconductor Corp.*
Yu-Guang Chen - *National Central Univ.*
Mango C.-T. Chao - *National Chiao Tung Univ.*

11B.2 GPU-Accelerated Static Timing Analysis
Zizheng Guo - *Peking Univ.*
Tsung-Wei Huang - *Univ. of Utah*
Yibo Lin - *Peking Univ.*

11B.3 SF-GRASS: Solver-Free Graph Spectral Sparsification
Ying Zhang - *Stevens Institute of Technology*
Zhiqiang Zhao - *Michigan Technological Univ.*
Zhuo Feng - *Stevens Institute of Technology*

11B.4 Meshed Stack Via Design Considering Complicated Design Rules with Automatic Constraint Generation
Kai-Chuan Yang, Tao-Chun Yu, Shao-Yun Fang - *National Taiwan Univ. of Science and Technology*
Teng-Yuan Cheng, Yang-Chun Liu, Cindy Chin-Fang Shen - *Synopsys Taiwan Co., Ltd.*

11C - EDA for Emerging Technologies based Computing Systems

Time: 8:30am - 9:00am

Moderator:

Chenchen Liu - *Univ. of Maryland, Baltimore County*

Emerging technologies have dramatically revolutionized the development of computing systems, while the progress of design automation of these new systems falls behind. This session proposes the latest research outcomes in this field. The first two papers discuss the resistance mapping solutions for resistive memory processing designs. Then a framework is proposed to counter the variation and thermal effects for optical neural networks. Finally, the risk of malicious/unpredictable changes in error rates of NISQ computers is explored and addressed.

11C.1 CONTRA: Area-Constrained Technology Mapping Framework For Memristive Memory Processing Unit
Debjyoti Bhattacharjee, Anupam Chattopadhyay - *Nanyang Technological Univ.*
Srijit Dutta - *SAMSUNG*
Ronny Ronen, Shahar Kvatinsky - *Technion - Israel Institute of Technology*

11C.2 DP-MAP: Towards Resistive Dot-Product Engines with Improved Precision
Necati Uysal, Baogang Zhang - *Univ. of Central Florida*
Sumit Kumar Jha - *Univ. of Texas at San Antonio*
Rickard Ewetz - *Univ. of Central Florida*

11C.3 Countering Variations and Thermal Effects for Accurate Optical Neural Networks
Ying Zhu, Grace Li Zhang, Bing Li - *Tech. Univ. of Munich*
Xunzhao Yin, Cheng Zhuo - *Zhejiang Univ.*
Huaxi Gu - *Xidian Univ.*
Tsung-Yi Ho - *National Tsing Hua Univ.*
Ulf Schlichtmann - *Tech. Univ. of Munich*

11C.4 A Lightweight Approach to Detect Malicious/Unexpected Changes in the Error Rates of NISQ Computers
Nikita Acharya, **Samah Saeed** - *City Univ. of New York*

Special Session 11D - Robust Quantum Computers: Challenges, Solutions and Future Directions

Time: 8:30am - 9:00am

Moderator:

Moinuddin Qureshi - *Georgia Tech*

Organizers:

Swaroop Ghosh - *Pennsylvania State Univ.*
Anupam Chattopadhyay - *Nanyang Technological Univ.*
Robert Wille - *Johannes Kepler Univ. Linz*

This special session will provide an in-depth treatment of the resilience of NISQ era quantum computers. The first talk will describe the holistic design flow of a quantum accelerator. The second talk will provide an overview of the Quantum Scientific Computing Open User Testbed (QSCOUT) developed at Sandia National Labs for trapped-ion qubits. It will also describe the implementation of the multi-channel dual tone modulation and control system in a Radio-Frequency System on a Chip (RFSoC) device. The third talk will cover compilation flows for quantum algorithms with focus on the correctness analysis. The fourth talk will introduce the use of Quantum Random Access Coding (QRAC) to map discrete features of a classifier efficiently into limited number of qubits for robust Variational Quantum Circuit (VQC) to speed up the training. The final talk will present compilation techniques for quantum approximate optimization algorithm to improve error resiliency.

11D.1 Quantum Computing - How to develop a Quantum Accelerator
Koen Bertels - *Univ. of Porto & Univ. do Porto*

11D.2 Classical and Quantum Control of a Trapped Ion Quantum Computing Testbed System
Daniel Lobser, Matthew Blain, Raymond Haltli, Craig W. Hogle, Andrew J. Landahl, Benjamin C. A. Morrison, Melissa Revelle, Kenneth M. Rudinger, Antonio Russo, Brandon Ruzic, Daniel Stick, Jay Van Der Wall, Christopher G. Yale - *Sandia National Labs*
Susan Clark - *Sandia National Laboratories*

11D.3 JKQ: JKU Tools for Quantum Computing
Robert Wille - *Johannes Kepler Univ. Linz & Software Competence Center Hagenberg GmbH (SCCH)*
Stefan Hillmich, Lukas Burgholzer - *Johannes Kepler Univ. Linz*

11D.4 Efficient Discrete Feature Encoding for Variational Quantum Classifier
Rudy Raymond - *IBM Quantum, IBM Research*
Hiroshi Yano, Yudai Suzuki, Naoki Yamamoto - *Keio Univ.*

11D.5 Noise Resilient Compilation Policies for Quantum Approximate Optimization Algorithm
Mahabubul Alam, Abdullah-Ash Saki, Junde Li - *Penn State*
Anupam Chattopadhyay - *Nanyang Technological Univ.*
Swaroop Ghosh - *Pennsylvania State Univ.*

12A - Extreme Automation in Standard Cell Synthesis and ECO Optimization

Time: 9:00am - 9:30am

Moderator:

Wuxi Li - *Xilinx Inc.*

This session consists of four talks, covering the emerging challenges in advanced technology nodes: The first talk proposes a machine learning (ML) model for dynamic IR-drop prediction and guides the spreading of high current-demand cells at the ECO stage. The second talk focuses on the place-and-route problem for the synthesis of multi-bit flip-flop cells with an A*-based multi-row transistor placement and a MAX-SAT based detailed router. The third talk formulates the complimentary-FET cell synthesis into a satisfiability modulo theories (SMT) problem with a dynamic complementary pin allocation scheme for routability and pin access optimization. The fourth talk integrates convolutional neural network (CNN) models into the cell layout search algorithm for routability and timing optimization by pruning the search space.

12A.1 Dynamic IR-Drop ECO Optimization by Cell Movement with Current Waveform Staggering and Machine Learning Guidance
Xuan-Xue Huang, Hsien-Chia Chen - *National Taiwan Univ.*
Sheng-Wei Wang - *National Chiao Tung Univ.*
Iris Hui-Ru Jiang - *National Taiwan Univ.*
Yih-Chih Chou, Cheng-Hong Tsai - *Global Unichip Corp.*

12A.2 MCell: Multi-Row Cell Layout Synthesis with Resource Constrained MAX-SAT Based Detailed Routing
Yih-Lang Li, **Shih-Ting Lin** - *National Chiao Tung Univ.*
Shinichi Nishizawa - *Fukuoka Univ.*
Hidetoshi Onodera - *Kyoto Univ.*

12A.3 A Routability-Driven Complimentary-FET (CFET) Standard Cell Synthesis Framework using SMT
Chung-Kuan Cheng, **Chia-Tung Ho**, Daeyeal Lee, Dongwon Park - *Univ. of California, San Diego*

12A.4 iTPlace: Machine Learning-Based Delay-Aware Transistor Placement for Standard Cell Synthesis
Tai-Cheng Lee, Cheng-Yen Yang, Yih-Lang Li - *National Chiao Tung Univ.*

12B - Deep Learning and Back-end Design

Time: 9:00am - 9:30am

Moderator:

Mandy Pant - *Intel Corp.*

Deep learning opens the door to new approaches for many back-end design problems ranging from cell characterization, power grid design, timing and power optimization. The first paper applies neural networks for electromigration induced IR drop prediction and localized IR drop optimization. The second paper uses graph neural networks for signoff power optimization. The third paper seeks to apply machine learning methods for the design-technology co-optimization and the last paper proposes a learning-based crosstalk noise prediction to guide physical channel routing.

***12B.1 GridNet: Fast Data-Driven EM-Induced IR Drop Prediction and Localized Fixing for On-Chip Power Grid Networks**
Han Zhou, Wentian Jin, Sheldon Tan - *Univ. of California, Riverside*

12B.2 A Fast Learning-Driven Signoff Power Optimization Framework
Yi-Chen Lu - *Georgia Institute of Technology*
Siddhartha Nath - *Synopsys, Inc.*
Sai Surya Kiran Pentapati, Sung Kyu Lim - *Georgia Institute of Technology*

12B.3 Cell Library Characterization using Machine Learning for Design Technology Co-Optimization
Florian Klemme - *Karlsruhe Institute of Technology*
Yogesh Chauhan - *Indian Institute of Technology Kanpur*
Joerg Henkel - *Karlsruhe Institute of Technology*
Hussam Amrouch - *Univ. of Stuttgart & Karlsruhe Institute of Technology*

12B.4 Routing-Free Crosstalk Prediction
Rongjian Liang - *Texas A&M Univ.*
Zhiyao Xie - *Duke Univ.*
Jinwook Jung - *IBM T.J. Watson Research Center*
Vishnavi Chauha - *Texas A&M Univ.*
Yiran Chen - *Duke Univ.*
Jiang Hu - *Texas A&M Univ.*
Hua Xiang - *IBM Research*
Gi-Joon Nam - *IBM T.J. Watson Research Center*

Special Session 12C - Towards Real-time Energy-efficient Mobile Robotics: From Algorithm to Hardware

Time: 9:00am - 9:30am

Moderator:
Jiang Hu - *Texas A&M Univ.*

Organizer:
Bo Yuan - *Rutgers Univ.*

Background— A Robot is a very complex information processing system. A robot needs inception capability to sense, cognition capability to understand, and decision capability to act. From the perspective of computing, such an entire sense-understand-act pipeline is involved with various computation-intensive algorithms in many fields, including but not limited to machine learning, computer vision, control, signal processing etc.

Motivation— In the emerging cyber-physical system (CPS) era, a rapidly growing field in robotics, namely mobile robotics, has received a lot of attention because of its very widespread practical applications, such as search-and-rescue, underwater exploration, and autonomous delivery. In the scenario of mobile robotics, computational resource and energy budget are typically restricted, while the need for real-time and low-power solutions become more demanding, thereby bringing severe challenges but also exciting opportunities for the VLSI and computing community.

Although the study in efficient computing for robotics is still in its infancy, recently researchers in both academia and industry have made significant progress in addressing the above challenges. These research efforts that would be presented in this special session, range from algorithm to circuit to accelerator architecture to near-sensor computing, and they will lead to promising cross-layer solutions towards real-time energy-efficient mobile robotics.

12C.1 Efficient Computing for Low-Energy Robotics
Vivienne Sze - *MIT*

12C.2 Hardware Acceleration of Robot Scene Perception Algorithms
Yanqi Liu, Can Eren Durman - *Brown Univ.*
Giuseppe Calderoni - *Politecnico di Torino*
R. Iris Bahar - *Brown Univ.*

12C.3 DaDu Series- Fast and Efficient Robot Accelerators
Yinhe Han, Yuxin Yang, Xiaoming Chen, Shiqi Lian - *Center for Intelligent Computing Systems, Institute of Computing Technology, Chinese Academy of Science*

12C.4 TACOS: Tactile Core with Optical Strain Sensor for Robotic Smart Skin
Zheyu Liu, Jingyi Zhou, Huichan Zhao, Qi Wei, **Fei Qiao**, Xinjun Liu, Huazhong Yang - *Tsinghua Univ.*

Embedded Tutorial 12D - GPU Acceleration in CAD: Opportunities and Challenges

Time: 9:00am - 9:30am

Moderator:

Yibo Lin - *Peking Univ.*

Organizers:

Yibo Lin - *Peking Univ.*
Tsung-Wei Huang - *Univ. of Utah*

The semiconductor industry never stops seeking to reduce the design time and effort in modern integrated circuit (IC) implementation that incorporates billions of transistors. To allow more efficient design space exploration and optimization, the core CAD algorithms must incorporate new parallel paradigms.Meanwhile, GPU has become more and more powerful with new architectures like Volta and Turing, new features like NVLink and tensor cores, and new programming models like CUDA graphs. It is reported that both the number of floating point operations per second (FLOPS) and the peak memory bandwidth have been growing exponentially in the past 10 years. These advances bring new opportunities for accelerating the long and complicated CAD flow. This session highlights the new CAD frameworks, in both front-end and back-end stages, for accelerating modern VLSI design flows with hybrid CPU-GPU platforms.

12D.1 Opportunities for RTL and Gate Level Simulation using GPUs
Yanqing Zhang, Haoxing Ren, Brucek Khailany - *NVIDIA Corp.*

12D.2 Empyrean ALPS-GT: GPU-accelerated Analog Circuit Simulation
Chen Zhao, Zhenya Zhou, Dake Wu - *Empyrean Software*

12D.3 GPU Acceleration in VLSI Back-end Design: Overview and Case Studies
Yibo Lin - *Peking Univ.*

12D.4 A General-purpose Parallel and Heterogeneous Task Programming System for VLSI CAD
Tsung-Wei Huang - *Univ. of Utah*

THURSDAY SCHEDULE

8:00am - 5:00pm

Top Picks in Hardware and Embedded Security

8:00am - 12:00pm

Designing Quantized IP Models with QKeras and hls4ml

8:00am - 3:30pm

2020 ACM/IEEE International Workshop on System-Level Interconnect Problems and Pathfinding (SLIP^2)

8:15am - 4:30pm

Workshop on Hardware and Algorithms for Learning On-a-chip (HALO) 2020

8:00am - 12:00pm (Section 1)

2nd Workshop on Accelerator Computer Aided Design (ACCAD) 2020

9:00am - 1:00pm

Workshop on Open-Source EDA Technology

FRIDAY SCHEDULE

8:00am - 12:00pm (Section 2)

2nd Workshop on Accelerator Computer Aided Design (ACCAD) 2020

All speakers are denoted in bold | * denotes Best Paper Candidate | Note Agenda time zone is PST (UTC-8)

Workshop - Top Picks in Hardware and Embedded Security

Time: 8:00am - 5:00pm

Organizers:

Ramesh Karri - *New York Univ.*
Gang Qu - *Univ. of Maryland -- College Park*
Ahmad-Reza Sadeghi - *TU Darmstadt*
Jeyavijayan Rajendran - *Texas A&M Univ.*

The top picks will be selected from conference and journal papers that have appeared in leading hardware security conferences including but not limited to DAC, DATE, ICCAD, HOST, VLSI Design, CHES, ETS, VTS, ITC, IEEE S&P, Euro S&P, Usenix Security, ASIA CCS, NDSS, ISCA, HASP, MICRO, ASPLOS, HPCA, ACSAC and ACM CCS. The top picks will appear in an IEEE Design and Test (if approved) special section on "Top Picks in Hardware and Embedded Security".
https://na.eventscloud.com/website/15990/?

Steering Committee

Ramesh Karri - New York Univ.
Gang Qu - Univ. of Maryland, College Park
Ahmad-Reza Sadeghi - TU Darmstadt
Jeyavijayan Rajendran - Texas A&M Univ.

Program Chairs

Srini Devadas - MIT
Jeyavijayan Rajendran - Texas A&M Univ.

Workshop - Designing Quantized IP Models with QKeras and hls4ml

Time: 8:00am - 12:00pm

Organizer:

Claudionor Coelho - *Palo Alto Networks, Inc.*

In this hands-on workshop, we will teach the basics of quantization using QKeras and show how to create a quanized model using QKeras, and how to generate ML/DL IPs using hls4ml.

We introduce the QKeras library, an extension of the Keras library allowing for the creation of heterogeneous quantized versions of deep neural network models, through drop-in replacement of Keras layers. These are trained quantization-aware, where the user can trade-off model area or

energy consumption by accuracy. We demonstrate how the reduction of numerical precision, through quantization-aware training, significantly

reduces resource consumption while retaining high accuracy when implemented on FPGA hardware.

hls4ml library is a popular library for synthesizing ML models, supporting QKeras. It generates models based in HLS, targeted at FPGA synthesis flow.

This workshop complements the paper submission to ICCAD, giving participants hands-on experience on quantization and synthesis of ML models from industry experts in this area from Google and CERN.

Speakers:

Claudionor Coelho - *Palo Alto Networks, Inc.*
Sioni Summers - *CERN*
Vladimir Loncar - *CERN*
Jennifer Ngadiuba - *CERN*
Thea Aarrestad - *CERN*

2020 ACM/IEEE International Workshop on System-Level Interconnect Problems and Pathfinding (SLIP^2)

Time: 8:00am - 3:30pm

The 2020 ACM/IEEE International Workshop on System-Level Interconnect Problems and Pathfinding (SLIP^2) is the 22nd, rebooted edition of the System-Level Interconnect Prediction (SLIP) Workshop. SLIP^2 is co-located with ICCAD 2020. It will bring together researchers and practitioners who have a shared interest in the challenges and future of system-level interconnect, and come from wide-ranging backgrounds that span system, application, design and technology. The technical goal of the workshop is to (1) identify fundamental problems, and (2) foster new pathfinding of design, analysis, and optimization of interconnect and communication fabrics in electronic systems. Additionally, a more interactive, workshop-like tone and format - recalling earlier editions of the SLIP workshop - is a goal for SLIP^2 this year. Original submissions in the form of regular technical papers, invited sessions (tutorials, panels, special-topic sessions), workshop discussion topics, and posters are welcome. Accepted technical papers will be published in the ACM and IEEE digital libraries.

Since SLIP^2 is virtual, registration is free and included with the ICCAD registration.

For complete details visit website: http://sliponline.org/

Workshop - Workshop on Hardware and Algorithms for Learning On-a-chip (HALO) 2020

Time: 8:15am - 4:30pm

Organizers:

Qinru Qiu - *Syracuse Univ.*
Yingyan Lin - *Rice Univ.*
Chenchen Liu - *Univ. of Maryland*

In recent years, machine/deep learning algorithms has unprecedentedly improved the accuracies in practical recognition and classification tasks, some even surpassing human-level accuracy. While significant progresses have been made on accelerating the models for real-time inference on edge and mobile devices, the training of the models largely remains offline on server side. State-of-the-art learning algorithms for deep neural networks (DNN) imposes significant challenges for hardware implementations in terms of computation, memory, and communication. This is especially true for edge devices and portable hardware applications, such as smartphones, machine translation devices, and smart wearable devices, where severe constraints exist in performance, power, and area.

There is a timely need to map the latest complex learning algorithms to custom hardware, in order to achieve orders of magnitude improvement in performance, energy efficiency and compactness. Exemplary efforts from industry and academia include many application-specific hardware designs (e.g., xPU, FPGA, ASIC, etc.). Recent progress in computational neurosciences and nanoelectronic technology, such as emerging memory devices, will further help shed light on future hardware-software platforms for learning on-a-chip. At the same time new learning algorithms need to be developed to fully explore the potential of the hardware architecture.

The overarching goal of this workshop is to explore the potential of on-chip machine learning, to reveal emerging algorithms and design needs, and to promote novel applications for learning. It aims to establish a forum to discuss the current practices, as well as future research needs in the aforementioned fields. For complete details visit website: https://iccad-halo.github.io/?

Speakers:

Mike Davies - *Intel Corp.*
Nathan McDonald - *Air Force Research Lab*
Hai (Helen) Li - *Duke Univ.*
Travis Dewolf - *Applied Brian Research*
Deming Chen - *Univ. of Illinois at Urbana-Champaign*
Yiyu Shi - *Univ. of Notre Dame*
Yanzhi Wang - *Northeastern Univ.*
Eriko Nurvitadhi - *Intel Corp.*
Priya Panda - *Yale Univ.*

Workshop - 2nd Workshop on Accelerator Computer Aided Design (ACCAD) 2020

Section One: Thursday, November 5: 8:00am - 12:00pm

Section Two: Friday, November 6: 8:00am - 12:00pm

Organizers:

Abe Elfadel - *Khalifa Univ.*
Subhasish Mitra - *Stanford Univ.*

This workshop provides a forum to present and discuss the current trends in computer-aided design in support of domain-specific accelerator chips, especially for artificial intelligence and machine learning applications. The workshop will be concerned with the VLSI methodology flow from high-level synthesis to physical verification and performance prediction, particularly in the way it gets impacted with the emerging design paradigms of domain-specific instruction sets, approximate computing, in-memory computing, and stochastic computing. Of particular interest to the workshop are the transformations that VLSI CAD has to undergo to adapt to the post-CMOS technologies when they are considered in the context of accelerator design. The workshop will include, but will not be limited to, the following topics:

- High-level synthesis of machine-learning accelerators
- Design space exploration of domain-specific accelerators
- Tools and methodologies for in-memory computing
- Tools and methodologies for approximate computing
- CAD for emerging accelerator technologies: ReRAM, MRAM, Photonics, etc.
- Tools and methodologies for the post-CNN era
- Tools and methodologies for the testing and verification of accelerator chips.

Each year, the workshop will be devoted to three focus areas of accelerator CAD. Renowned speakers are invited to speak on each of the three areas. The remainder of the workshop will be open to the larger community on the basis of a call-for-posters. Short oral presentations will be given by all the accepted poster presenters in advance of the poster session.

The four topics selected for this year are:

1. CAD for emerging accelerator technologies
2. High-level synthesis of machine-learning accelerators
3. Accelerator verification
4. Hardware/software co-acceleration

For complete details visit website: https://sites.google.com/masdar.ac.ae/accad2020/home.

Workshop - Workshop on Open-Source EDA Technology

Time: 9:00am - 1:00pm

Organizer:

Jose Renau - *Alibaba DAMO Academy*
Matthew Guthaus - *Univ. of California, Santa Cruz*

This one-day workshop aims to galvanize the open-source EDA movement. The workshop will bring together EDA researchers who are committed to open-source principles to share their experiences and coordinate efforts towards developing a reliable, fully open-source EDA flow. The workshop will feature presentations and posters for existing and under-development open-source tools. The workshop will include a panel to brainstorm about potential gaps and obstacles to open-source EDA, and how to coordinate efforts and ensure quality and interoperability across open-source tools. A cash award will be given to the Best Tool Award.

The 2020 WOSET papers are available at WOSET 2020

https://woset-workshop.github.io/WOSET2020.html

Video presentations will be added roughly October 25, 2020.

The Q&A schedule will be posted soon.

https://woset-workshop.github.io/

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