IEEE/ACM

2019 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

ICCAD

38th Edition

CONFERENCE PROGRAM

NOVEMBER 4 – 7, 2019

The Westin Wesminster, Westminster, Colorado

ICCAD.COM

IEEE CAS CEDA ACM Association for Computing Machinery sigda | In cooperation with: IEEE Electron Devices Society

WELCOME TO THE 38TH ICCAD

FROM DAVID PAN

ICCAD GENERAL CHAIR

Welcome to the 38th International Conference on Computer-Aided Design! For the first time, ICCAD is being held in the Denver area. As ICCAD has been moving around from its birthplace in Silicon Valley, to Silicon Hills (Austin), to Southern California, and this year to Rocky Mountains, we hope you enjoy these different locations, get to know local related industry, and of course the ICCAD conference itself. Jointly sponsored by IEEE and ACM, ICCAD has been the premier forum to explore emerging technology challenges in electronic design automation, present leading-edge R&D solutions, and identify future research directions. The ICCAD scope has also been adapted and expanded to address emerging technology, design, and automation challenges including those in AI, IoT, security, among others.

This is yet another strong year for ICCAD in terms of regular paper submissions. The total 394 final submissions were organized into 14 tracks and reviewed by 135 outstanding TPC members from both academia and industry around the world. Our rigorous double-blind review process culminated with a full-day in-person meeting in June, where 94 regular papers were accepted and formed into 28 regular sessions. This marks a competitive 23.9% acceptance rate. We also had a high number of special session and tutorial proposals submitted to ICCAD. In the end, 11 special sessions and 1 embedded tutorial were formed on topics that complement the regular sessions.

We are delighted to host several distinguished keynote speakers: the Monday morning keynote on "Beyond CMOS Technologies for Computing: Prospects and Best Bets" will be given by Dr. Ian Young, Intel Senior Fellow. On Wednesday morning, Dr. Wolfram Burgard, VP for Automated Driving Technology at the Toyota Research Institute, will present the keynote on "Probabilistic and Machine Learning Approaches for Autonomous Robots and Automated Driving". On Tuesday, IEEE CEDA will host its annual ICCAD Luncheon Distinguished Lecture. We hope you find these keynotes informative and inspiring.

On Thursday, we have seven stimulating workshops on a variety of trending topics, including: Hands-on Workshop on Machine Learning, Deep Learning and Reinforcement Learning for EDA Developers; 3rd International Workshop on Quantum Compilation; Top Picks in Hardware and Embedded Security; Second Workshop on Open-Source EDA Technology (WOSET); International Workshop on Design Automation for Analog and Mixed-Signal Circuits; and 1st Workshop on Accelerator Computer-Aided Design. They all have exciting programs themselves, so we hope that many of you will take advantage of them and stay an extra day.

Following its long tradition, ICCAD continues to be the home to strong student-oriented activities: the SIGDA CADathlon, the ACM Student Research Competition, and the ICCAD CAD Contests. In addition, on Wednesday night, for the first time, ICCAD will host a "Career & Diversity" event where recruiters from industry will share their views on what companies are looking for and young graduates who recently joined industry will share their experiences and tips, and why diversity is important at work.

Once again ICCAD promises to be an ultimate destination for those working on the cutting-edge EDA research. We do hope you will be able to join us. Finally, we are grateful to our ICCAD 2019 sponsors, supporters, and volunteers for making this year's conference another great success.

Enjoy ICCAD and Rocky Mountains!

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Registration Hours & Location

Location: Terrazza Foyer

Monday, November 4	*7:00am – 6:00pm*
Tuesday, November 5	*7:30am – 6:00pm*
Wednesday, November 6	*7:30am – 6:00pm*
Thursday, November 7	*7:00am – 4:00pm*

ICCAD 2019 Mobile App

Review the program, save sessions to your personalized conference schedule, read speakers abstracts, and connect with other attendees using the ICCAD 2019 mobile app provided by Whova, available for download today. Download Whova and search for **ICCAD 2019**.

Proceedings

ICCAD Conference Papers will be delivered electronically online via a username and password.
To access: http://proceedings.iccad.com
Badge ID = Registration ID (on your badge)
Your Email = Email address
Please refer to your registration receipt to access the files you are eligible to view.

For Speakers & Presenters

SPEAKERS' BREAKFAST

Please attend the day of your presentation!

Location: Legacy Ballroom

Monday, November 4	*7:30 - 8:15am*
Tuesday, November 5	*7:30 - 8:15am*
Wednesday, November 6	*7:30 - 8:15am*

NEED PRACTICE?

An AV Practice Room will be available in Sage Board Room, set up with a computer, LCD projector, and screen for you to practice/view your slides before your session.

Location: Sage Board Room

Monday, November 4	*7:00am - 6:00pm*
Tuesday, November 5	*7:00am - 6:00pm*
Wednesday, November 6	*7:00am - 6:00pm*

ICCAD Social Media

Connect with ICCAD through Twitter @ICCAD.

Stay Connected during the Conference

ICCAD 2019 is offering internet access in the meeting rooms for attendees.

The Wi-Fi connection is Westin Westminster, user name: iccad2019 password: iccad2019.

Conference Management

Our mission is to facilitate networking, education and marketing with efficiency and precision in order to maximize customer experiences, and client profitability and recognition. We accomplish this by having a committed staff of trade show production organizers with the training, technology tools, processes and experience to offer the best service in the industry.

Visit **mpassociates.com** for more information.

BEST PAPER CANDIDATES

IEEE/ACM William J. McCalla ICCAD Best Paper Award Candidates

MONDAY, NOVEMBER 4

1B.1* Power Grid Fixing for Electromigration-Induced Voltage Failures
Zahi Moudallal - *Univ. of Toronto*
Valeriy Sukharev - *Mentor, A Siemens Business*
Farid N. Najm - *Univ. of Toronto*

TUESDAY, NOVEMBER 5

4A.1* How to Efficiently Handle Complex Values? Implementing Decision Diagrams for Quantum Computing
Stefan Hillmich - *Johannes Kepler Univ. Linz*
Alwin Zulehner - *Johannes Kepler Univ. Linz*
Robert Wille - *Johannes Kepler Univ. Linz*

4B.1* Analyzing and Modeling In-Storage Computing Workloads On EISC — An FPGA-Based System-Level Emulation Platform
Zhenyuan Ruan - *Univ. of California, Los Angeles*
Tong He - *Univ. of California, Los Angeles*
Jason Cong - *Univ. of California, Los Angeles*

6B.4* GenUnlock: An Automated Genetic Algorithm Framework for Unlocking Logic Encryption
Huili Chen - *Univ. of California, San Diego*
Cheng Fu - *Univ. of California, San Diego*
Jishen Zhao - *Univ. of California, San Diego*
Farinaz Koushanfar - *Univ. of California, San Diego*

WEDNESDAY, NOVEMBER 6

9A.3* Security and Complexity Analysis of LUT-based Obfuscation: From Blueprint to Reality
Gaurav Kolhe - *Univ. of California, Davis*
Hadi Mardani Kamali - *George Mason Univ.*
Miklesh Naicker - *San Francisco State Univ.*
Tyler David Sheaves - *San Francisco State Univ.*
Hamid Mahmoodi - *San Francisco State Univ.*
Sai Manoj Pudukotai Dinakarrao - *George Mason Univ.*
Houman Homayoun - *Univ. of California, Davis*
Setareh Rafatirad - *George Mason Univ.*
Avesta Sasan - *George Mason Univ.*

10B.3* NanoTherm: An Analytical Fourier-Boltzmann Framework for Full Chip Thermal Simulations
Smruti R. Sarangi - *Indian Institute of Technology Delhi*
Shashank Varshney - *Indian Institute of Technology Delhi*
Hameedah Sultan - *Indian Institute of Technology Delhi*
Palkesh Jain - *Qualcomm Technologies, Inc.*

BEST PAPER AWARD COMMITTEES

IEEE/ACM William J. McCalla ICCAD Best Paper Award Selection Committee

Joerg Henkel (Chair) - *Karlsruhe Institute of Technology*
Yier Jin - *Univ. of Florida*
Frank Liu - *IBM, Corp.*
Partha Pande - *Univ. of Washington*
Chia-Lin Yang - *National Taiwan Univ.*

Ten-Year Retrospective Most Influential Paper Award Selection Committee

Robert Wille (Chair) - *Univ. of Linz.*
Niraj K. Jha - *Princeton Univ.*
Hai (Helen) Li - *Duke Univ.*
Sachin Sapatnekar - *Univ. of Minnesota*
Pingqiang Zhou- *ShanghaiTech Univ.*

TUTORIAL/SPECIAL SESSION COMMITTEE

Tulika Mitra (Chair) - *National Univ. of Singapore*
Deming Chen - *Univ. of Illinois at Urbana-Champaign*
Siddharth Garg - *New York Univ.*
Tony Givargis - *Univ. of California, Irvine*
Iris Hui-Ru Jiang - *National Taiwan Univ.*
Hai (Helen) Li - *Duke Univ.*
Yu Wang - *Tsinghua Univ.*
Robert Willie - *Univ. Linz*

ACM SIGDA CADathlon 2019 at ICCAD

Sunday, November 3

Time: 8:00am - 5:00pm | Room: Cotton Creek

In the spirit of the long-running ACM programming contest, the CADathlon is a challenging, all-day, programming competition focusing on practical problems at the forefront of Computer-Aided Design, and Electronic Design Automation in particular. The contest emphasizes the knowledge of algorithmic techniques for CAD applications, problem-solving and programming skills, as well as teamwork.

As the "Olympic games of EDA," the contest brings together the best and the brightest of the next generation of CAD professionals. It gives academia and the industry a unique perspective on challenging problems and rising stars, and it also helps attract top graduate students to the EDA field.

The contest is open to two-person teams of graduate students specializing in CAD and currently full-time enrolled in a Ph.D. granting institution in any country. Students are selected based on their academic backgrounds and their relevant EDA programming experiences. Travel grants are provided to qualifying students. The CADathlon competition consists of six problems in the following areas:

(1) Circuit design and analysis
(2) Physical design and design for manufacturability
(3) Logic and high-level synthesis
(4) System design and analysis
(5) Verification and testing
(6) Future technologies (Bio-EDA, Security, AI, etc.)

More specific information about the problems and relevant research papers will be released on the Internet one week prior to the competition. The writers and judges that construct and review the problems are experts in EDA from both academia and industry. At the contest, students will be given the problem statements and example test data, but they will not have the judges' test data. Solutions will be judged on correctness and efficiency. Where appropriate, partial credit might be given. The team that earns the highest score is declared the winner. In addition to handsome trophies, the first and second place teams will receive cash award.

Contest winners will be announced at the ICCAD Opening Session on Monday morning and celebrated at the ACM/SIGDA Dinner and Member Meeting.

The CADathlon competition is sponsored by ACM/SIGDA and several Computer and EDA companies. For detailed contest information and sample problems from last year's competition, please visit the ACM/SIGDA website at: https://www.sigda.org/sigda-events/cadathlon/

For all inquiries, please send emails to: cadathlon@gmail.com

ORGANIZING COMMITTEE:

Chair: Tsung-Wei Huang, *Univ. of Utah, UT, USA*
Vice Chair: Yu-Guang Chen, *National Central Univ., Taiwan*
Vice Chair: Pei-Yu Lee, *Maxeda Technology, Taiwan*

Sponsored by: cadence ACADEMIC NETWORK SIGDA

MONDAY SCHEDULE

8:30 - 9:00am
Opening Session & Awards

Location: Westminster IV

9:00 - 10:00am
Keynote: Beyond CMOS Technologies for Computing: Prospects and Best Bets

Ian A. Young - Intel Corp. | Location: Westminster IV

10:00 - 10:30am
Coffee Break

Location: Westminster Foyer

10:30am - 12:30pm
Session 1A: Random Ski: PUF and Random Number Generators

Location: Westminster IV

Session 1B: New Perspectives of Timing, Power and IR Drops

Location: Westminster I

Session 1C: Optimization Attacks Routing Challenges

Location: Westminster II

Special Session 1D: Design Automation and DNN for FPGAs

Location: Westminster III

11:30am - 1:30pm
ACM Student Research Competition Poster Session

Location: Westminster Foyer

12:30 - 1:30pm
Lunch

Location: Legacy Ballroom

MONDAY SCHEDULE

1:45 - 3:45pm

Session 2A: Accelerating Neural Networks
Location: Westminster IV

Session 2B: Emerging Applications in Synthesis
Location: Westminster I

Session 2C: Approximation in Behavioral Specifications, Neural Network Design, and Stochastic Computing
Location: Westminster II

Special Session 2D: 2019 CAD Contest at ICCAD
Location: Westminster III

3:45 - 4:15pm

Coffee Break
Location: Westminster Foyer

4:15 - 5:45pm

Session 3A: Processing in Memory and Secure Memory Design
Location: Westminster IV

Session 3B: Efficient and Reliable Design
Location: Westminster I

Session 3C: Emerging Technologies for Computing and Networks
Location: Westminster II

Special Session 3D: Design Automation for Power Electronics
Location: Westminster III

5:45 - 6:15pm

AI / Machine Learning at Cadence
Location: Westminster I

Sponsored by: cadence ACADEMIC NETWORK

6:00 - 10:00

Second Working Group Meeting on Logic Locking and Anti-Trojan Solutions
Location: Westminster II & Westminster III

6:15 - 6:45pm

Networking Reception
Location: Westminster Foyer

Sponsored by: cadence ACADEMIC NETWORK

6:45 - 8:15pm

ACM Student Research Competition Technical Presentations
Location: Westminster I

Sponsored by: STUDENT RESEARCH COMPETITION, Association for Computing Machinery, Microsoft

Opening Session and Awards

Time: 8:30am - 9:00am | Room: Westminster IV

Start off the conference with opening remarks from the ICCAD Executive Committee members and hear the highlights of the conference. The IEEE/ACM William J. McCalla ICCAD Best Paper award will be announced along with other award presentations from IEEE CEDA and ACM. .

IEEE/ACM WILLIAM J. MCCALLA ICCAD BEST PAPER AWARD

This award is given in memory of William J. McCalla for his contributions to ICCAD and his CAD technical work throughout his career.

Front-End Award:

4B.1 Analyzing and Modeling In-Storage Computing Workloads On EISC — An FPGA-Based System-Level Emulation Platform

Zhenyuan Ruan - *Univ. of California, Los Angeles*
Tong He - *Univ. of California, Los Angeles*
Jason Cong - *Univ. of California, Los Angeles*

Back-End Award:

1B.1 Power Grid Fixing for Electromigration-Induced Voltage Failures

Zahi Moudallal - *Univ. of Toronto*
Valeriy Sukharev - *Mentor, A Siemens Business*
Farid N. Najm - *Univ. of Toronto*

TEN YEAR RETROSPECTIVE MOST INFLUENTIAL PAPER AWARD

This award is being given to the paper judged to be the most influential on research and industrial practice in computer-aided design over the ten years since its original appearance at ICCAD.

2009 Paper Titled: Nonvolatile Memristor Memory: Device Characteristics and Design Implications

Yenpo Ho, Garng M. Huang, Peng Li; *Texas A&M Univ.*
ICCAD 2009, pp. 485-490

IEEE FELLOW

Farinaz Koushanfar, *Univ. of California, San Diego*
For contributions to hardware and embedded systems security and to privacy-preserving computing.

IEEE CEDA OUTSTANDING SERVICE RECOGNITION

Iris Bahar - *Brown Univ.*
For outstanding service to the EDA community as ICCAD General Chair in 2018.

IEEE CEDA ERNEST S. KUH EARLY CAREER AWARD

Pierre-Emmanuel Gaillardon - *Univ. of Utah*
For contributions to Electronic Design Automation targeting emerging logic and memory technologies.

ACM/SIGDA CADATHALON

Introduction of the 2019 winners.

Keynote: Beyond CMOS Technologies for Computing: Prospects and Best Bets

Time: 9:00 - 10:00am | Location: Westminster IV

Speaker:
Ian A. Young - *Senior Fellow and Director of Exploratory Integrated Circuits, Components Research, Technology and Manufacturing Group, Intel Corporation, Hillsboro, Oregon*

CMOS integrated circuit technology for computation is at an inflexion point. Although this is the technology which has enabled the semiconductor industry to make vast progress over the past 30-plus years, it is expected to see challenges going beyond the ten year horizon, particularly from an energy efficiency point of view. Thus it is extremely important for the semiconductor industry to discover a new integrated circuit technology which can carry us to the beyond CMOS era, so that the power-performance of computing can continue to improve. Currently, researchers are exploring novel device concepts and new information tokens as an alternative for CMOS technology. Examples of areas being actively researched are; quantum electronic devices, such as the tunneling field-effect transistor (TFET), and devices based on electron spin and nano-magnetics (spintronics). It is clear that choices will need to be made in the next 10 years to identify viable energy efficient alternatives to augment CMOS for computation. To prioritize and guide the research exploration in materials, devices and circuits, benchmarking methodology and metrics are being used.

In this talk research in quantum materials for beyond CMOS devices (nanoelectronic and/or nanomagnetic) is presented. Some device proposals and demonstrations are reviewed and the trends in this field are identified. Considerations guiding development of competitive computing technologies are described. Results of beyond-CMOS circuit benchmarking are reviewed.

Biography: Ian Young is a Senior Fellow and director of Exploratory Integrated Circuits in the Technology and Manufacturing Group of Intel Corporation. He joined Intel in 1983 and his technical contributions have been in the design of DRAMs, SRAMs, microprocessor circuit design, Phase Locked Loops and microprocessor clocking, mixed-signal circuits for microprocessor high speed I/O links, RF CMOS circuits for wireless transceivers, and research for chip to chip optical I/O. He has also contributed to the definition and development of Intel's process technologies. He now leads a research group exploring the future options for the integrated circuit in the beyond CMOS era. Ian Young received the Bachelor of Electrical Engineering and the Master Eng. Science, from the Univ. of Melbourne, Australia. He received the PhD in Electrical Engineering from the Univ. of California, Berkeley. He is the recipient of the 2009 International Solid-State Circuits Conference's Jack Raper Award for Outstanding Technology Directions paper. He received the 2018 IEEE Frederik Philips Award "for leadership in research and development on circuits and processes for the evolution of microprocessors". Ian Young is a Fellow of the IEEE.

Coffee Break

Time: 10:00am - 10:30am | Room: Westminster Foyer

Session 1A - Random Ski: PUF and Random Number Generators

Time: 10:30am - 12:30pm | Room: Westminster IV

Moderator:

Weize Yu - *Old Dominion Univ.*

PUFs and random number generators are fundamental building blocks for many hardware and system security techniques. However, there are many practical challenges in ensuring their performance, reliability, and security. This session is comprised of three papers addressing these challenges. The first paper develops a new two-layer PUF composition to defend against modeling attacks. The second paper proposes and implements an all-digital TRNG design based on a chaotic cellular automata topology. The third paper presents a quantum random number generator resilient against side channel attacks.

1A.1 An All-Digital True Random Number Generator Based on Chaotic Cellular Automata Topology
Scott Best - *Rambus Inc.*
Xiaolin Xu - *Univ. of Illinois at Chicago*

1A.2 SCR-QRNG: Side-Channel Resistant Design using Quantum Random Number Generator
Jungmin Park - *Univ. of Florida*
Seongjoon Cho, Taejin Lim - *EYL Partners*
Swarup Bhunia, Mark Tehranipoor - *Univ. of Florida*

1A.3 Strengthening PUFs using Composition
Zhuanhao Wu, Hiren Patel, Manoj Sachdev, Mahesh Tripunitara - *Univ. of Waterloo*

Session 1B - New Perspectives of Timing, Power and IR Drops

Time: 10:30am - 12:30pm | Room: Westminster I

Moderator:

Tsung-Wei Huang - *Univ. of Utah*

This session covers the state-of-the-art advances in timing, power, and IR drop analysis. It focuses on the power grid optimization for electromigration, machine-learning based IR drop estimation, advanced wake-up delay minimization, and new clock gating techniques.

***1B.1 Power Grid Fixing for Electromigration-Induced Voltage Failures**
Zahi Moudallal - *Univ. of Toronto*
Valeriy Sukharev - *Mentor, A Siemens Business*
Farid N. Najm - *Univ. of Toronto*

1B.2 "IncPIRD": Fast Learning-Based Prediction of Incremental IR Drop
Chia-Tung Ho, Andrew Kahng - *Univ. of California, San Diego*

1B.3 Allocation of State Retention Registers Boosting Practical Applicability to Power Gated Circuits
Gyounghwan Hyun, Taewhan Kim - *Seoul National Univ.*

1B.4 Flip-Flop State Driven Clock Gating: Concept, Design, and Methodology
Gyounghwan Hyun, Taewhan Kim - *Seoul National Univ.*

Session 1C - Optimization Attacks Routing Challenges

Time: 10:30am - 12:30pm | Room: Westminster II

Moderator:

Bei Yu - *Chinese Univ. of Hong Kong.*

Optimization is needed in all areas. This session introduces new optimization methods in Clock Network Synthesis, inter- and intra-chip routing, and FPGAs. The first paper discusses machine learning based optimization for clock tree synthesis. The next paper presents linear programming and graph based global inter-chip routing. The third paper proposes interconnect optimization method while considering key designs constraints. Finally, the last paper is on using Lagrangian relaxation based time division multiplexing optimization for multi-FPGA systems.

1C.1 GAN-CTS: A Generative Adversarial Framework for Clock Tree Prediction and Optimization
Yi-Chen Lu, Jeehyun Lee, Anthony Agnesina - *Georgia Institute of Technology*
Kambiz Samadi - *Qualcomm Technologies, Inc.*
Sung Kyu Lim - *Georgia Institute of Technology*

1C.2 Obstacle-Aware Group-Based Length-Matching Routing for Pre-Assignment Area-I/O Flip-Chip Designs
Yu-Hsuan Chang, **Hsiang-Ting Wen**, Yao-Wen Chang - *National Taiwan Univ.*

1C.3 Global Interconnect Optimization
Siad Daboul, Stephan Held - *Univ. of Bonn*
Bento Natura - *London School of Economics and Political Science*
Daniel Rotter - *Univ. of Bonn*

1C.4 Lagrangian Relaxation-Based Time-Division Multiplexing Optimization for Multi-FPGA Systems
Chak-Wa Pui, Evangeline Young - *Chinese Univ. of Hong Kong*

Special Session 1D - Design Automation and DNN for FPGAs

Time: 10:30am - 12:30pm | Room: Westminster III

Organizer:

Wei Zhang - *Hong Kong Univ. of Science and Technology*
Yun Liang - *Peking Univ.*

Field-Programmable Gate Arrays (FPGAs) are increasingly used as hardware accelerators to implement various tasks due to their advantages of low power and massive parallelism. However, conventional manual implementation of RTL codes on FPGAs requires deep comprehension of the hardware architecture and great efforts. In order to lower the programming barrier and improve the design efficiency, it is crucial to develop the high-level design automation framework for the FPGA based design, such as high-level synthesis, automatic design optimization framework, etc. However, it also brings new challenges to the mapping flow and tool support for the FPGA implementation. At the same time, the machine learning workloads, especially the deep neural networks (DNNs) are increasingly deployed on FPGA for acceleration, where DNN's deeper network and diverse branch structures pose great challenges for an efficient FPGA implementation.

This session presents six talks and addresses the above challenges from different perspectives. On one hand, it highlights new approaches for the automatic code generation, and synthesis flows for the efficient mapping of high-level designs on FPGA. On the other hand, it presents several DNN accelerator designs on FPGA with novel design optimization techniques.

1D.1 Zac : Towards Automatic Optimization and Deployment of Quantized Deep Neural Networks on Embedded Devices
Qingcheng Xiao, **Yun Liang** - *Peking Univ.*

1D.2 Energy-Driven Dataflow Optimization for DNN on FPGA
Qi Sun, Tinghuan Chen - *Chinese Univ. of Hong Kong*
Jin Miao - *Cadence Design System, Inc.*
Bei Yu - *Chinese Univ. of Hong Kong*

1D.3 Towards In-Circuit Tuning of Deep Learning Designs
Zhiqiang Que, Daniel Holanda Noronha, Ruizhe Zhao, Steven J.E. Wilton, **Wayne Luk** - *Imperial College*

1D.4 NAIS: Neural Architecture and Implementation Search and its Applications in Autonomous Driving
Cong Hao - *Univ. of Illinois at Urbana-Champaign*
Yao Chen - *Advanced Digital Sciences Center*
Deming Chen - *Univ. of Illinois at Urbana-Champaign*
Atif Sarwari, Daryl Sew - *XMotors.ai*
Ashutosh Dhar - *Univ. of Illinois at Urbana-Champaign*
Dongdong Fu - *XMotors.ai*
Jinjun Xiong - *IBM Corp.*
Wen-mei Hwu - *Univ. of Illinois at Urbana-Champaign*
Junli Gu - *XMotors.ai*

1D.5 What You Simulate Is What You Synthesize: Designing a Processor Core from C++ Specifications
Simon Rokicki, Joseph Paturel - *Univ Rennes, Inria*
Davide Pala, **Olivier Sentieys** - *Univ. of Rennes 1*

1D.6 Hi-ClockFlow: Multi-Clock Dataflow Automation and Throughput Optimization in High-Level Synthesis
Tingyuan Liang, Jieru Zhao, Liang Feng - *Hong Kong Univ. of Science and Technology*
Sharad Sinha - *Indian Institute of Technology, Goa*
Wei Zhang - *Hong Kong Univ. of Science and Technology*

All speakers are denoted in bold | * denotes Best Paper Candidate

Additional Meeting - ACM Student Research Competition Poster Session

Time: 11:30am - 1:30pm | Room: Westminster Foyer

Sponsored by Microsoft Research, the ACM Student Research Competition is an internationally recognized venue enabling undergraduate and graduate students who are ACM members to:

- Experience the research world — for many undergraduates this is a first!
- Share research results and exchange ideas with other students, judges, and conference attendees
- Rub shoulders with academic and industry luminaries
- Understand the practical applications of their research
- Perfect their communication skills
- Receive prizes and gain recognition from ACM and the greater computing community.

The ACM Special Interest Group on Design Automation (ACM SIGDA) is organizing such an event in conjunction with the International Conference on Computer Aided Design (ICCAD). Authors of accepted submissions will get travel grants up to $500 from ACM/Microsoft and ICCAD registration fee support from SIGDA. The event consists of several rounds, as described at http://src.acm.org/ and http://www.acm.org/student-research-competition, where you can also find more details on student eligibility and timeline.

Sponsored by: STUDENT RESEARCH COMPETITION · Association for Computing Machinery · Microsoft

Lunch

Time: 12:30pm - 1:30pm | Room: Legacy Ballroom

Join fellow attendees for lunch in Legacy Ballroom.

Session 2A - Accelerating Neural Networks

Time: 1:45pm - 3:45pm | Room: Westminster IV

Moderator:

Hai Helen Li - *Duke Univ.*

This session includes four papers on designing neural network accelerators. The first paper proposes a modular DNN accelerator generator with configurable dataflow and an NN-to-architecture mapper to generate energy-efficient designs. The second paper presents an accelerator for the instance normalization layer in generative neural networks. The third paper designs a CNN accelerator framework that can reduce off-chip memory accesses for super-resolution tasks with large feature maps. The last paper develops an FPGA-based accelerator for auto-regressive convolutional neural networks to accelerate audio synthesis.

2A.1 **MAGNet: A Modular Accelerator Generator for Neural Networks**
Rangharajan Venkatesan, Yakun Sophia Shao - *NVIDIA Corp.*
Miaorong Wang - *Massachusetts Institute of Technology*
Jason Clemons, Steve Dai, Matthew Fojtik, Ben Keller, Alicia Klinefelter, Nathaniel Pinckney - *NVIDIA Corp.*
Priyanka Raina - *Stanford Univ.*
Yanqing Zhang, Brian Zimmer, William J. Dally, Joel Emer, Stephen W. Keckler, Brucek Khailany - *NVIDIA Corp.*

2A.2 **ACG-Engine: An Inference Accelerator for Content Generative Neural Networks**
Haobo Xu - *Institute of Computing Technology, Chinese Academy of Sciences*
Ying Wang, Yujie Wang, Jiajun Li, Bosheng Liu, Yinhe Han - *Institute of Computing Technology, Chinese Academy of Sciences*

2A.3 **eSRCNN: A Framework for Optimizing Super-Resolution Tasks on Diverse Embedded CNN Accelerators**
Youngbeom Jung, Yeongjae Choi, Jaehyeong Sim, Lee-Sup Kim - *Korea Advanced Institute of Science and Technology*

2A.4 **FastWave: Accelerating Autoregressive Convolutional Neural Networks on FPGA**
Shehzeen S. Hussain, Mojan Javaheripi, Paarth Neekhara, Ryan Kastner, Farinaz Koushanfar - *Univ. of California, San Diego*

Session 2B - Emerging Applications in Synthesis

Time: 1:45pm - 3:45pm | Room: Westminster I

Moderator:

Alexandre Levisse - *Swiss Federal Institute of Technology*

This session shows new, emerging, applications in synthesis. The first paper presents a path balancing mapping algorithm for superconducting electronics. The second paper builds a generic synthesis framework using a large set of memristor-based Boolean operators. The third paper studies the conditions for a set of threshold functions to be realized with a common weight vector, enabling a higher compression ratio for libraries of threshold functions.

2B.1 A Dynamic Programming-Based, Path Balancing Technology Mapping Algorithm Targeting Area Minimization
Ghasem Pasandi, Massoud Pedram - *Univ. of Southern California*

2B.2 A General Logic Synthesis Framework for Memristor-Based Logic Design
Zhenhua Zhu, Mingyuan Ma, Jialong Liu - *Tsinghua Univ.*
Liying Xu - *Peking Univ.*
Xiaoming Chen - *Chinese Academy of Sciences*
Yuchao Yang - *Peking Univ.*
Yu Wang, Huazhong Yang - *Tsinghua Univ.*

2B.3 Searching Parallel Separating Hyperplanes for Effective Compression of Threshold Logic Networks
Siang-Yun Lee, Nian-Ze Lee, Jie-Hong Roland Jiang - *National Taiwan Univ.*

Session 2C - Approximation in Behavioral Specifications, Neural Network Design, and Stochastic Computing

Time: 1:45pm - 3:45pm | Room: Westminster II

Moderator:

Hai Zhou - *Northwestern Univ.*

Approximation as a means for optimizing power, energy, and security in systems is addressed in the papers in this session. The first paper introduces the notion of approximation within the high-level synthesis flow. The second paper proposes a method for incremental training of neural networks using approximate multipliers. The third paper presents a technique for design space exploration for approximate neural networks without expensive retraining. Finally, the last paper of the session introduces a method for leveraging randomness in designing secure stochastic systems.

2C.1 Approximating Behavioral HW Accelerators Through Selective Partial Extractions Onto Synthesizable Predictive Models
Siyuan Xu, Benjamin Carrion Schaefer - *Univ. of Texas at Dallas*

2C.2 INA: Incremental Network Approximation Method for Limited Precision Deep Neural Networks
Zheyu Liu, Kaige Jia - *Tsinghua Univ.*
Weiqiang Liu - *Nanjing Univ. of Aeronautics and Astronautics*
Qi Wei, Fei Qiao, Huazhong Yang - *Tsinghua Univ.*

2C.3 ALWANN: Automatic Layer-Wise Approximation of Deep Neural Network Accelerators without Retraining
Vojtech Mrazek, Zdenek Vasicek, Lukas Sekanina - *Brno Univ. of Technology*
Muhammad Abdullah Hanif, Muhammad Shafique - *Vienna Univ. of Technology*

2C.4 Exploiting Randomness in Stochastic Computing
Paishun Ting, **John Hayes** - *Univ. of Michigan*

Special Session 2D - 2019 CAD Contest at ICCAD

Time: 1:45pm - 3:45pm | Room: Westminster III

Moderator:

Mark Po-Hung Lin - *National Chiao Tung Univ.*

Organizers:

Ulf Schlichtmann - *Tech. Univ. of Munich*
Sabya Das - *Synopsys, Inc.*
Ing-Chao Lin - *National Cheng Kung Univ.*
Mark Po-Hung Lin - *National Chiao Tung Univ.*

The CAD Contest at ICCAD (https://iccad-contest.org/) is a challenging, multi-month, research & development competition, focusing on advanced, real-world problems in the field of Electronic Design Automation (EDA). Contestants can participate in one or more problems provided by EDA/IC industry. The winners will be awarded at an ICCAD special session dedicated to this contest. Since 2012, the CAD Contest at ICCAD has been attracting more than a hundred teams per year, fostering productive industry-academia collaborations, and leading to hundreds of publications in top-tier conferences and journals. The contest keeps enhancing its impact and boosts EDA research.

This session will give an overview of the CAD Contest at ICCAD, present the three contest problems of 2019 CAD Contest to the EDA community, announce the contest results, and introduce a verified robust academic design flow from logic synthesis to physical design. The session will contain five presentations: The contest chair will first give a brief introduction to the contest. Afterwards, three topic chairs will introduce each of the contest problems and benchmark suites, announce the contest results, and present awards to the winners. The topic chairs will also play some video clips provided by Top-X teams which present key ideas and algorithms of their solutions to the contest problems. Finally, the Design Automation Technical Committee (DATC) of IEEE CEDA will introduce a reference design flow in academia.

2D.1 Overview of 2019 CAD contest at ICCAD
Ulf Schlichtmann - *Tech. Univ. of Munich*
Sabya Das - *Synopsys, Inc.*
Ing-Chao Lin - *National Cheng Kung Univ.*
Mark Po-Hung Lin - *National Chiao Tung Univ.*

2D.2 2019 CAD Contest: Logic Regression on High Dimensional Boolean Space
Ching-Yi Huang, Chi-An (Rocky) Wu, Tung-Yuan Lee, Chih-Jen (Jacky) Hsu, Kei-Yong Khoo - *Cadence Design Systems, Inc.*

2D.3 2019 CAD Contest: System-Level FPGA Routing with Timing Division Multiplexing Technique
Yu-Hsuan Su - *Synopsys Taiwan Co., Ltd.*
Richard Sun, Pei-Hsin Ho - *Synopsys, Inc.*

2D.4 ICCAD 2019 LEF/DEF Based Global Routing Contest
Alexander Volkov, Sergei Dolgov - *Mentor, A Siemens Business*
Lutong Wang, **Bangqi Xu** - *Univ. of California, San Diego*

2D.5 DATC RDF-2019: Towards a Complete Academic Reference Design Flow
Jianli Chen - *Fuzhou Univ.*
Iris Hui-Ru Jiang - *National Taiwan Univ.*
Jinwook Jung - *IBM T. J. Watson Research Center*
Andrew B. Kahng - *Univ. of California, San Diego*
Victor N. Kravets - *IBM T. J. Watson Research Center*
Yih-Lang Li, Shih-Ting Lin - *National Chiao Tung Univ.*
Mingyu Woo - *Univ. of California, San Diego*

All speakers are denoted in bold | * denotes Best Paper Candidate

Coffee Break

Time: 3:45pm - 4:15pm | Room: Westminster Foyer

Session 3A - Processing in Memory and Secure Memory Design

Time: 4:15pm - 5:45pm | Room: Westminster IV

Moderator:

Deliang Fan - *Univ. of Central Florida*

This session is devoted to the computing and security applications of memory devices. The first paper focuses on a novel design for bit-wise data processing in dynamic random memory (DRAM) that exploits a hybrid sense-amp design to extend the range of functions that can be executed in one clock cycle in memory. The second paper proposes a neuromorphic inference accelerator based on resistive switching memories that can efficiently run models with variable weight precision. The last paper in the session proposes a novel way to sanitize flash memories without the need for explicit erase cycles or encryption, thus leading to reduced overhead and improved endurance.

3A.1 ReDRAM: A Reconfigurable Processing-in-DRAM Platform for Accelerating Bulk Bit-Wise Operations
Shaahin Angizi, **Deliang Fan** - *Univ. of Central Florida*

3A.2 An Agile Precision-Tunable CNN Accelerator Based on ReRAM
Yintao He, Ying Wang, Yongchen Wang, Huawei Li, Xiaowei Li - *Chinese Academy of Sciences*

3A.3 Toward Instantaneous Sanitization through Disturbance-Induced Errors and Recycling Programming Over 3D Flash Memory
Wei-Chen Wang - *Macronix International Co., Ltd. & National Taiwan Univ.*
Ping-Hsien Lin, **Yung-Chun Li** - *Macronix International Co., Ltd.*
Chien-Chung Ho - *National Chung Cheng Univ.*
Yu-Ming Chang - *National Taiwan Univ.*
Yuan-Hao Chang - *Academia Sinica*

Session 3B - Efficient and Reliable Design

Time: 4:15pm - 5:45pm | Room: Westminster I

Moderator:

Sebastian Huhn - *Univ. of Bremen*

In modern implementation technologies, across all design components and circuit families, variation, aging, and other analog and design-time uncertain properties increasingly affect our ability to quickly design reliable logic and memory circuits. This session presents papers covering efficient design methodologies for evaluating the impact of continuous variations on discrete architectural values, improving the reliability of PCM memories, and optimizing the layout of analog circuits.

3B.1 Efficient Uncertainty Modeling for System Design via Mixed Integer Programming
Zichang He, Weilong Cui, Chunfeng Cui, Timothy Sherwood, Zheng Zhang - *Univ. of California, Santa Barbara*

3B.2 BagNet: Berkeley Analog Generator with Layout Optimizer Boosted with Deep Neural Networks
Kourosh Hakhamaneshi, Nick Werblun, Pieter Abbeel, Vladimir Stojanović - *Univ. of California, Berkeley*

3B.3 Flipcy: Efficient Pattern Redistribution for Enhancing MLC PCM Reliability and Storage Density
Muhammad Imran, Taehyun Kwon - *Sungkyunkwan Univ. & Samsung Electronics Co., Ltd.*
Jung Min You, Joon-Sung Yang - *Sungkyunkwan Univ.*

Session 3C - Emerging Technologies for Computing and Networks

Time: 4:15pm - 5:45pm | Room: Westminster II

Moderator:

Yanzhi Wang - *Northeastern Univ.*

This session focuses on emerging concepts and technologies for multi-level memories, microfluidic bio-chips, and hybrid NoCs. The first paper considers extending the endurance of multi-layer PCMs by reducing the number of RESET steps. The second paper aims to bridge the gap between the system-level and physical layout design in micro-chips by introducing a simulation-based approach for synthesizing channel-level pressurization protocols. The third paper introduces an energy-delay optimization for the laser source of optic-electronic hybrid NoCs via task-mapping source gating. Together, these novel directions show energy consumption reductions as well as design and hardware speed-ups for next-generation compute systems.

3C.1 Endurance Enhancement of Multi-Level Cell Phase Change Memory
Cheongwon Lee, Youngsoo Song, **Youngsoo Shin** - *Korea Advanced Institute of Science and Technology*

3C.2 VOM: Flow-Path Validation and Control-Sequence Optimization for Multilayered Continuous-Flow Microfluidic Biochips
Mengchu Li, Tsun-Ming Tseng, Yanlu Ma - *Technische Univ. München*
Tsung-Yi Ho - *National Tsing Hua Univ.*
Ulf Schlichtmann - *Technische Univ. München*

3C.3 Task Mapping-Assisted Laser Power Scaling for Optical Network-on-Chips
Yuyang Wang - *Univ. of California, Santa Barbara*
Kwang-Ting Cheng - *Hong Kong Univ. of Science and Technology*

Special Session 3D - Design Automation for Power Electronics

Time: 4:15pm - 5:45pm | Room: Westminster III

Moderator:
Jose Ayala - *Complutense Univ.*

Organizers:
Miroslav Vasic - *Univ. Politecnica de Madrid*
Jose Ayala - *Complutense Univ.*

Design Automation has become of strategic importance for the Power Electronics Society as modern highly integrated designs are dealing with multi-physics problems, shorter design time and multivariable optimization to obtain higher efficiencies and better power density. Additionally, the development and employment of Wide Bandgap devices (GaN and SiC based) has opened a set of design problems that has not been seen with Si based technology. All these trends are driving the need to revisit design tools and capabilities.

The purpose of this special session is to understand the problems of Design Automation in Power Electronics and identify methodologies that have been used so far by academia and industry. The focus of the special session is to bring together the experts in both Power Electronics and Design Automation and have them presenting their perspectives on the emerging needs.

The expected results are:

- A clear identification of the common ground and synergy between Power Electronics and Design Automation
- An understanding where the limits of the current technology and tools are in Design Automation for Power Electronics

3D.1 **Design Automation for Power Electronics**
Alan Mantooth - *Univ. of Arkansas*

3D.2 **Towards the Limits of GaN Power Electronics**
Elison Matioli - *Ecole Polytechnique Fédérale de Lausanne (EPFL)*

3D.3 **Ultra-High Fidelity Real-Time Simulation for Power Electronics and Microgrids:Empowering Test Driven Control Development**
Ivan Celanovic - *Typhoon HIL*

Additional Meeting - AI / Machine Learning at Cadence

Time: 5:45pm - 6:15pm | Room: Westminster I

Machine Learning though not a new idea is currently one of the most hot topics in computer science. Cadence as a company which has lot of experience with computational tasks is heavily adopting Machine Learning for various aspects of EDA design methodology. In the presentation areas will be shown, where Cadence is already using Machine Learning and ethe "inside" and "outside" usage of ML in Cadence design flow will be explained. Cadence as IP provider is providing design and processor IP, which are targeted on creation of ML-assisted systems in the cloud and on the edge. The different requirements for the IP, which is targeted at different use scenarios will be explained in the presentation.

Biography: Anton Klotz, studied Technical Computer Science at Mannheim Univ. in Germany and joined Cadence Design Systems in 2004 as Application Engineer, where he was responsible for physical verification and DFM for large digital designs. In 2015 he became Univ. Program Manager for the EMEA region. He is running Cadence Academic Network, which is the interface to all academia-related topics at Cadence, such as academic licenses, academic conference, internship program and government-funded research projects"

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Additional Meeting - Second Working Group Meeting on Logic Locking and Anti-Trojan Solutions

Time: 6:00pm - 10:00pm | Room: Westminster II & Westminster III

Organizers:

Swarup Bhunia - *Univ. of Florida*
Yier Jin - *Univ. of Florida*
J. V. Rajendran - *Texas A&M Univ.*

It will be the second of the two Working Group Meetings on Logic Locking and Anti-Trojan Solutions, sponsored by DARPA. The goal of this meeting is to bring together members from academia, industry and government to discuss current challenges and needs in obfuscation and Trojan countermeasures; identify promising research directions in these areas; and suggest appropriate actions for the DoD enterprise. The first workshop was successfully held on June 5, 2019, co-located with Design Automation Conference (DAC).

Networking Reception

Time: 6:15pm - 6:45pm | Room: Westminster Foyer

Whatever your goal, networking receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day's presentations with the conference presenters. All attendees are invited.

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Additional Meeting - ACM Student Research Competition Technical Presentations

Time: 6:45pm - 8:15pm | Room: Westminster I

The ACM Student Research Competition allows both graduate and undergraduate students to discuss their research with student peers, as well as academic and industry researchers, in an informal setting, while enabling them to attend ICCAD.

This session is the final round of ACM SRC at ICCAD 2019. Each student will present for 10 minutes, followed by a 2-minute question and answer period. This session will be attended by the evaluators and any interested conference attendees. The top three winners in each category will be chosen based on these presentations. The undergraduate and graduate finalists will be eligible to compete in the ACM SRC Grand Finals to be held in June 2020.

More details can be found at:

https://www.sigda.org/sigda-events/src/

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TUESDAY SCHEDULE

8:30 - 10:00am

Session 4A: Quantum Computing

Location: Westminster IV

Session 4B: FPGA Emulation and Optimization

Location: Westminster I

Special Session 4C: Placement for Heterogeneity

Location: Westminster II

Special Session 4D: Advanced Logic Locking Techniques for Hardware IP Protection

Location: Westminster III

10:00 - 10:30am

Coffee Break

Location: Westminster Foyer

Sponsored by: HUAWEI

10:30am - 12:00pm

Session 5A: System-Level Attacks and Protection

Location: Westminster IV

Session 5B: Pushing the Frontiers of Synthesis

Location: Westminster I

Session 5C: Advanced Design Techniques for Manufacturability

Location: Westminster II

Embedded Tutorial 5D: When Neural Networks Meet Hardware: The Princess, The Knight, and the Very Bad Dragon

Location: Westminster III

12:00 - 12:30pm

Lunch

Location: Legacy Ballroom

12:30 - 1:30pm

Current Progress in Quantum Computing

Paul Nation - IBM T.J. Watson Research Center | Location: Legacy Ballroom

Sponsored by: IEEE CEDA

TUESDAY SCHEDULE

1:45 - 3:45pm

Session 6A: Algorithmic Innovations for Neural Computing

Location: Westminster IV

Session 6B: Verified and Efficient Embedded Security

Location: Westminster I

Session 6C: Overcoming the Complexity of System Level Validation

Location: Westminster II

Special Session 6D: Quantum Computing - Resilience and Security

Location: Westminster III

3:45 - 4:15pm

Coffee Break

Location: Westminster Foyer

Sponsored by: HUAWEI

4:15 - 6:15pm

Special Session 7A: The Road to Safe Autonomy: Neural Networks Meet Formal Reasoning

Location: Westminster IV

Session 7B: Accelerator Design and Modeling

Location: Westminster I

Session 7C: Combating Circuit Aging and Device Variability

Location: Westminster II

Special Session 7D: Breaking the Ice Between Silicon Photonics Design and EDA: Electronic-Photonic Design Automation

Location: Westminster III

6:15 - 6:45pm

Networking Reception

Location: Westminster Foyer

Sponsored by: SYNOPSYS® Silicon to Software™

6:45 - 8:30pm

ACM/SIGDA Member Meeting

Location: Legacy Ballroom

Sponsored by: acm Association for Computing Machinery SIGDA

Session 4A - Quantum Computing

Time: 8:30am - 10:00am | Room: Westminster IV

Moderator:

Rolf Drechsler - *Univ. of Bremen*

This session presents three contributions to the emerging field of quantum computing. The first one provides an implementation of a decision diagram package with a particular focus on the efficient representation of complex values. The second paper shows how logic synthesis for XOR-AND graphs can generate quantum circuits and yield better upper bounds on resources for fault-tolerant quantum computing. The third one lifts the consideration to a higher level and provides an HDL-based synthesis approach for related reversible circuits that enables to generate components for quantum circuits without additional qubits.

***4A.1 How to Efficiently Handle Complex Values? Implementing Decision Diagrams for Quantum Computing**
Alwin Zulehner, **Stefan Hillmich**, Robert Wille - *Johannes Kepler Univ. Linz*

4A.2 The Role of Multiplicative Complexity in Compiling Low T-Count Oracle Circuits
Giulia Meuli, Mathias Soeken - *École Polytechnique Fédérale de Lausanne*
Earl Campbell - *Univ. of Sheffield*
Martin Roetteler - *Microsoft Corporation*
Giovanni De Micheli - *École Polytechnique Fédérale de Lausanne*

4A.3 Towards HDL-Based Synthesis of Reversible Circuits with No Additional Lines
Robert Wille - *Johannes Kepler Univ. Linz*
Majid Haghparast - *Islamic Azad Univ.*
Smaran Adarsh, Tanmay M - *People's Education Society Univ.*

Session 4B - FPGA Emulation and Optimization

Time: 8:30am - 10:00am | Room: Westminster I

Moderator:

Daniel Große - *Univ. of Bremen*

This session includes three impactful research explorations on FPGA emulation platforms and optimizations. The first paper presents an open-source FPGA emulation platform for in-storage computing that can provide a publicly available platform for rapid evaluation for in-storage applications. The second paper proposes a co-design approach to perform sparse matrix-vector multiplication efficiently on a CPU-FPGA heterogeneous platform. The last paper explores an automated multi-accelerator SoC generation toolchain, which can perform rapid and accurate full-system simulation of SoCs with user-specified accelerators.

***4B.1 Analyzing and Modeling In-Storage Computing Workloads On EISC — An FPGA-Based System-Level Emulation Platform**
Zhenyuan Ruan, Tong He, Jason Cong - *Univ. of California, Los Angeles*

4B.2 ReDESK: A Reconfigurable Dataflow Engine for Sparse Kernels on Heterogeneous Platforms
Kai Lu, Zhaoshi Li, Leibo Liu, Jiawei Wang, Shouyi Yin, Shaojun Wei - *Tsinghua Univ.*

4B.3 Centrifuge: Evaluating Full-System HLS-Generated Heterogenous-Accelerator SoCs using FPGA-Acceleration
Qijing Huang, Christopher Yarp, Sagar Karandikar, Nathan Pemberton, Benjamin Brock - *Univ. of California, Berkeley*
Liang Ma - *Politecnico di Torino*
Guohao Dai - *Tsinghua Univ.*
Robert Quitt, Krste Asanovic, John Wawrzynek - *Univ. of California, Berkeley*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 4C - Placement for Heterogeneity

Time: 8:30am - 10:00am | Room: Westminster II

Moderator:

Stephen Yang - *Xilinx Inc.*

In this heterogeneous world, placement is far more than just 2D geometric optimization. Issues like multi-dimensions, diverse fabrics, heterogeneous cell sizes are challenging in this long-studied area. In this session, we have three papers on placement dealing with these challenges. The first two are on FPGA and the last one is on ASIC macro placement. The first paper extends the-state-of-the-art ASIC placer ePlace to FPGA and achieves good performance. The second work is on 2.5D FPGA placement with non-linear optimization, and the last work is on ASIC macro placement with a novel simulated evolution algorithm.

4C.1 **elfPlace: Electrostatics-Based Placement for Large-Scale Heterogeneous FPGAs**
Wuxi Li, Yibo Lin, David Z. Pan - *Univ. of Texas at Austin*

4C.2 **Analytical Placement with 3D Poisson's Equation and ADMM Based Optimization for Large-Scale 2.5D Heterogeneous FPGAs**
Jianli Chen - *Fudan Univ. & Fuzhou Univ.*
Wenxing Zhu - *Fuzhou Univ.*
Jun Yu - *Fudan Univ.*
Lei He - *Univ. of California, Los Angeles*
Yao-Wen Chang - *National Taiwan Univ.*

4C.3 **A Novel Macro Placement Approach Based on Simulated Evolution Algorithm**
Jai-Ming Lin, You-Lun Deng, Ya-Chu Yang, **Jia-Jian Chen**, Yao-Chieh Chen - *National Cheng Kung Univ.*

Special Session 4D - Advanced Logic Locking Techniques for Hardware IP Protection

Time: 8:30am - 10:00am | Room: Westminster III

Moderator:

Yier Jin - *Univ. of Florida*

Organizers:

Yier Jin - *Univ. of Florida*
Swarup Bhunia - *Univ. of Florida*

The globalization of the semiconductor supply chain introduces ever-increasing security and privacy risks. Two major concerns are IP theft through reverse engineering and malicious modification of the design. The latter concern in part relies on successful reverse engineering of the design as well. Developing low overhead locking/camouflaging schemes that can resist the ever-evolving state-of-the-art attacks has been a research challenge for several years. This special session provides a comprehensive overview of the state-of-art with respect to locking/camouflaging techniques.

4D.1 A Practical Application of Trust Through Technology
Yier Jin, Swarup Bhunia - *Univ. of Florida*
Eric Breckenfeld - *DARPA*
Saverio Fazzari - *Booz Allen Hamilton, Inc.*
Kenneth Plaks - *DARPA*

4D.2 Protecting Microelectronics IP: Issues, Needs, and Emerging Research Directions
Vipul J. Patel - *Air Force Research Lab*

4D.3 SFLL-HLS: Stripped-Functionality Logic Locking Meets High-Level Synthesis
Muhammad Yasin, Chongzhi Zhao, **Jeyavijayan Rajendran** - *Texas A&M Univ.*

4D.4 Resolving the Trilemma in Logic Encryption
Hai Zhou, Amin Rezaei, Yuanqi Shen - *Northwestern Univ.*

Coffee Break

Time: 10:00am - 10:30am | Room: Westminster Foyer

Session 5A - System-Level Attacks and Protection

Time: 10:30am - 12:00pm | Room: Westminster IV

Moderator:

Bo Yuan - *Rutgers Univ.*

Although powerful, the autonomous systems also expose to an emerging physical attacking space through software/hardware side-channels. This section includes papers that characterize, analyze, and defend against these attack scenarios and provide novel and unique solutions. The first paper proposes a novel metric for leakage assessment of power based side channel attacks on cryptographic implementations. The second paper presents an automated system to precisely and efficiently reposition the probe when performing repeated measurements. The third paper proposes a consolidated runtime-configurable hardware-assisted security mechanism, which supports proper security level according to the trade-off between security requirement and performance overhead.

5A.1 Holistic Power Side-Channel Leakage Assessment: Towards a Robust Multidimensional Metric
Alric Althoff, Jeremy Blackstone, Ryan Kastner - *Univ. of California, San Diego*

5A.2 Automated Probe Repositioning for On-Die EM Measurements
Bastian Richter - *Ruhr Univ. Bochum*
Alexander Wild - *NXP Semiconductors*
Amir Moradi - *Ruhr Univ. Bochum*

5A.3 CHASE: A Configurable Hardware-Assisted Security Extension for Real-Time Systems
Ghada Dessouky, Shaza Zeitouni, Ahmad Ibrahim - *Technische Univ. Darmstadt*
Lucas Davi - *Univ. of Duisburg-Essen*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt*

Session 5B - Pushing the Frontiers of Synthesis

Time: 10:30am - 12:00pm | Room: Westminster I

Moderator:

Mathias Soeken - *Swiss Federal Institute of Technology*

This session provides a new perspective to synthesis. The first paper proposes a new FPGA architecture and mapping flow, combining the completeness of LUT and the expressiveness of threshold logic functions. The second paper proposes a deep reinforcement learning scheduling solution for high-level synthesis in FPGA. The third paper introduces a novel canonical sentential decision diagram variant, showing smaller representation than other decision diagrams.

5B.1 Embedding Binary Perceptrons in FPGA to Improve Area, Power, and Performance
Ankit Wagle, Elham Azari, Sarma Vrudhula - *Arizona State Univ.*

5B.2 A Deep-Reinforcement-Learning-Based Scheduler for FPGA HLS
Hongzheng Chen, Minghua Shen - *Sun Yat-sen Univ.*

5B.3 Tagged Sentential Decision Diagrams: Combining Standard and Zero-Suppressed Compression and Trimming Rules
Liangda Fang - *Jinan Univ.*
Biqing Fang, Hai Wan - *National Sun Yat-sen Univ.*
Zeqi Zheng - *Jinan Univ.*
Liang Chang - *Guilin Univ. of Electronic Technology*
Quan Yu - *Qiannan Normal Univ. for Nationalities*

Session 5C - Advanced Design Techniques for Manufacturability

Time: 10:30am - 12:00pm | Room: Westminster II

Moderator:

Takashi Sato - *Kyoto Univ.*

This session introduces the latest progress in design for manufacturability techniques. The first paper proposes timing-aware fill insertion that simultaneously considers the total capacitance and metal density constraints for better timing and for less crosstalk. The second paper presents an ILP approach and a more efficient binary ILP approach for cut redistribution in two-dimensional directed self-assembly. The third paper critically analyzes existing works on machine learning-based lithographic hotspot detection and pinpoints their common misconceptions.

5C.1 Timing-Aware Fill Insertions with Design-Rule and Density Constraints
Tingshen Lan, Xingquan Li - *Fuzhou Univ.*
Jianli Chen - *Fudan Univ. & Fuzhou Univ.*
Jun Yu - *Fudan Univ.*
Lei He - *Univ. of California, Los Angeles*
Senhua Dong - *Huada Empyrean Software Co., Ltd*
Wenxing Zhu - *Fuzhou Univ.*
Yao-Wen Chang - *National Taiwan Univ.*

5C.2 Graph- and ILP-Based Cut Redistribution for Two-Dimensional Directed Self-Assembly
Zhan-Ling Wang, Yao-Wen Chang - *National Taiwan Univ.*

5C.3 Machine Learning-Based Hotspot Detection: Fallacies, Pitfalls and Marching Orders
Gaurav Rajavendra Reddy - *Univ. of Texas at Dallas*
Kareem Madkour - *Mentor, A Siemens Business*
Yiorgos Makris - *Univ. of Texas at Dallas*

Embedded Tutorial 5D - When Neural Networks Meet Hardware: The Princess, The Knight, and the Very Bad Dragon

Time: 10:30am - 12:00pm | Room: Westminster III

Moderator:
Qinru Qiu - *Syracuse Univ.*

Organizer:
Jingtong Hu - *Univ. of Pittsburgh*

Hardware acceleration of neural networks, which combines the performance of neural networks and the speed of dedicated hardware, has been widely adopted in many applications. However, the marriage between hardware and neural networks is not as straightforward as it seems. Careless implementations without considering various hardware related issues would easily lead to designs with inferior speed, performance, or even reliability. In this tutorial, three talks will cover the most critical parts in the design flow of hardware accelerators of neural networks. Specifically, the first talk will discuss hardware-aware neural architecture search; The second talk will introduce hardware-aware neural architecture compression; The third talk will cover hardware-defect-tolerant neural networks. Together they convey an important message that neural network and hardware needs to be co-designed and co-optimized throughout the design flow for maximum speed, performance and reliabilty.

5D.1 Hardware-Aware Neural Architecture Search
Qing Lu, Weiwen Jiang - *Univ. of Notre Dame*
Jingtong Hu - *Univ. of Pittsburgh*
Yiyu Shi - *Univ. of Notre Dame*

5D.2 How to Obtain and Run Light and Efficient Deep Learning Networks
Fan Chen, Wei Wen, Linghao Song, Jingchi Zhang, Hai Li, Yiran Chen - *Duke Univ.*

5D.3 Making the Fault-Tolerance of Emerging Neural Network Accelerators Scalable
Tao Liu - *Florida International Univ.*
Wujie Wen - *Lehigh Univ.*

Lunch

Time: 12:00pm - 12:30pm | Room: Legacy Ballroom

Join fellow attendees for lunch in Legacy Ballroom.

CEDA Invited Luncheon Talk: Current Progress in Quantum Computing

Time: 12:30pm - 1:30pm | Room: Legacy Ballroom

Speaker:

Paul Nation - *IBM T.J. Watson Research Center*

Since the first publicly available quantum computer was introduced by IBM in 2016, we have seen an explosion of interest in exploring the application of quantum computing systems to real-world problems. Although still in their infancy, quantum computers have already been applied in a variety of disciplines such as quantum chemistry, machine learning, and optimization. In this talk we give a brief overview of quantum computing before detailing the current state of the art in quantum computing hardware and software. We will see how these systems are helping to train users for the time when there is a definitive advantage to running certain tasks on a quantum computer.

Biography: Paul Nation is a theoretical physicist focusing on numerical methods for open quantum systems and high-fidelity quantum operations in superconducting quantum systems. He received his PhD in 2010 from Dartmouth College, and was a Postdoctoral Research at RIKEN in Japan. Before joining IBM Quantum he was an Assistant Professor at Korea University, and a Staff Physicist at Northrup Grumman.

Sponsored by: IEEE CEDA

Session 6A - Algorithmic Innovations for Neural Computing

Time: 1:45pm - 3:45pm | Room: Westminster IV

Moderator:

Xuan 'Silvia' Zhang - *Washington Univ.*

This section presents four interesting papers at the algorithmic aspect for neural computing. The first paper looks at methods to accelerate tensor decomposition on resource-constrained devices. The second paper presents a brain-inspired hyper-dimensional computational platform that is trained via a semi-supervised learning algorithm. The third paper proposes a novel disturbance-based method to encrypt the weights that are stored in non-volatile memory to achieve secure in-memory neural network computing. Finally, the last paper shows a methodology for neural architecture search with varying bit precision to design energy efficient architectures.

6A.1 Tucker Tensor Decomposition on FPGA
Kaiqi Zhang, Xiyuan Zhang, Zheng Zhang - *Univ. of California, Santa Barbara*

6A.2 SemiHD: Semi-Supervised Learning Using Hyperdimensional Computing
Mohsen Imani - *Univ. of California, San Diego*
Samuel Bosch - *École Polytechnique Fédérale de Lausanne*
Mojan Javaheripi, Bita Darvish Rouhani, Xinyu Wu, Farinaz Koushanfar, Tajana Rosing - *Univ. of California, San Diego*

6A.3 Enabling Secure in-Memory Neural Network Computing by Sparse Fast Gradient Encryption
Yi Cai - *Tsinghua Univ.*
Xiaoming Chen - *Chinese Academy of Sciences*
Lu Tian, Yu Wang, Huazhong Yang - *Tsinghua Univ.*

6A.4 Mixed Precision Neural Architecture Search for Energy Efficient Deep Learning
Chengyue Gong, **Zixuan Jiang**, Dilin Wang, Yibo Lin, Qiang Liu, David Z. Pan - *Univ. of Texas at Austin*

Session 6B - Verified and Efficient Embedded Security

Time: 1:45pm - 3:45pm | Room: Westminster I

Moderator:

Xiaolong Guo - *Kansas State Univ.*

This session presents verified and efficient techniques to enhance the security of embedded systems. The first paper proposes to use verified remote attestation for security software updates, erasure and resets. The second paper presents a multi-version concurrency control on intermittent systems. The third paper explores the reverse engineering approach to understand GPU memory resource allocation. The last paper develops an efficient genetic algorithm-based framework to speed up logic unlocking.

6B.1 PURE: Using Verified Remote Attestation to Obtain Proofs of Update, Reset and Erasure in Low-End Embedded Systems
Ivan De Oliveira Nunes - *Univ. of California, Irvine*
Karim Eldefrawy - *SRI International*
Norrathep Rattanavipanon, Gene Tsudik - *Univ. of California, Irvine*

6B.2 Multiversion Concurrency Control on Intermittent Systems
Wei-Ming Chen - *National Taiwan Univ. & Academia Sinica*
Yi-Ting Chen - *National Taiwan Univ.*
Pi-Cheng Hsiu - *Academia Sinica*
Tei-Wei Kuo - *National Taiwan Univ.*

6B.3 Understanding and Exploiting the Internals of GPU Resource Allocation for Critical Systems
Alejandro J. Calderón - *Univ. Politècnica de Catalunya & Ikerlan Technology Research Centre*
Leonidas Kosmidis - *Barcelona Supercomputing Center*
Carlos F. Nicolás - *Ikerlan Technology Research Centre*
Francisco J. Cazorla - *Barcelona Supercomputing Center*
Peio Onaindia - *Ikerlan Technology Research Centre*

***6B.4 GenUnlock: An Automated Genetic Algorithm Framework for Unlocking Logic Encryption**
Huili Chen, Cheng Fu, Jishen Zhao, Farinaz Koushanfar - *Univ. of California, San Diego*

Session 6C - Overcoming the Complexity of System Level Validation

Time: 1:45pm - 3:45pm | Room: Westminster II

Moderator:

Christopher Harris - *Auburn Univ.*

System level validation is getting more complicated for modern SoCs with increasing number of embedded cores. This session presents recent advancements in the field for overcoming the growing complexity challenges. The session includes four papers that address the challenges in different aspects, including two papers in emulation, one in multi-core memory coherence, and a novel approach to convert a combinational circuit into a sequential one.

6C.1 Reducing Compilation Effort in Commercial FPGA Emulation Systems Using Machine Learning
Anthony Agnesina - *Georgia Institute of Technology*
Etienne Lepercq, Jose Escobedo - *Synopsys, Inc.*
Sung Kyu Lim - *Georgia Institute of Technology*

6C.2 Golden Gate: Bridging The Resource-Efficiency Gap Between ASICs and FPGA Prototypes
Albert Magyar, David Biancolin, Jack Koenig, Sanjit Seshia, Jonathan Bachrach, Krste Asanović - *Univ. of California, Berkeley*

6C.3 Spec&Check: An Approach to the Building of Shared-Memory Runtime Checkers for Multicore Chip Design Verification
Marleson Graf, Olav P. Henschel, Rafael P. Alevato, **Luiz C. V. dos Santos** - *Federal Univ. of Santa Catarina*

6C.4 Time-Frame Folding: Back to the Sequentiality
Po-Chun Chien, Jie-Hong Roland Jiang - *National Taiwan Univ.*

Special Session 6D - Quantum Computing - Resilience and Security

Time: 1:45pm - 3:45pm | Room: Westminster III

Moderator:

Rolf Drechsler - *Univ. of Bremen*

Organizers:

Swaroop Ghosh - *Pennsylvania State Univ.*
Anupam Chattopadhyay - *Nanyang Technological Univ.*

The Noisy Intermediate Scale Quantum (NISQ) computers suffer from decoherence and gate errors. Quantum error correction (QEC) e.g., Shor code, Steane code, Surface code increases the overhead substantially e.g., 20X in surface code. Advancement in EDA is required to enhance the resilience by exploring trade-off opportunities present at various levels of design hierarchy, accommodate wide variety of qubits and their system architecture. A resilient quantum computer presents a threat to conventional crypto-systems since it can solve combinatorially hard problems such as, factorization. Post-Quantum Cryptography (PQC) is being developed to address this issue however their real deployment in a wide range of computing devices faces several challenges that need to be resolved. Quantum systems also bring new security promises in terms of Quantum Key Distribution (QKD), quantum-enabled security primitives e.g., TRNG. This special session that includes 5 invited talks by speakers from academia, industry and government agency, will provide in-depth treatment of both sides of the coin namely the resilience and security of NISQ era quantum computers including PQC/QKD. Talk-1 will describe a holistic quantum computer architecture for interfacing with Intel's quantum computer. Talk-2 will present NASA's perspective on algorithmic to device optimization for resilience. Talk-3 will introduce a single-pass qubit allocation and technology mapping flow for noise resilience. Talk-4 will discuss the security of quantum cryptography. Talk-5 will cover new approaches in lattice-based post-quantum cryptography.

6D.1 Quantum Computing: From Qubits to Quantum Accelerator
Koen Bertels - *Delft Univ. of Technology*

6D.2 A NASA Perspective on Quantum Computing
Eleanor Rieffel, **Zhihui Wang** - *NASA Ames Research Center*

6D.3 Integrated Qubit Allocation and Technology Mapping for NISQ Computing
Debjyoti Bhattacharjee - *Nanyang Technological Univ.*
Abdullah-Ash Saki, Mahabubul Alam - *Pennsylvania State Univ.*
Anupam Chattopadhyay - *Nanyang Technological Univ.*
Swaroop Ghosh - *Pennsylvania State Univ.*

6D.4 Security of Quantum Cryptography
Anindita Banerjee - *QuNu Labs*
MT Karunakaran - *QuNu labs*

6D.5 Engineering Lattice-Based Post-Quantum Cryptography
Sujoy Sinha Roy - *Univ. of Birmingham*

Coffee Break

Time: 3:45pm - 4:15pm | Room: Westminster Foyer

Special Session 7A - The Road to Safe Autonomy: Neural Networks Meet Formal Reasoning

Time: 4:15pm - 6:15pm | Room: Legacy Ballroom

Moderator:

Wenchao Li - *Boston Univ.*

Organizers:

Wenchao Li - *Boston Univ.*
Jyotirmoy Deshmukh - *Univ. of Southern California*

Recent advances in neural networks and deep learning have spurred a race towards increasing autonomy in both civilian and military spaces. However, recent incidents such as the Uber crash in March 2018 have raised alarms over the safety of these autonomous systems. This session introduces the topic of safety assurance of autonomous systems through the lens of formal reasoning. The four talks are contributed by experts in this field from both academia and industry, and discuss existing techniques and open challenges of safety assurance in diverse applications such as automated insulin delivery and autonomous driving.

7A.1 Verifying Conformance of Neural Network Models
Monal Narasimhamurthy, Taisa Kushner, Souradeep Dutta, **Sriram Sankaranarayanan** - *Univ. of Colorado*

7A.2 nn-Dependability-Kit: Engineering Neural Networks for Safety-Critical Autonomous Driving Systems
Chih-Hong Cheng, Chung-Hao Huang, Georg Nührenberg - *fortiss GmbH*

7A.3 Learning Deep Neural Network Controllers for Dynamical Systems with Safety Guarantees
Jyotirmoy Deshmukh - *Univ. of Southern California*
James Kapinski - *Amazon.com, Inc.*
Tomoya Yamaguchi, Danil Prokhorov - *Toyota Research Institute of North America*

7A.4 Towards Verification-Aware Knowledge Distillation for Neural-Network Controlled Systems
Jiameng Fan - *Boston Univ.*
Chao Huang - *Northwestern Univ.*
Wenchao Li - *Boston Univ.*
Xin Chen - *Univ. of Dayton*
Qi Zhu - *Northwestern Univ.*

Session 7B - Accelerator Design and Modeling

Time: 4:15pm - 6:15pm | Room: Westminster I

Moderator:

Joerg Henkel - *Karlsruhe Institute of Technology*

This session includes papers that propose novel methodologies, which enable exploration of the accelerator design space. The first two papers focus on modeling energy consumption in accelerators, while the third paper focuses on jointly optimizing accuracy of the DNNs and energy consumed by the underlying hardware.

7B.1 A Uniform Modeling Methodology for Benchmarking DNN Accelerators
Indranil Palit - *Valeo*
Qiuwen Lou, Robert Perricone, Michael Niemier, X. Sharon Hu - *Univ. of Notre Dame*

7B.2 PABO: Pseudo Agent-Based Multi-Objective Bayesian Hyperparameter Optimization for Efficient Neural Accelerator Design
Maryam Parsa, Aayush Ankit - *Purdue Univ.*
Amirkoushyar Ziabari - *Oak Ridge National Laboratory*
Kaushik Roy - *Purdue Univ.*

7B.3 Accelergy: An Architecture-Level Energy Estimation Methodology for Accelerator Designs
Yannan N. Wu, Joel S. Emer - *Massachusetts Institute of Technology & NVIDIA Corp.*
Vivienne Sze - *Massachusetts Institute of Technology*

Session 7C - Combating Circuit Aging and Device Variability

Time: 4:15pm - 6:15pm | Room: Westminster II

Moderator:

Vojtech Mrazek - *Brno Univ. of Technology*

Timing, reliability, and variability have been critical issues in circuit designs when process technology enters into sub-10nm era.

The first paper in this session proposes an asymmetric aging concept to enhance reliability for multi-core systems. The second paper proposes an analytical timing model, that is applicable for statistical timing calculation of near threshold circuits. The third paper presents a meta-model based importance sampling method for efficient yield estimation of SRAM cells.

7C.1 ROAD: Improving Reliability of Multi-Core Systems via Asymmetric Aging
Yu-Guang Chen - *National Central Univ.*
Ing-Chao Lin, Jian-Ting Ke - *National Cheng Kung Univ.*

7C.2 A Statistical Timing Model for Low Voltage Design Considering Process Variation
Peng Cao, Zhiyuan Liu, Jiangping Wu, Jingjing Guo, Jun Yang, Longxing Shi - *Southeast Univ.*

7C.3 Efficient Yield Analysis for SRAM and Analog Circuits using Meta-Model Based Importance Sampling Method
Xiao Shi - *Univ. of California, Los Angeles*
Hao Yan, Jiajia Zhang, Qiancun Huang, Longxing Shi - *Southeast Univ.*
Lei He - *Univ. of California, Los Angeles*

Special Session 7D - Breaking the Ice Between Silicon Photonics Design and EDA: Electronic-Photonic Design Automation

Time: 4:15pm - 6:15pm | Room: Westminster III

Moderator:

Joerg Henkel - *Karlsruhe Institute of Technology*

Organizers:

Mahdi Nikdast - *Colorado State Univ.*
Ulf Schlichtmann - *Tech. Univ. of Munich*

Silicon Photonics (SiPh) is rapidly emerging as a standard platform for large-scale photonic integrated circuits. Today's SiPh circuits, which are mostly Datacom-driven, are generally small in size and low in complexity (i.e., circuits with a small number of optical devices and/or simple repetitive scaling, e.g., a transceiver). However, emerging applications of SiPh (e.g., HPC, biosensing, quantum computing, LIDAR) are pushing the boundaries of such simple designs, creating a bottleneck for the current component-oriented SiPh design. This necessitates a more circuit-oriented design flow, which makes abstraction from the very detailed geometry and enables design on a larger scale. As a result, the SiPh design process is evolving along the lines of electronic design automation (EDA), hence the term electronic-photonic design automation (EPDA). This special session discusses the state-of-the-art of this emerging SiPh circuit design flow and its synergies with EDA. It discusses the most recent advances in EPDA, the design challenges and requirements that can be addressed through design automation solutions to scale SiPh circuits, as well as those in systems integrating optical interconnects. Particularly, the session aims at bridging the gap between the Silicon Photonics Community and the EDA and CAD community, discussing the latest advances and challenges that can be addressed by each community. It is comprised of five invited talks from pioneer groups in both academia and industry. This special session is of high interest to researchers who want to learn about the promise of silicon photonics and understand potential research topics and challenges related to the design of such circuits that can be addressed through design automation and CAD solutions. Moreover, those already working on silicon photonics and want to understand the promise of design automation in SiPh design will highly benefit from this special session.

7D.1 Wavelength-Routed Optical NoCs: Design and EDA – State of the Art and Future Directions
Tsun-Ming Tseng, Alexandre Truppel, Mengchu Li - *Tech. Univ. of Munich*
Mahdi Nikdast - *Colorado State Univ.*
Ulf Schlichtmann - *Tech. Univ. of Munich*

7D.2 Design Technology for Scalable and Robust Photonic Integrated Circuits
Zheng Zhao, Zhoufeng Ying, Chenghao Feng, Jiaqi Gu, **Ray T. Chen**, David Z. Pan - *Univ. of Texas at Austin*

7D.3 Systematic Exploration of High-Radix Integrated Silicon Photonic Switches for Datacenters
Zhifei Wang, Jiang Xu, Xuanqi Chen, Zhehui Wang, Jun Feng, Jiaxu Zhang, Shixi Chen - *Hong Kong Univ. of Science and Technology*

7D.4 Latest Advancements to the Industry-Leading EPDA Design Flow for Silicon Photonics
James Pond, Xu Wang, Zeqin Lu - *Lumerical Inc.*
Gilles Lamant, Ahmadreza Farsaei - *Cadence Design Systems, Inc.*

7D.5 From Inverse Design to Implementation of Practical Photonics
Jinhie Skarda, Logan Su, **Ki Youl Yang**, Dries Vercruysse, Rahul Trivedi, Jelena Vuckovic - *Stanford Univ.*

All speakers are denoted in bold | * denotes Best Paper Candidate

Networking Reception

Time: 6:15pm - 6:45pm | Room: Westminster Foyer

Whatever your goal, networking receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day's presentations with the conference presenters. All attendees are invited.

Sponsored by: SYNOPSYS® Silicon to Software™

Additional Meeting - ACM/SIGDA Member Meeting

Time: 6:45pm - 8:30pm | Room: Legacy Ballroom

The annual ACM/SIGDA Member Meeting will be held on Tuesday evening from 6:45 - 8:00pm. The meeting is open for ACM SIGDA members to attend. Members of the Electronic Design Automation community who would like to learn more about SIGDA or get involved with SIGDA activities are also invited. Dinner and beverages will be served.

The meeting will begin with a brief overview of SIGDA, including its organization, activities, volunteering opportunities, and member benefits. Next, the Outstanding Young Faculty Award winner will present a brief talk on his work. Finally, we will end the evening with the announcement of the winners of ACM Design Automation Student Research Competition taking place at this year's ICCAD. We hope to see you there!

Sponsored by: sigda special interest group on design automation acm

WEDNESDAY SCHEDULE

8:30 - 9:30am

Keynote: Probabilistic and Machine Learning Approaches for Autonomous Robots and Automated Driving

Wolfram Burgard - Toyota Research Institute | Location: Westminster IV

9:30 - 10:00am

Coffee Break

Location: Westminster Foyer

9:45 - 11:45pm

Session 8A: In-Memory and Analog-Domain Neural Computing

Location: Westminster IV

Session 8B: Hot Data Architectures

Location: Westminster I

Session 8C: Adaptive Cyber-Physical Systems

Location: Westminster II

Special Session 8D: Results, Perspectives and Trends on Open-Source EDA

Location: Westminster III

11:45am - 12:45pm

Lunch

Location: Legacy Ballroom

1:00 - 3:00pm

Session 9A: (Un)Locking the Pandora's Box: Logic Locking Techniques

Location: Westminster IV

Special Session 9B: Open-Source Microfluidic Design Ecosystem: Recent Developments and Upcoming Challenges

Location: Westminster I

Session 9C: Analog Layout and Performance Optimization

Location: Westminster II

Special Sessionl 9D: Tensor Methods for Accelerated Machine Learning and Electronic Design Automation

Location: Westminster III

WEDNESDAY SCHEDULE

3:00 - 3:30pm

Coffee Break

Location: Westminster Foyer

3:30 - 5:00pm

Session 10A: Mitigating Side-Channel Analysis: From EDA to Cloud

Location: Westminster IV

Session 10B: Thermal and Power Management for Circuits and Systems

Location: Westminster I

Session 10C: Global and Detailed Routing

Location: Westminster II

Special Session 10D: The Impact of Emerging Technologies on Architectures and System-Level Management

Location: Westminster III

5:00 - 5:30pm

Networking Reception

Location: Westminster Foyer

Sponsored by: HUAWEI

5:30 - 7:00pm

Career & Diversity @ ICCAD

Location: Westminster IV

Sponsored by: SIGDA

Keynote: Probabilistic and Machine Learning Approaches for Autonomous Robots and Automated Driving

Time: 8:30am - 9:30am | Room: Westminster IV

Speaker:
Wolfram Burgard - *Toyota Research Institute*

The capability to robustly perceive their environments and to execute their actions is the ultimate goal in the areas autonomous robots and automated driving. The key challenge is that there are no sensors and no actuators that are perfect, which means that robots and cars need the ability to properly deal with the resulting uncertainty. In this presentation I will provide an introduction to the probabilistic approach to robotics, which provides a rigorous statistical methodology to deal with the perception and planning. I will furthermore discuss how this approach can be extended using state-of-the-art technology from machine learning to bring us closer to the development of truly robust systems able to serve us in our every-day life.

Biography:Wolfram Burgard is VP for Automated Driving Technology at the Toyota Research Institute in Los Altos, USA. He is on leave from a Professorship for Autonomous Intelligent Systems at the Univ. of Freiburg, Germany. His interests lie in AI and Robotics. He has made substantial contributions to several relevant problems including state estimation, navigation, localization, SLAM and mobile manipulation. For his work, Wolfram Burgard received the Gottfried Wilhelm Leibniz Prize from the Deutsche Forschungsgemeinschaft, the most prestigious German research award, and an Advanced Grant from the European Research Council. He is fellow of the AAAI, the EurAI as well as the IEEE. He currently also serves as President of the IEEE Robotics and Automation Society.

Coffee Break

Time: 9:30am - 10:00am | Room: Westminster Foyer

Session 8A - In-Memory and Analog-Domain Neural Computing

Time: 9:45am - 11:45am | Room: Westminster IV

Moderator:

Chia-Lin Yang - *National Taiwan Univ.*

This session presents novel techniques that look beyond conventional digital implementation to enable efficient deep learning and neuromorphic computing. One direction is to explore analog and mixed-signal domain representations; another is to perform the in-situ computation inside the memory to reduce expensive data movement.

8A.1 Neural Network-Inspired Analog-to-Digital Conversion to Achieve Super-Resolution with Low-Precision RRAM Devices
Weidong Cao, Liu Ke, Ayan Chakrabarti, Xuan Zhang - *Washington Univ.*

8A.2 An Event-Driven Neuromorphic System with Biological Plausible Temporal Dynamics
Haowen Fang, Amar Shrestha, Ziyi Zhao, Yilan Li, **Qinru Qiu** - *Syracuse Univ.*

8A.3 A PVT-Robust Customized 4T Embedded DRAM Cell Array for Accelerating Binary Neural Networks
Hyein Shin, Jaehyeong Sim, Daewoong Lee, Lee-Sup Kim - *Korea Advanced Institute of Science and Technology*

8A.4 An Energy-Efficient Processing-in-Memory Architecture for Long Short Term Memory in a Spin Orbit Torque MRAM
Kyeonghan Kim, Hyein Shin, Jaehyeong Sim, Myeonggu Kang, Lee-Sup Kim - *Korea Advanced Institute of Science and Technology*

Session 8B - Hot Data Architectures

Time: 9:45am - 11:45am | Room: Westminster I

Moderator:

Tulika Mitra - *National Univ. of Singapore*

This session brings together research that looks into the challenges of coping with hot data, minimizing data movement with innovative storage and computation architectures, and accelerating storage management for data that is no longer hot.

8B.1 Re-Tangle: ReRAM-Based Processing-in-Memory Architecture for Transaction-Based Blockchain
Qian Wang, Tianyu Wang, **Zhaoyan Shen**, Zhiping Jia, Mengying Zhao - *Shandong Univ.*
Zili Shao - *Chinese Univ. of Hong Kong*

8B.2 HAML-SSD: A Hardware Accelerated Hotness-Aware Machine Learning Based SSD Management
Bingzhe Li - *Univ. of Minnesota, Twin Cities*
Chunhua Deng - *Rutgers Univ.*
Jinfeng Yang, David Lilja - *Univ. of Minnesota, Twin Cities*
Bo Yuan - *Rutgers Univ.*
David Du - *Univ. of Minnesota, Twin Cities*

8B.3 Accelerating Garbage Collection for 3D MLC Flash Memory with SLC Blocks
Shuai Li, Wei Tong, Jingning Liu, **Bing Wu**, Yazhi Feng - *Huazhong Univ. of Science & Technology*

Session 8C - Adaptive Cyber-Physical Systems

Time: 9:45am - 11:45am | Room: Westminster II

Moderator:

Zili Shao - *Chinese Univ. of Hong Kong*

This session presents work on innovative techniques for runtime adaptation across diverse cyber-physical systems, spanning wearable sensing platforms, automotive systems, and FPGA platforms.

8C.1 Multi-Stage Optimization for Energy-Efficient Active Cell Balancing in Battery Packs
Debayan Roy, Swaminathan Narayanaswamy, Alma Pröbstl, Samarjit Chakraborty - *Tech. Univ. of Munich*

8C.2 Adar: Adversarial Activity Recognition in Wearables
Ramesh K. Sah, Hassan Ghasemzadeh - *Washington State Univ.*

8C.3 4D-CGRA : Introducing Branch Dimension to Spatio-Temporal Application Mapping on CGRAs
Manupa Karunaratne, Dhananjaya Wijerathne, Tulika Mitra, Li-Shiuan Peh - *National Univ. of Singapore*

8C.4 WCET Guarantees for Opportunistic Runtime Reconfiguration
Marvin Damschen, **Lars Bauer**, Jörg Henkel - *Karlsruhe Institute of Technology*

Special Session 8D - Results, Perspectives and Trends on Open-Source EDA

Time: 9:45am - 11:45am | Room: Westminster III

Moderator:

Alexandre Levisse - *École Polytechnique Fédérale de Lausanne*

Organizer:

Pierre-Emmanuel Gaillardon - *Univ. of Utah*

While academic research has been long fueling innovations in Electronic Design Automation, the recently introduced DARPA Electronics Resurgence Initiative with a $1.5B funding did put open-source EDA in the spotlight. The aim of this special session is to present an overview of the current situation in the four main fields of EDA, namely logic synthesis, digital physical design, digital verification and analog physical design.

8D.1 Looking Into the Mirror of Open Source
Andrew B. Kahng - *Univ. of California, San Diego*

8D.2 LSOracle: a Logic Synthesis Framework Driven by Artificial Intelligence
Walter Lau Neto, Max Austin, Scott Temple - *Univ. of Utah*
Luca Amaru - *Synopsys, Inc.*
Xifan Tang, **Pierre-Emmanuel Gaillardon** - *Univ. of Utah*

8D.3 Unlocking the Power of Formal Hardware Verification with CoSA and Symbolic QED
Florian Lonsing, Karthik Ganesan, Makai Mann, Srinivasa Shashank Nuthakki, Eshan Singh, Mario Srouji, Yahan Yang, Subhasish Mitra, Clark Barrett - *Stanford Univ.*

8D.4 MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence
Biying Xu, Keren Zhu, Mingjie Liu, Yibo Lin, Shaolan Li, Xiyuan Tang, Nan Sun, **David Pan** - *Univ. of Texas at Austin*

Lunch

Time: 11:45am - 12:45pm | Room: Legacy Ballroom

Join fellow attendees for lunch in Legacy Ballroom.

Session 9A - (Un)Locking the Pandora's Box: Logic Locking Techniques

Time: 1:00pm - 3:00pm | Room: Westminster IV

Moderator:

Muhammad Yasin - *Texas A&M Univ.*

Logic locking techniques actively defend against attacks in the semiconductor supply chain, including overproduction, piracy, and reverse engineering. In this session, we have three papers discussing the two sides of logic locking: attacks and defenses. The first paper targets locked sequential designs even when their scan chain is inaccessible. The second paper breaks many locking techniques that introduce loops into circuits. Finally, the third paper sheds light on what secure locking techniques will look like in the future.

9A.1 Is Robust Design-for-Security Robust Enough? Attack on Locked Circuits with Restricted Scan Chain Access
Nimisha Limaye, Abhrajit Sengupta - *New York Univ.*
Mohammed Nabeel, Ozgur Sinanoglu - *New York Univ., Abu Dhabi*

9A.2 IcySAT: Improved SAT-Based Attacks on Cyclic Locked Circuits
Kaveh Shamsi - *Univ. of Florida*
David Z. Pan - *Univ. of Texas at Austin*
Yier Jin - *Univ. of Florida*

***9A.3 Security and Complexity Analysis of LUT-based Obfuscation: From Blueprint to Reality**
Gaurav Kolhe - *Univ. of California, Davis*
Hadi Mardani Kamali - *George Mason Univ.*
Miklesh Naicker, Tyler David Sheaves, Hamid Mahmoodi - *San Francisco State Univ.*
Sai Manoj Pudukotai Dinakarrao - *George Mason Univ.*
Houman Homayoun - *Univ. of California, Davis*
Setareh Rafatirad, Avesta Sasan - *George Mason Univ.*

Special Session 9B - Open-Source Microfluidic Design Ecosystem: Recent Developments and Upcoming Challenges

Time: 1:00pm - 3:00pm | Room: Westminster I

Moderator:

Tsung-Yi Ho - *National Tsing Hua Univ.*

Organizer:

Tsung-Yi Ho - *National Tsing Hua Univ.*

Despite the impressive research progress over the last 15-20 years and recent commercialization, the microfluidic community is still rather small. That is mainly because the development of microfluidics products today is of low efficiency and high cost. First, lacking of standardized rule and design automation tools for microfluidics, one has to draw the layout of a device manually which may take weeks; second, due to small number of microfluidic chips a lab normally requires, making small amount microfluidic chips is much more expensive than mass production; third, people are using non-standardized components and application-unique layout. There is almost no ability to connect disparate parts to synergies breakthroughs or to create economic development via specialization.

To keep microfluidic community growing, we looked into the possibility of building an open-source ecosystem where a wide range of users (e.g., researchers, entrepreneurs, students, hobbyists) can focus on their own ideas and applications without worrying about the engineering and manufacturing side of microfluidic technology.

The session will consist of five talks on comprehensive aspects of both open-source software and hardware for digital and continuous-flow microfluidic research, including open-source incubation ecosystem, cloud-based platform, API, benchmark, and its application on Internet of Microfluidic Things. We believe that the special session will generate interest in this topic, leading to more research, future challenges, and several open problems in this area. This is a novel and multidisciplinary topic of relevance to the EDA community.

9B.1 Open-Source Incubation Ecosystem for Digital Microfluidics — Status and Roadmap
Xing Huang, Chi-Chun Liang - *National Tsing Hua Univ.*
Jia Li - *Univ. of California, Los Angeles*
Tsung-Yi Ho - *National Tsing Hua Univ.*
Chang-Jin Kim - *Univ. of California, Los Angeles*

9B.2 Scaling Microfluidics to Complex, Dynamic Protocols
Max Willsey, Ashley Stephenson, Chris Takahashi - *Univ. of Washington*
Bichlien Nguyen, Karin Strauss - *Microsoft*
Luis Ceze - *Univ. of Washington*

9B.3 Specification, Integration, and Benchmarking of Continous Flow Microfluidic Devices
Radhakrishna Sanka - *Boston Univ.*
Brian Crites, Jeffrey McDaniel, **Philip Brisk** - *Univ. of California, Riverside*
Douglas Densmore - *Boston Univ.*

9B.4 Cloud Columba: Accessible Design Automation Platform for Production and Inspiration
Tsun-Ming Tseng, Mengchu Li, Yushen Zhang - *Tech. Univ. of Munich*
Tsung-Yi Ho - *National Tsing Hua Univ.*
Ulf Schlichtmann - *Tech. Univ. of Munich*

9B.5 The Internet of Microfluidic Things: Perspectives on System Architecture and Design Automation
Mohamed Ibrahim - *Intel*
Maria Gorlatova, Krishnendu Chakrabarty - *Duke Univ.*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 9C - Analog Layout and Performance Optimization

Time: 1:00pm - 3:00pm | Room: Westminster II

Moderator:

Evangeline F.Y. Young - *Chinese Univ. of Hong Kong*

This session presents a set of novel techniques for analog circuit design. The first half of the session addresses routing, while the second half is related to performance optimization. The first paper in the session uses generative neural network techniques to solve the analog routing problem, mimicking human design through network training. In the next paper, a novel routing model based on Cartesian detection lines is used to migrate layouts from one technology node to another. The last two papers are directed toward optimizing the performance of analog circuits using Bayesian optimization to model the Pareto front of optimal designs, and by using transposed neural networks to model and optimize inductors in voltage regulator circuits.

9C.1 GeniusRoute: A New Analog Routing Paradigm Using Generative Neural Network Guidance
Keren Zhu, Mingjie Liu, Yibo Lin, Biying Xu, Shaolan Li, Xiyuan Tang, Nan Sun, David Z. Pan - *Univ. of Texas at Austin*

9C.2 Achieving Routing Integrity in Analog Layout Migration via Cartesian Detection Lines
Hao-Yu Chi - *National Chiao Tung Univ.*
Zi-Jun Lin, Chia-Hao Hung - *National Central Univ.*
Chien-Nan Liu, Hung-Ming Chen - *National Chiao Tung Univ.*

9C.3 Efficient Performance Trade-off Modeling for Analog Circuit based on Bayesian Neural Network
Zhengqi Gao, Jun Tao, Fan Yang, Yangfeng Su - *Fudan Univ.*
Dian Zhou - *Univ. of Texas at Dallas*
Xuan Zeng - *Fudan Univ.*

9C.4 A Spectral Convolutional Net for Co-Optimization of Integrated Voltage Regulators and Embedded Inductors
Hakki Torun, Huan Yu, Nihar Dasari, Venkata Chaitanya Krishna Chekuri, Arvind Singh, Jinwoo Kim, Sung Kyu Lim, Saibal Mukhopadhyay, Madhavan Swaminathan - *Georgia Institute of Technology*

Special Session 9D - Tensor Methods for Accelerated Machine Learning and Electronic Design Automation

Time: 1:00pm - 3:00pm | Room: Westminster III

Moderator:

Wei Zhang - *Hong Kong Univ. of Science and Technology*

Organizers:

Zhiru Zhang - *Cornell Univ.*
Zheng Zhang - *Univ. of California, Santa Barbara*

As a high-order generalization of matrices and vectors, tensor computation has emerged as a powerful tool to solve high-dimensional problems in scientific computing, machine learning, data mining and optimal control. Despite its superior efficiency in overcoming the curse of dimensionality, the research of tensor computation in hardware accelerators and in EDA is still in the early stage.

Recently we note that an active body of research has emerged in both academia and industry, ranging from hardware design to EDA algorithms, making encouraging progress in both theory and engineering applications. This special session will present a number of these research efforts, with topics ranging from new tensor-based EDA algorithms (wafer data analysis, circuit modeling and simulation, parasitic extraction, uncertainty quantification) to tensor hardware accelerators (tensorized DNN on edge devices, architecture for tensor-based DNN). We envision that the discussions in this session will lead to novel cross-layer solutions the enable highly efficient tensor-based machine learning systems and EDA frameworks.

9D.1 DEEPEYE: A Deeply Tensor Compressed Neural Network Hardware accelerator
Yuan Cheng - *Shanghai Jiaotong Univ.*
Guangya Li - *Southern Univ. of Science and Technology*
Ngai Wong - *Univ. of Hong Kong*
Hai-Bao Chen - *Shanghai Jiao Tong Univ.*
Hao Yu - *Southern Univ. of Science and Technology*

9D.2 High-Performance Hardware Architecture for Tensor Singular Value Decomposition
Chuanhua Deng - *Rutgers Univ.*
Xiaoyang Liu - *Columbia Univ.*
Miao Yin - *Rutgers Univ.*
Xiaodong Wang - *Columbia Univ.*
Bo Yuan - *Rutgers Univ.*

9D.3 Tensor Methods for Generating Compact Uncertainty Quantification and Deep Learning Models
Chunfeng Cui, Cole Hawkins, Zheng Zhang - *Univ. of California, Santa Barbara*

9D.4 Tensor Methods for Modeling Nonlinear Circuits and Systems
Ngai Wong - *Univ. of Hong Kong*

9D.5 Facilitating Deployment Of A Wafer-Based Analytic Software Using Tensor Methods
Li-C. Wang, Chuanhe (Jay) Shan, Ahmed Wahba - *Univ. of California, Santa Barbara*

9D.6 Tensor Train Accelerated Electromagnetic Modeling of Interconnects
Shucheng Zheng - *Univ. of Manitoba*
Zhuotong Chen - *Univ. of California, Santa Barbara*
Vladimir Okhmatovski - *Univ. of Manitoba*

Coffee Break

Time: 3:00pm - 3:30pm | Room: Westminster Foyer

Session 10A - Mitigating Side-Channel Analysis: From EDA to Cloud

Time: 3:30pm - 5:00pm | Room: Westminster IV

Moderator:

Wenjie Che - *New Mexico State Univ.*

This session is on mitigating power-based side-channel analysis with three papers targeting different abstraction layers. The first paper focuses on EDA techniques to automatically identify and modify vulnerable gates in a netlist. The second paper proposes circuit-level techniques for randomizing the clock source to hide side-channel exposure. The last paper analyzes remote side-channel attacks on multi-tenant FPGA clouds and demonstrates strategies for improving side-channel resiliency.

10A.1 Karna: A Gate-Sizing Based Security Aware EDA Flow for Improved Power Side-Channel Attack Protection

Patanjali Slpsk, **Prasanna Karthik Vairam**, Chester Rebeiro - *Indian Institute of Technology Madras*
Kamakoti V - *Professor*

10A.2 SCRIP: Secure Random Clock Execution on Soft Processor Systems to Mitigate Power-Based Side Channel Attacks

Darshana Jayasinghe, Aleksandar Ignjatovic, Sri Parameswaran - *Univ. of New South Wales*

10A.3 Active Fences against Voltage-Based Side Channels in Multi-Tenant FPGAs

Jonas Krautter, **Dennis Gnad** - *Karlsruhe Institute of Technology*
Falk Schellenberg, Amir Moradi - *Ruhr Univ. Bochum*
Mehdi Tahoori - *Karlsruhe Institute of Technology*

Session 10B - Thermal and Power Management for Circuits and Systems

Time: 3:30pm - 5:00pm | Room: Westminster I

Moderator:

Yu Wang - *Tsinghua Univ.*

This session covers topics in thermal and power-aware design methods. The first paper presents a clock gating technique to address cyclic logic paths. The second paper presents a dynamic power management scheme utilizing predictive models to leverage timing slack in varying workload characteristics in a multi-FPGA system. Finally, the session is concluded with a temperature modeling approach that can reach nanoscale spatial resolution with high accuracy.

10B.1 Clock Gating Synthesis of Netlist with Cyclic Logic Paths
Yonghwi Kwon - *Korea Advanced Institute of Science and Technology*
Inhak Han - *BAUM*
Youngsoo Shin - *Korea Advanced Institute of Science and Technology*

10B.2 Workload-Aware Opportunistic Energy Efficiency in Multi-FPGA Platforms
Sahand Salamat, Behnam Khaleghi, Mohsen Imani, Tajana Rosing - *Univ. of California, San Diego*

***10B.3 NanoTherm: An Analytical Fourier-Boltzmann Framework for Full Chip Thermal Simulations**
Shashank Varshney, Hameedah Sultan - *Indian Institute of Technology Delhi*
Palkesh Jain - *Qualcomm Technologies, Inc.*
Smruti R. Sarangi - *Indian Institute of Technology Delhi*

Session 10C - Global and Detailed Routing

Time: 3:30pm - 5:00pm | Room: Westminster II

Moderator:

William Swartz - *Timberwolf Systems, Inc.*

Finding good routing solutions is one of the most critical challenges for the advanced nodes. If congestion and routing violations cannot be resolved, designs go nowhere. This session first presents a new way to model global routing graph which haven't been changed for decades. Then, a hybrid multi-threading scheme is introduced to further speedup global routing algorithms. Last but not least, a detailed routing paper will be presented to minimize design-rule-checking violations and converge routing challenges.

10C.1 Global Routing on Rhomboidal Tiles
Nicolai Hähnle - *Advanced Micro Devices, Inc.*
Pietro Saccardi - *Univ. of Bonn*

10C.2 SPRoute: A Scalable Parallel Negotiation-based Global Router
Jiayuan He - *Univ. of Texas at Austin*
Martin Burtscher - *Texas A&M Univ.*
Rajit Manohar - *Yale Univ.*
Keshav Pingali - *Univ. of Texas at Austin*

10C.3 Dr. CU 2.0: A Scalable Detailed Routing Framework with Correct-by-Construction Design Rule Satisfaction
Haocheng Li, Gengjie Chen, Bentian Jiang, Jingsong Chen, Evangeline Young - *Chinese Univ. of Hong Kong*

Special Session 10D - The Impact of Emerging Technologies on Architectures and System-Level Management

Time: 3:30pm - 5:00pm | Room: Westminster III

Moderator:

Sri Parameswaran - *Univ. of New South Wales*

Organizers:

Jörg Henkel - *Karlsruhe Institute of Technology (KIT)*
Hussam Amrouch - *Karlsruhe Institute of Technology (KIT)*

The goal of this session is to introduce and discuss different kinds of emerging technologies for logic circuitry and memory with respect to the key question of how they will impact future system-on-chip architectures and system-level management techniques. It is obvious that emerging technologies should have an impact there in order to fully exploit their technological advantages but also in order to deal with any disadvantages they might come with. In this special session, three promising emerging technologies are presented: (i) Negative Capacitance Field-Effect Transistor (NCFET) as a new CMOS technology with advantages primarily for low-power design, (ii) Ferroelectric FET (FeFET) as a non-volatile, area-efficient and low-power combined logic and memory as well as (iii) a Phase-Change Memory (PCM) and Resistive RAM (ReRAM) offering a large potential for tackling the memory wall problem in the von Neumann architecture. Our analysis demonstrates that not only new computing paradigms are promoted by these new technologies, it will also be seen that the trade-offs between the classical design parameters of low power, performance etc. will shift and hence emerging technologies will offer new Pareto points in the design space of future on-chip architectures. In that context, this special session is unique as it bridges the gap between the technology side and system/architecture-level side to draw a vision of new technologies and their impact on architectures and system-level management.

10D.1 NCFET's Impact on Architecture and System-Level Management

Jörg Henkel, Hussam Amrouch, Martin Rapp, Sami Salamin - *Karlsruhe Institute of Technology (KIT)*
Dayane Reis - *Univ. of Notre Dame*
Di Gao - *Zhejiang Univ.*
Michael Niemier, Cheng Zhou, X. Sharon Hu - *Univ. of Notre Dame*
Hsiang-Yun Cheng - *Academia Sinica*
Chia-Lin Yang - *National Taiwan Univ.*

10D.2 Blurring the Boundary of Compute and Memory via FeFETs

Dayane Reis - *Notre Dame Univ.*
Di Gao - *Zhejiang Univ.*
Xunzhao Yin, Michael Niemier - *Univ. of Notre Dame*
Cheng Zhuo - *Zhejiang Univ.*
X. Sharon Hu - *Univ. of Notre Dame*

10D.3 Device-Architecture Co-Design to Enable Future Resistive Memory Systems

Hsiang-Yun Cheng - *Research Center for Information Technology Innovation, Academia Sinica*
Chia-Lin Yang - *National Taiwan Univ.*

Networking Reception

Time: 5:00pm - 5:30pm | Room: Westminster Foyer

Whatever your goal, networking receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day's presentations with the conference presenters. All attendees are invited.

Sponsored by: HUAWEI

Additional Meeting - Career & Diversity @ ICCAD

Time: 5:30pm - 7:00pm | Room: Westminster IV

Moderator:

Patrick Groeneveld - *Stanford Univ.*

Organizers:

Evangeline Young - *The Chinese Univ. of Hong Kong*
Patrick Groeneveld - *Stanford Univ.*

This session will focus primarily on two closely related issues, career development and diversity at work. Recruiters from industry will share their views and opinions on what companies are looking for from young graduates, and there will also be sharings from young graduates from industry on their works, experiences, and tips in locating a suitable career for PhD students who are going to graduate soon. While career planning and development is important for individuals, diversity at work is an essential ingredient for a healthy organization and company. Studies have shown that diverse companies have a significantly higher chance of success with more financial returns above their respective industry medians. This session will also seek to increase understanding of the importance of diversity and inclusion at works. Light food and beverage will be provided.

Speakers:

Laleh Behjat - *Univ. of Calgary*
Meng Li - *Facebook*
Rangharajan Venkatesan - *NVIDIA Corp.*

Sponsored by: SIGDA

THURSDAY SCHEDULE

8:00am - 12:00pm

Hands On Workshop on Machine Learning, Deep Learning and Reinforcement Learning for EDA Developers

Location: Westminster I

8:00am - 6:00pm

3rd International Workshop on Quantum Compilation

Location: Westminster II

8:00am - 5:50pm

Top Picks in Hardware and Embedded Security

Location: Cotton Creek II

8:15am - 5:00pm

Workshop on Hardware and Algorithms for Learning On-a-Chip

Location: Westminster III

8:30am - 5:30pm

Second Workshop on Open-Source EDA Technology (WOSET)

Location: Westminster IV

9:00am - 7:00pm

International Workshop on Design Automation for Analog and Mixed-Signal Circuits

Location: Cotton Creek I

11:30am - 1:30pm

Workshop Lunch

Location: Legacy Ballroom

1:00 - 6:00pm

1st Workshop on Accelerator Computer-Aided Design

Location: Westminster I

Save the Date for ICCAD 2020
November 2 - 5, 2020 | Hilton San Diego Spa & Resort

Workshop 1W - Workshop on Hardware and Algorithms for Learning On-a-Chip

Time: 8:15am - 5:00pm | Room: Westminster III

Moderator:

Yiran Chen - *Duke Univ.*

Organizers:

Yiran Chen - *Duke Univ.*
Qinru Qiu - *Syracuse Univ.*
Yanzhi Wang - *Northeastern Univ.*
Jishen Zhao - *Univ. of California, San Diego*

In recent years, machine/deep learning algorithms has unprecedentedly improved the accuracies in practical recognition and classification tasks, some even surpassing human-level accuracy. However, to achieve incremental accuracy improvement, state-of-the-art deep neural network (DNN) algorithms tend to present very deep and large models, which poses significant challenges for hardware implementations in terms of computation, memory, and communication. This is especially true for edge devices and portable hardware applications, such as smartphones, machine translation devices, and smart wearable devices, where severe constraints exist in performance, power, and area.

There is a timely need to map the latest complex learning algorithms to custom hardware, in order to achieve orders of magnitude improvement in performance, energy efficiency and compactness. Exemplary efforts from industry and academia include many application-specific hardware designs (e.g., xPU, FPGA, ASIC, etc.). Recent progress in computational neurosciences and nanoelectronic technology, such as emerging memory devices, will further help shed light on future hardware-software platforms for learning on-a-chip.

The overarching goal of this workshop is to explore the potential of on-chip machine learning, to reveal emerging algorithms and design needs, and to promote novel applications for learning. It aims to establish a forum to discuss the current practices, as well as future research needs in the aforementioned fields.

Speakers:

Hsien-Hsin Lee - *Facebook*
Vikas Chandra - *Facebook*
Yu Wang - *Tsinghua Univ.*
Jae-Joon Kim -
Yingyan Lin - *Rice Univ.*
Tinoosh Mohsenin - *Univ. of Maryland*
Jaewoong Sim - *Intel Corp.*
Siddharth Garg - *New York Univ.*
Zhen Zhang - *Univ. of California, Santa Barbara*
Pierre-Emmanuel Gailiardon - *Univ. of Utah*
Catherine Schuman - *Oak Ridge National Laboratory*

Workshop 2W - Hands On Workshop on Machine Learning, Deep Learning and Reinforcement Learning for EDA Developers

Time: 8:00am - 12:00pm | Room: Westminster I

Organizer:

Claudionor Coelho - *Google Inc.*

This workshop covers the basics of machine learning, deep learning and reinforcement learning with examples on how to use this information to build the next generation of EDA tools.

Machine learning is gaining greater acceptance in EDA industry, replacing complicated heuristics and solving problems that were very hard to characterize without a probabilistic mindset, with applications in design, verification, physical implementation and debugging.

This workshop shows how to solve common EDA problems using Naïve Bayes, regression and classification, going to convolutional and recurrent neural networks, and finally presenting reinforcement learning, in a completely hands on manner, so that the attendees will have first hand experience in solving EDA problems with ML/DL/RL formulations. We will also focus on how to debug these problems and understand what goes on when the results do not match what you expected.

During the workshop, we have selected a number of small EDA projects that are going to be executed by the attendees.

1. Regression and classification of parameters in NP complete heuristics
2. Estimating delays of libraries using machine learning and deep learning techniques
3. Using reinforcement learning to solve EDA problems
4. Using recurrent networks to analyze temporal data in EDA

Attendees will receive an executable notebook containing all the material, with examples both in Keras and PyTorch.

At the end of the workshop, attendees will be able to use ML/DL/RL to solve the most challenging problems in EDA, being able to discuss, implement and architect solutions.

Speakers:

Manish Pandey - *Synopsys, Inc.*
Claudionor Coelho - *Google, Inc*

Workshop Lunch

Time: 11:30am - 1:30pm | Room: Legacy Ballroom

Join fellow attendees for lunch in Legacy Ballroom.

Workshop 3W - 1st Workshop on Accelerator Computer-Aided Design

Time: 1:00pm - 6:00pm | Room: Westminster I

Organizers:

Ibrahim Elfadel - *Khalifa Univ.*
Subhasish Mitra - *Stanford Univ.*

1. Topics

This workshop provides a forum to present and discuss the current trends in computer-aided design in support of domain-specific accelerator chips, especially for artificial intelligence and machine learning applications. The workshop will be concerned with the VLSI methodology flow from high-level synthesis to physical verification and performance prediction, particularly in the way it gets impacted with the emerging design paradigms of domain-specific instruction sets, approximate computing, in-memory computing, and stochastic computing. Of particular interest to the workshop are the transformations that VLSI CAD has to undergo to adapt to the post-CMOS technologies when they are considered in the context of accelerator design. The workshop will include, but will not be limited to, the following topics:

- High-level synthesis of machine-learning accelerators
- Design space exploration of domain-specific accelerators
- Tools and methodologies for in-memory computing
- Tools and methodologies for approximate computing
- CAD for emerging accelerator technologies: ReRAM, MRAM, Photonics, etc.
- Tools and methodologies for the post-CNN era
- Tools and methodologies for the testing and verification of accelerator chips.

2. Audience

The workshop will be of interest to all designers and CAD engineers involved in accelerator projects or to academics and graduate students interested in the state of the art of CAD for accelerator chip design.

Speakers:

Yiran Chen - *Duke Univ.*
Priyanka Raina - *Stanford Univ.*
Stelios Diamantidis - *Synopsys, Inc.*
Victor Kravets - *IBM Research*
Danny Bankman - *Stanford Univ.*

Workshop 4W - 3rd International Workshop on Quantum Compilation

Time: 8:00am - 6:00pm | Room: Westminster II

Organizers:

Mathias Soeken - *École Polytechnique Fédérale de Lausanne*
Thomas Haener - *Microsoft*

The workshop aims to bring together researchers from quantum computing, electronic design automation, and compiler construction. Open questions that we anticipate this group to tackle include new methods for circuit synthesis and optimization, optimizations and rewriting, techniques for verifying the correctness of quantum programs, and new techniques for compiling efficient circuits and protocols regarding fault-tolerant and architecture constraints.

The scope of the workshop includes, but not limited to, current hot topics in quantum circuit design such as:

- space-optimizing compilers for reversible circuits
- design-space exploration for automatic code generation from classical HDL specification
- quantum programming languages
- reversible logic synthesis
- technology-aware mapping
- error correction
- optimized libraries (e.g., for arithmetic and Hamiltonian simulation)
- benchmarking of circuits for small and medium scale quantum computers
- quantum and reversible circuit peep-holing and (re)synthesis
- software and tools for all above mentioned topics
- quantum outreach: coding contests, tutorials, education

Speakers:

Alexander Cowtan - *Cambridge Quantum Computing*
Marc Grau Davis - *Univ. of California, Berkeley*
Vadym Kliuchnikov - *Microsoft Corporation*
Raban Iten - *ETH Zurich*
Damien Nguyen - *Huawei Technologies Co., Ltd.*
Eric Peterson - *Rigetti Computing*
Yunong Shi - *Univ. of Chicago*
Seyon Sivarajah - *Cambridge Quantum Computing*
Mitchell Thornton - *Southern Methodist Univ.*

Workshop 5W - International Workshop on Design Automation for Analog and Mixed-Signal Circuits

Time: 9:00am - 7:00pm | Room: Cotton Creek I

Organizers:

Xin Li - *Duke Univ.*
Chandramouli Kashyap - *Intel*
Masanori Hashimoto - *Osaka Univ.*
Jaeha Kim - *Seoul National Univ.*
Scott Little - *Maxim Integrated*
Chris Myers - *Univ. of Utah*
Dejan Nickovic - *Austrian Institute of Technology*

Growing digitization of integrated circuits has contributed to making system-on-chips ever more complex. Yet, a substantial portion of a chip consists of analog and mixed-signal (AMS) circuits that provide critical functionality like clock generation, voltage regulation, interface with the external world, etc. Aggressive scaling of IC technologies as well as advancing the integration of heterogeneous physical domains on chip substantially complicates the design of AMS components. On the one hand, their modeling and design becomes extremely complex. On the other hand, their interplay with the rest of the system-on-chip challenges design, verification and test. These new technology trends bring enormous challenges and opportunities for AMS design automation. This is reflected by an increase in research activity on AMS CAD worldwide. The purpose of this workshop is to bring together academic and industrial researchers from both design and CAD communities to report recent advances and motivate new research topics and directions in this area.

Speakers:

Ronald Rohrer - *Southern Methodist Univ.*
Chandramouli Kashyap - *Intel Corp.*
Mark Po-Hung Lin - *National Chiao Tung Univ.*
Chunfeng Cui - *Univ. of California, Santa Barbara*
Hanbin Hu - *Univ. of California, Santa Barbara*
Duane Boning - *Massachusetts Institute of Technology*
Jun-Yang Lei - *Georgia Institute of Technology*
Thao Dang - *Univ of Grenoble-Alpes France*
Mingjie Liu - *Univ. of Texas at Austin*
Jun Tao - *Fudan Univ.*
Jiahua Li - *Southern Methodist Univ.*

Workshop 6W – Second Workshop on Open-Source EDA Technology (WOSET)

Time: 8:30am - 5:30pm | Room: Westminster IV

Organizers:

Sherief Reda - *Brown Univ.*
Andrew Kahng - *Univ. of California, San Diego*
Sachin Sapatnekar - *Univ. of Minnesota*
Mohamned Shalan - *The American Univ. in Cairo*

The cost and difficulty of IC design in advanced nodes have stifled hardware design innovation and raised unprecedented barriers to bringing new design ideas to the marketplace. Notably, commercial EDA tools have become both expensive and highly complex, as they are aimed at leading-edge, expert users. Unlike the thriving software community, which enjoys a large number of open-source operating systems, compilers, libraries and applications, the hardware community lacks such an ecosystem. This workshop aims to organise the open-source EDA movement. The workshop will bring together EDA researchers who are committed to open-source principles to share their experiences and coordinate efforts towards developing a reliable, fully open-source EDA flow. The workshop will feature presentations and posters that overview existing or under-development open-source tools, designs and technology libraries. A live demo-session for tools in advanced state will be planned. The workshop will feature a panel on the present status and future challenges of open-source EDA, and how to coordinate efforts and ensure quality and interoperability across open-source tools. A cash award will be given for a Best Tool Award.

Submission categories:

- Overview of an existing or under-development open-source EDA tool
- Overview of support infrastructure, such as databases, file formats, and design benchmarks.
- Open-source cloud-based tools
- Position statements (e.g. critical gaps, blockers/obstacles).

http://woset.org

Workshop 7W - Top Picks in Hardware and Embedded Security

Time: 8:00am - 5:30pm | Room: Cotton Creek II

Organizers:

Ramesh Karri - *New York Univ.*
Jeyavijayan Rajendran - *Texas A&M Univ.*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt*
Gang Qu - *Univ. of Maryland, College Park*

The top picks will be selected from conference papers that have appeared in leading hardware security conferences including but not limited to DAC, DATE, ICCAD, HOST, VLSI Design, CHES, ETS, VTS, ITC, IEEE S&P, Euro S&P, Usenix Security, ASIA CCS, NDSS, ISCA, HASP, MICRO, ASPLOS, HPCA, ACSAC and ACM CCS. The top picks will appear in an IEEE Transactions on CAD special section on "Top Picks in Hardware and Embedded Security." To reiterate, top picks will span a gamut of topics in hardware, microarchitecture, and embedded security from leading conferences. Shortlist of papers are invited to the "Top Picks" workshop, collocated with ICCAD 2019. Authors are required to present the paper at the workshop. This is mandatory for consideration to be a top pick. Selected papers are then invited for submission to TCAD Top Picks.
http://toppicksinhardwaresecurity.alari.ch/

Speakers:

Boyou Zhou - *ADI Global Distribution*
Cynthia Sturton - *Univ. of North Carolina*
Hongyu Fang - *George Washington Univ.*
Hoda Naghibijouybari - *Univ. of California, Riverside*
Rui Zhang - *Univ. of North Carolina, Chapel Hill*
Farinaz Koushanfar - *Univ. of California, San Diego*
JV Rajendran - *Texas A&M Univ.*
Bita Darvish Rouhani - *Microsoft Corporation*
Dennis R.E. Gnad - *Karlsruhe Institute of Technology*
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Wenjie Xiong - *Yale Univ.*
Rei Ueno - *Tohoku Univ.*

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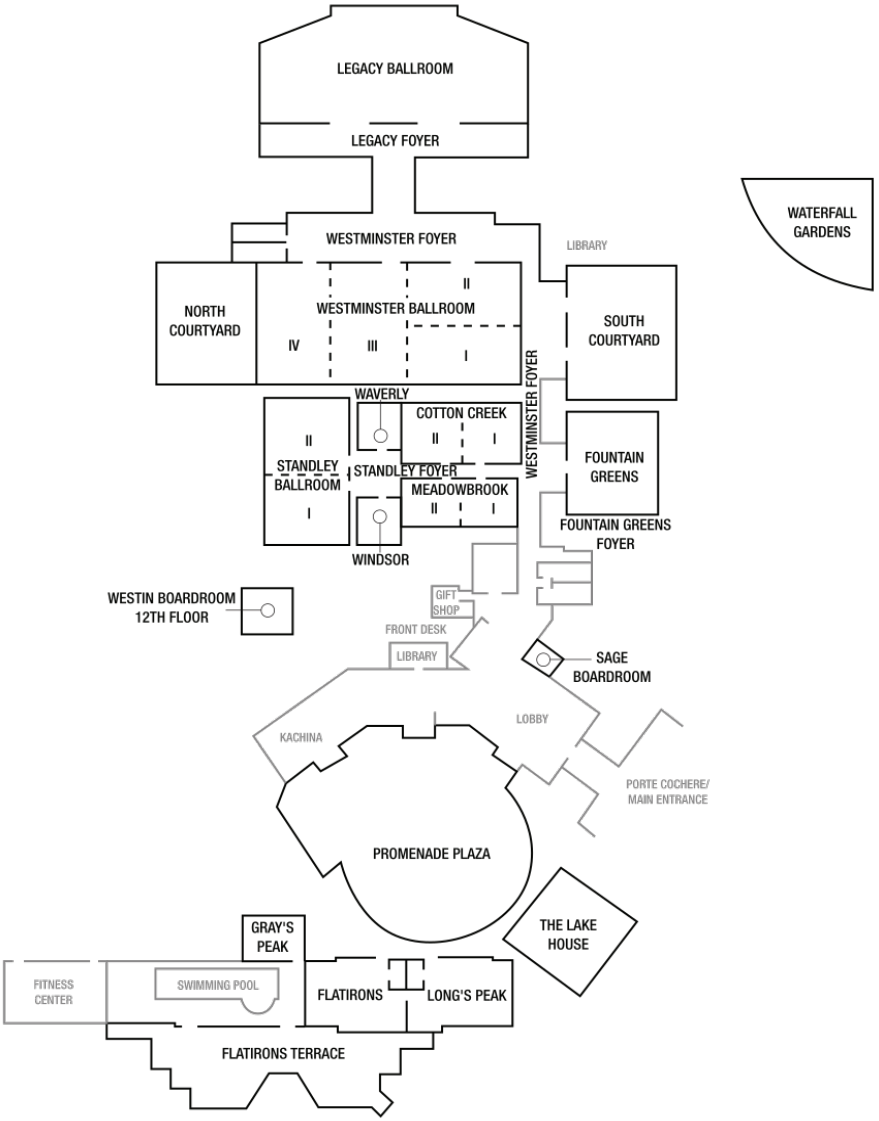

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