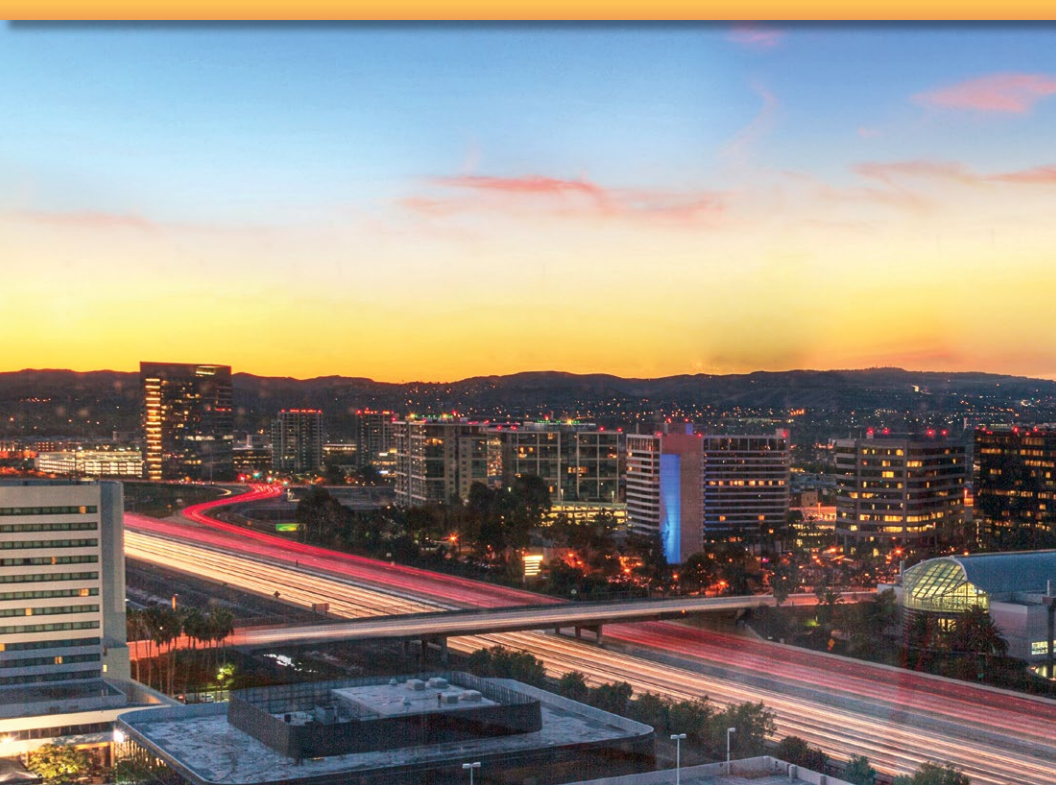
IEEE/ACM ICCAD
2017 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN
36th Edition

CONFERENCE PROGRAM



NOVEMBER 13-16, 2017 • Irvine, CA • ICCAD.COM

IEEE CAS CEDA Association for Computing Machinery sigda

In cooperation with: IEEE

• WELCOME TO THE 36TH ICCAD •

It is with great pleasure that I welcome you to the 36th International Conference on Computer Aided Design. ICCAD is being held for the first time in the city of Irvine, a place that I hold dear.

In this increasingly compute centric world, there is increased demand for electronic design automation with exciting changes and challenges being faced in the way we design, compute, and deploy systems. For over thirty-five years, ICCAD has been a premier forum that has paved the way in creating systems which are fast, small, power efficient, low cost, correct, manufacturable, and reliable. Recent keynotes, papers, tutorials and workshops at ICCAD have addressed novel technologies, the exciting prospects offered by deep learning, newer memories, IoT, approximate computing, and security concerns amongst others. This year's program promises to be equally exciting. Executive committee members, the technical program committee members, volunteers and the staff from MP Associates have worked tirelessly over the last year to prepare a stimulating program.

The program consists of 29 regular paper sessions, with 105 papers drawn from a submission of 399 papers. For over a month, 125 technical program committee members scrutinized the papers, and in a face-to-face meeting selected these papers for inclusion in the program. There are nine special sessions and two embedded tutorials that will be presented during the three days. A record six workshops will be held on the Thursday after the regular conference. Three keynotes will be presented by eminent researchers. The first, on Monday, will be given by Krysta Svore from Microsoft Research titled "Quantum Computing: Revolutionizing computation through quantum mechanics". The Wednesday keynote will be by Todd Austin from The University of Michigan on "How EDA Could Save the World (of Computing)" and the CEDA Invited Keynote will be presented on Tuesday by Maja Matarić from the University of Southern California.

On Thursday, there are six stimulating workshops on a variety of trending topics. These are: Workshop on Hardware and Algorithms for Learning On-a-chip (HALO); International Workshop on Design Automation for Analog and Mixed-Signal Circuits; IEEE/ACM 10th Workshop on Variability Modeling and Characterization; Electronic Design Automation for Quantum Computers; EDA/CAD in the IoT eHealth Era: From Devices to Architectures, Applications, and Data Analytics; and, Workshop on Non-Conventional Approaches to Hard Optimization (NAHO). Note that these workshops have exciting programs in themselves with keynotes from leading exponents.

Once again ICCAD promises to be on the cutting edge of EDA research. We do hope you will be able to join us next year for ICCAD 2018 November 5 -9, Hilton San Diego Resort and Spa, San Diego, CA.

ICCAD 2017 GENERAL CHAIR

Sri Parameswaran

Univ. of New South Wales School of Computer Science & Engineering

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Registration Hours & Location

Location: Salon E Foyer

Monday, November 13	*7:00am – 6:00pm*
Tuesday, November 14	*7:30am – 6:00pm*
Wednesday, November 15	*7:30am – 6:00pm*
Thursday, November 16	*7:00am – 4:00pm*

ICCAD 2017 Mobile App

Review the program, save sessions to your personalized conference schedule, read speakers abstracts, and connect with other attendees using the ICCAD 2017 mobile app provided by Whova, available for download today. Download Whova and search for **ICCAD 2017**.

ANDROID APP ON Google play

Available on the App Store

Proceedings

ICCAD Conference Papers will be delivered electronically online via a username and password.
To access: http://proceedings.iccad.com
Badge ID = Registration ID (on your badge)
Your Email = Email address
Please refer to your registration receipt to access the files you are eligible to view.

Parking Information

Discounted event self-parking of $12.00 per vehicle.

For Speakers & Presenters

SPEAKERS' BREAKFAST

Please attend the day of your presentation!

Location: Salon D

Monday, November 13	*8:00 - 8:45am*
Tuesday, November 14	*7:15 - 8:00am*
Wednesday, November 15	*8:00 - 8:45am*

NEED PRACTICE?

An AV Practice Room will be available in Suite 206, set up with a computer, LCD projector, and screen for you to practice/view your slides before your session.

Location: Suite 206

Monday, November 13	*7:00am - 6:00pm*
Tuesday, November 14	*7:00am - 6:00pm*
Wednesday, November 15	*7:00am - 6:00pm*

ICCAD Social Media

Connect with ICCAD through Twitter @ICCAD. ICCAD will be tweeting hourly updates and conference highlights

Stay Connected during the Conference

ICCAD 2017 is offering internet access in the meeting rooms for attendees.

The Wi-Fi connection is Marriott Conference, password: ICCAD2017.

Conference Management

Our mission is to facilitate networking, education and marketing with efficiency and precision in order to maximize customer experiences, and client profitability and recognition. We accomplish this by having a committed staff of trade show production organizers with the training, technology tools, processes and experience to offer the best service in the industry.

Visit **mpassociates.com** for more information.

• BEST PAPER CANDIDATES & AWARD COMMITTEES •

IEEE/ACM William J. McCalla ICCAD Best Paper Award Candidates

TUESDAY, NOVEMBER 14

4B.2 Speeding Up Crossbar Resistive Memory by Exploiting In-memory Data Patterns
Wen Wen, Lei Zhao, Youtao Zhang, Jun Yang – Univ. of Pittsburgh

5D.1 ATRIUM: Runtime Attestation Resilient Under Memory Attacks
Shaza Zeitouni, Ghada Dessouky, Ahmad Ibrahim, Ahmad-Reza Sadeghi –Technische Univ. Darmstadt
Orlando Arias – Univ. of Central Florida
Dean Sullivan, Yier Jin – Univ. of Florida

6A.4 COMBA: A Comprehensive Model-Based Analysis Framework for High Level Synthesis of Real Applications
Jieru Zhao, Liang Feng, Wei Zhang – Hong Kong Univ. of Science and Technology
Sharad Sinha – Nanyang Technological Univ.
Yun (Eric) Liang – Peking Univ.
Bingsheng He – National Univ. of Singapore

WEDNESDAY, NOVEMBER 15

8A.3 SALT: Provably Good Routing Topology by a Novel Steiner Shallow-Light Tree Algorithm
Genjie Chen, Peishan Tu, Evangeline F.Y. Young – Chinese Univ. of Hong Kong

8C.1 Adaptive Error Recovery in MEDA Biochips Based on Droplet-Aliquot Operations and Predictive Analysis
Zhanwei Zhong, Zipeng Li, Krishnendu Chakrabarty – Duke Univ.

10B.1 Cost-Effective Design of Scalable High-Performance Systems using Active and Passive Interposers
Dylan Stow, Yuan Xie – Univ. of California, Santa Barbara
Taniya Siddiqua, Gabriel H. Loh – Advanced Micro Devices, Inc.

IEEE/ACM William J. McCalla ICCAD Best Paper Award Selection Committee

Naehyuck Chang (Chair) - *Korea Advanced Institute of Science and Technology (KAIST)*
Deming Chen - *Univ. of Illinois Urbana-Champaign*
Azadeh Davoodi - *Univ. of Wisconsin - Madison*
Gang Qu - *Univ. of Maryland, College Park*
Xuan Zeng - *Fudan Univ., China*

Ten-Year Retrospective Most Influential Paper Award Selection Committee

Jason Cong (Chair) - *Univ. of California, Los Angeles*
Duane Boning - *Massachusetts Institute of Technology*
Vivek De - *Intel Corp.*
Ramesh Karri - *New York Univ.*
Tulika Mitra - *National Univ. of Singapore*

ACM SIGDA CADathlon 2017 at ICCAD

Time: 8:00am - 5:00pm | Location: Salons A,B & C

The CADathlon is a challenging, all-day, programming competition focusing on practical problems at the forefront of Computer-Aided Design, and Electronic Design Automation in particular. The contest emphasizes the knowledge of algorithmic techniques for CAD applications, problem-solving and programming skills, as well as teamwork.

In its sixteenth year as the "Olympic games of EDA," the contest brings together the best and the brightest of the next generation of CAD professionals. It gives academia and the industry a unique perspective on challenging problems and rising stars, and it also helps attract top graduate students to the EDA field.

The contest is open to two-person teams of graduate students specializing in CAD and currently full-time enrolled in a Ph.D. granting institution in any country. Students are selected based on their academic backgrounds and their relevant EDA programming experiences. Travel grants are provided to qualifying students. The CADathlon competition consists of six problems in the following areas:

(1) Circuit analysis
(2) Physical design
(3) Logic and behavioral synthesis
(4) System design and analysis
(5) Functional verification
(6) Future technologies (Bio-EDA, Security, etc.)

More specific information about the problems and relevant research papers will be released on the Internet one week prior to the competition. The writers and judges that construct and review the problems are experts in EDA from both academia and industry. At the contest, students will be given the problem statements and example test data, but they will not have the judges' test data. Solutions will be judged on correctness and efficiency. Where appropriate, partial credit might be given. The team that earns the highest score is declared the winner. In addition to handsome trophies, the first and second place teams will receive cash award.

Contest winners will be announced at the ICCAD Opening Session on Monday morning and celebrated at the ACM/SIGDA Dinner and Member Meeting.

The CADathlon competition is sponsored by ACM/SIGDA and several Computer and EDA companies. For detailed contest information and sample problems from last year's competition, please visit the ACM/SIGDA website at http://www.sigda.org/programs/cadathlon.

ORGANIZING COMMITTEE:
Chair, Jingtong Hu, University of Pittsburgh, (jthu@pitt.edu)
Vice Chair, Iris Hui-Ru Jiang, National Taiwan University (huiru.jiang@gmail.com)
Vice Chair, JV Rajendran University of Texas at Dallas (jv.ee@utdallas.edu)

Sponsored by: Association for Computing Machinery

• MONDAY SCHEDULE •

8:45 - 9:15am

Opening Session & Awards

Location: Salon E

9:15 - 10:00am

Keynote: Quantum Computing: Revolutionizing Computation Through Quantum Mechanics

Dr. Krysta Svore - Microsoft Research | Location: Salon E

10:00 - 10:30am

Coffee Break

Location: Salon E Foyer

10:30am - 12:30pm

Session 1A: Advanced Caching and In-Memory Processing

Location: Salon E

Session 1B: Camouflaging and Logic Encryption

Location: Salons A & B1

Session 1C: Improving Manufacturability – From Design through Mask Generation

Location: Salons B2 & C

Special Session 1D: Cross-Layer Efforts for Combating Computationally Hard Problems

Location: Newport & Marina

11:30am - 1:30pm

ACM Student Research Competition Poster Session

Location: SSR

Sponsored by:

STUDENT RESEARCH COMPETITION

Association for Computing Machinery

Advancing Computing as a Science & Profession

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12:45 - 1:45pm

Lunch

Location: Salon D

• MONDAY SCHEDULE •

2:00 - 4:00pm

Session 2A: Modern Techniques for Challenging Verification Problems
Location: Salon E

Session 2B: Physical Attacks: Implementation, Simulation, and Synthesis
Location: Salons A & B1

Special Session 2C: 3D Integration Beyond TSVs
Location: Salons B2 & C

Special Session 2D: AI for CPS: Machine Learning for Intelligent and Secure Cyber-Physical Systems
Location: Newport & Marina

4:00 - 4:30pm

Coffee Break
Location: Salon E Foyer

4:30 - 6:00pm

Session 3A: New Advances in Circuit Simulation
Location: Salon E

Session 3B: Intelligent Control on Wheels
Location: Salons A & B1

Session 3C: Next Generation System Level Design Methods
Location: Salons B2 & C

Special Session 3D: 2017 CAD Contest
Location: Newport & Marina

Sponsored by:

6:00 - 6:20pm

EDA Megatrends: Enabling a Wide and Dynamic Range of Applications
Location: Salons B2 & C

6:20 - 6:50pm

Sponsored by:

Networking Reception
Location: Salon E Foyer

6:30 - 8:00pm

ACM Student Research Competition Technical Presentations
Location: Salon E

Sponsored by:

Opening Session, Awards, and Keynote

Time: 8:45am - 10:00am | Location: Salon E

Kick off the conference with opening remarks from the ICCAD Executive Committee members and hear the highlights of the conference. The IEEE/ACM William J. McCalla ICCAD Best Paper award will be announced along with other award presentations from IEEE and ACM.

IEEE/ACM WILLIAM J. MCCALLA ICCAD BEST PAPER AWARD

This award is given in memory of William J. McCalla for his contributions to ICCAD and his CAD technical work throughout his career.

Front-End Award:

6A.4 COMBA: A Comprehensive Model-Based Analysis Framework for High Level Synthesis of Real Applications
Jieru Zhao, Liang Feng, Wei Zhang – Hong Kong Univ. of Science and Technology
Sharad Sinha – Nanyang Technological Univ.
Bingsheng He – National Univ. of Singapore

Back-End Award:

8A.3 SALT: Provably Good Routing Topology by a Novel Steiner Shallow-Light Tree Algorithm
Genjie Chen, Peishan Tu, Evangeline F.Y. Young – Chinese Univ. of Hong Kong

TEN YEAR RETROSPECTIVE MOST INFLUENTIAL PAPER AWARD

This award is being given to the paper judged to be the most influential on research and industrial practice in computer-aided design over the ten years since its original appearance at ICCAD.

2008 Paper Titled: Lightweight Secure PUFs
Mehrdad Majzoobi, Farinaz Koushanfar - Rice Univ., Miodrag Potkonjak- Univ. of California, Los Angeles
ICCAD 2008, pp. 670 – 673

2017 ACM/SIGDA PIONEER AWARD

Mary Jane Irwin, Emeritus Evan Pugh University Professor in Computer Science and Engineering - *Pennsylvania State University*
For contributions to VLSI architectures, electronic design automation and community mentorship.

IEEE CEDA OUTSTANDING SERVICE AWARD

Dr. Frank Liu - *IBM Research Austin*
For outstanding service to the EDA community as ICCAD General Chair in 2016.

IEEE CEDA ERNEST S. KUH EARLY CAREER AWARD

Ayse Coskun - *Boston University*
For sustained and outstanding contributions to energy-efficient system-level design, including temperature-aware design and management, 3D-stacked system design, and management of large-scale computing systems.

ACM/SIGDA CADATHALON

Introduction of the 2017 winners.

Keynote: Quantum Computing: Revolutionizing Computation Through Quantum Mechanics

Time: 9:15am - 10:00am | Location: Salon E

Speaker:

Dr. Krysta Svore - *Microsoft Research*

In 1981, Richard Feynman proposed a device called a "quantum computer" to take advantage of the laws of quantum physics to achieve computational speed-ups over classical methods. Quantum computing promises to revolutionize how and what we compute. Over the course of three decades, quantum algorithms have been developed that offer fast solutions to problems in a variety of fields including number theory, optimization, chemistry, physics, and materials science. Quantum devices have also significantly advanced such that components of a scalable quantum computer have been demonstrated; the promise of implementing quantum algorithms is in our near future. I will attempt to explain some of the mysteries of this disruptive, revolutionary computational paradigm and how it will transform our digital age.

Biography: Dr. Krysta Svore is a Principal Researcher and Research Manager at Microsoft Research, where she leads the Quantum Architectures and Computation (QuArC) group. Dr. Svore joined Microsoft Research in 2006 and started the QuArC group in 2010. Her research focuses on the development and implementation of quantum algorithms, including the design of a scalable, fault-tolerant software architecture for translating a high-level quantum program into a low-level, device-specific quantum implementation. She has also developed techniques for protecting quantum computers from noise, including methods of quantum error correction, establishment of noise thresholds, and the development of improved decoders. She spent her early years at Microsoft developing machine-learning methods for web applications, including ranking, classification, and summarization algorithms. Her work in machine learning has expanded to include quantum algorithms for improve machine learning methods. Dr. Svore was recently appointed as a member of the Advanced Scientific Computing Advisory Committee of the Department of Energy and chaired the 2017 Quantum Information Processing Conference. Svore received an ACM Best of 2013 Notable Article award. In 2010, she was a member of the winning team of the Yahoo! Learning to Rank Challenge. Dr. Svore is honored as a Kavli Fellow of the National Academy of Sciences. She is a Senior Member of the Association for Computing Machinery (ACM), serves as a representative for the Academic Alliance of the National Center for Women and Information Technology (NCWIT), and is an active member of the American Physical Society (APS). Dr. Svore has authored over 65 papers and has filed over 20 patents. She received her PhD in computer science with highest distinction from Columbia University and her BA from Princeton University in Mathematics with a minor in Computer Science and French.

Session 1A - Advanced Caching and In-Memory Processing

Time: 10:30am - 12:30pm | Location: Salon E

Moderator:

Miroslav N. Velev - *Aries Design Automation, LLC*

This session presents four papers to advance the design of cache memories and take advantage of in-memory processing to accelerate applications. The first paper builds an efficient hybrid cache for multicore processors by exploiting value locality. The second paper explores cache bypassing and partitioning on GPUs. The third paper proposes a virtual persistent cache concept to remedy the long latency in Host-Aware Shingled Magnetic Recording (HA-SMR) drives. The final paper present a memristor-based in-memory processing for accelerating object recognition tasks.

1A.1 Leveraging Value Locality for Efficient Design of a Hybrid Cache in Multicore Processors
Mohammad Arjomand - *Georgia Institute of Technology*
Amin Jadidi, Mahmut Kandemir, Chita Das - *Pennsylvania State Univ.*

1A.2 Exploring Cache Bypassing and Partitioning for MultiTasking on GPUs
Yun (Eric) Liang, Xiuhong Li, Xiaolong Xie - *Peking Univ.*

1A.3 Virtual Persistent Cache: Remedy the Long Latency Behavior of Host-Aware Shingled Magnetic Recording Drives
Ming-Chang Yang - *Chinese Univ. of Hong Kong, Chinese Univ. of Hong Kong & Academia Sinica and National Taiwas Univ.*
Yuan-Hao Chang - *Academia Sinica*
Fenggang Wu - *Univ. of Minnesota, Twin Cities*
Tei-Wei Kuo - *National Taiwan Univ. & Academia Sinica*
David H.C. Du - *Univ. of Minnesota, Twin Cities*

1A.4 ORCHARD: Visual Object Recognition Accelerator Based on Approximate In-Memory Processing
Yeseong Kim, **Mohsen Imani**, Tajana Rosing - *Univ. of California, San Diego*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 1B - Camouflaging and Logic Encryption

Time: 10:30am - 12:30pm | Location: Salons A & B1

Moderator:

Fareena Saqib - *Florida Institute of Technology*

This session covers camouflaging and logic encryption attacks and countermeasures. Topics include attacks on decamouflaging sequential circuits without scan access, SAT-based attack on cyclic logic encryption, and a variety of novel countermeasure techniques for storing obfuscated master keys with quantifiable security and obfuscation of interconnects.

1B.1 Reverse Engineering Camouflaged Sequential Circuits Without Scan Access
Mohamed El Massad, Siddharth Garg - *New York Univ.*
Mahesh Tripunitara - *Univ. of Waterloo*

1B.2 Obfuscating the Interconnects: Low-Cost and Resilient Full-Chip Layout Camouflaging
Satwik Patnaik - *New York Univ.*
Mohammed Ashraf, Johann Knechtel, Ozgur Sinanoglu - *New York Univ., Abu Dhabi*

1B.3 CycSAT: SAT-Based Attack on Cyclic Logic Encryptions
Hai Zhou, Ruifeng Jiang, Shuyu Kong - *Northwestern Univ.*

1B.4 Threshold-based Obfuscated Keys with Quantifiable Security Against Invasive Readout
Shahrzad Keshavarz, Daniel Holcomb - *Univ. of Massachusetts, Amherst*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 1C - Improving Manufacturability -- From Design through Mask Generation

Time: 10:30am - 12:30pm | Location: Salons B2 & C

Moderator:

Srikanth Venkataraman - *Intel Corp.*

Assuring manufacturability of present and future technologies and designs is crucial, and multiple methods are needed to achieve this. First, designs must better comprehend process constraints. The first paper effectively factors in implant-area constraints in multi-Vt designs, during mixed-cell-height place and route. Second, potential layout hotspots must be efficiently identified in a candidate design. The second paper achieves cluster count reduction during layout pattern classification using proposed heuristics. Third, manufacturable multi-patterned masks must be generated, and the third paper proposes a novel framework to simultaneously optimize layout decomposition and mask corrections. Finally, future technologies and designs will require joint multi-objective consideration of alternatives, as presented in the last paper.

1C.1 Mixed-Cell-Height Detailed Placement Considering Complex Minimum-Implant-Area Constraints
Yen-Yi Wu, Yao-Wen Chang - *National Taiwan Univ.*

1C.2 Blockage-Aware Terminal Propagation for Placement Wirelength Minimization
Sheng-Wei Yang, Yao-Wen Chang - *National Taiwan Univ.*
Tung-Chieh Chen - *Maxeda Technology, Inc.*

1C.3 A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization
Yuzhe Ma - *Chinese Univ. of Hong Kong*
Jhih-Rong Gao, Jian Kuang, Jin Miao - *Cadence Design Systems, Inc.*
Bei Yu - *Chinese Univ. of Hong Kong*

1C.4 IR-drop Aware Design & Technology Co-Optimization for N5 Node with Different Device and Cell Height Options
Luca Mattii - *Technische Univ. Braunschweig & Cadence Design systems, Inc.*
Dragomir Milojevic, Peter Debacker, Yasser Sherazi - *IMEC*
Mladen Berekovic - *Technische Univ. Braunschweig*
Praveen Raghavan - *IMEC*

All speakers are denoted in bold | * denotes Best Paper Candidate

Special Session 1D: Cross-Layer Efforts for Combating Computationally Hard Problems

Time: 10:30am - 12:30pm | Location: Newport & Marina

Moderator:

Michael Niemier - *Univ. of Notre Dame*

Organizers:

X. Sharon Hu - *Univ. of Notre Dame*
Michael Niemier - *Univ. of Notre Dame*

Computationally hard (i.e., NP-hard) problems are quintessential to many electronic design automation problems, and are also at the heart of many decision, scheduling, error-correction and security applications. Their NP-hard nature makes solving them extremely resource demanding, either in terms of computation time or hardware components or energy. Most of the efforts on improving solvers for such problems aim at developing more effective search algorithms with the understanding that these algorithms would eventually be implemented on modern general-purpose digital computing platforms such as multi-core or many-core processors or application specific digital circuits.

However, with Moore's Law coming to an end, exploring novel computational paradigms (e.g., quantum computing and neuromorphic computing) supported by emerging devices and alternative circuit styles is more imperative than ever. Recently there has been increased interest in cross-layer efforts for designing analog, or mixed-signal solvers for some specific NP-hard optimization problems based on continuous-time dynamical systems. Furthermore, a number of researchers are investigating approaches that exploit intrinsic properties exhibited by certain beyond-CMOS devices to solve NP-hard optimization problems.

In this special session, we highlight four cross-layer research efforts targeted at solving NP-hard problems (e.g., satisfiability, graph coloring, etc.) using computational primitives that (i) exploit spatio-temporal dynamics of coupled systems, and (ii) avoid Boolean abstraction in order to achieve high efficiencies with respect to energy and performance. The speakers will present a range of new solver implementations including mixed signal circuits based on conventional transistors, oscillators derived from phase transitions in correlated electron materials, and spin-based devices. While all approaches offer paths toward speedups and/or improvements in energy efficiencies of several orders of magnitude when compared to state-of-the-art approaches, challenges exist that the members of the EDA community are uniquely positioned to address, e.g., managing routing complexity as problem sizes scale, addressing noise tolerance, etc.

1D.1 Solving Constraint Satisfaction Problems: From Neural Dynamics to Silicon Chips
Hesham Mostafa - *Univ. of California, San Diego*
Giacomo Indiveri - *Univ. of Zurich*
Lorenz K. Muller - *ETH Zurich*

1D.2 An Analog SAT Solver based on a Deterministic Dynamical System
Xunzhao Yin, Zoltan Toroczkai, **X. Sharon Hu** - *Univ. of Notre Dame*

1D.3 Connecting Spectral Techniques for Graph Coloring and Eigen Properties of Coupled Dynamics: A Pathway for Solving Combinatorial Optimizations
Abhinav Parihar - *Georgia Institute of Technology*
Matthew Jerry, Nikhil Shukla, Suman Datta - *Univ. of Notre Dame*
Arijit Raychowdhury - *Georgia Institute of Technology*

1D.4 Spin-Device Based Circuits for Computationally Hard Problems
Kerem Y Camsari, Rafatul Faria, Brian M. Sutton, Supriyo Datta - *Purdue Univ.*

All speakers are denoted in bold | * denotes Best Paper Candidate

ACM Student Research Competition Poster Session

Time: 11:30am - 1:30pm | Location: SSR

Sponsored by Microsoft Research, the ACM Student Research Competition (SRC) is an internationally recognized venue enabling undergraduate and graduate students who are members of ACM and ACM SIGDA to:

- Experience the research world—for many undergraduates this is a first!
- Share research results and exchange ideas with other students, judges, and conference attendees.
- Rub shoulders with academic and industry luminaries.
- Understand the practical applications of their research.
- Perfect their communication skills.
- Receive prizes and gain recognition from ACM, and the greater computing community.

ACM SRC has three rounds:

(1) abstract review
(2) poster session (this session)
(3) technical presentation

In the first round, 2-page research abstracts are evaluated by EDA experts from academia and industry to select participants for the second round (this session). For the ACM SRC at ICCAD 2016 competition, 20 participants were selected to present their research at ICCAD.

The posters are evaluated by EDA experts to select up to 5 participants in graduate and undergraduate categories to advance to the final round (technical presentation round). Students are expected to discuss their work with judges. Each judge will rate the student's visual presentation based on the criteria of uniqueness of the approach, the significance of the contribution, visual presentation, and quality of presentation.

More details can be found at: sigda.org/src

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All speakers are denoted in bold | * denotes Best Paper Candidate

Lunch

Time: 12:45pm - 1:45pm | Location: Salon D

Join fellow attendees for lunch in Salon D.

Session 2A - Modern Techniques for Challenging Verification Problems

Time: 2:00pm - 4:00pm | Location: Salon E

Moderator:
Ian Harris - *Univ. of California, Irvine*

This session presents a range of SAT-based techniques to conquer major challenges in pre-silicon, post-silicon, repair and functional timing. The first paper proposes a novel approach for SAT-based model checking using approximations. The second paper introduces an approach for improving the coverage of electrical bugs in post silicon validation. The third paper formulates the problem of patching sequential circuits in the presence of retiming and resynthesis. The final paper in the session accelerates functional timing analysis by removing redundancies from the CNF formula that describes the functional and timing constraints on a path.

2A.1 Safety Model Checking with Complimentary Approximations
Jianwen Li - *Rice Univ. & East China Normal Univ.*
Shufang Zhu, Yueling Zhang, Geguang Pu - *East China Normal Univ.*
Moshe Vardi - *Rice Univ.*

2A.2 An Automated SAT-Based Method for the Design of On-Chip Bit-Flip Detectors
Pouya Taatizadeh, **Nicola Nicolici** - *McMaster Univ.*

2A.3 Sequential Engineering Change Order Under Retiming and Resynthesis
Nian-Ze Lee - *National Taiwan Univ.*
Victor Kravets - *IBM Corp.*
Jie-Hong Roland Jiang - *National Taiwan Univ.*

2A.4 Accelerating Functional Timing Analysis with Encoding Duplication Removal and Redundant State Propagation
Denny C.-Y. Wu, Pin-Ru Jhao, Charles H.-P. Wen - *National Chiao Tung Univ.*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 2B - Physical Attacks: Implementation, Simulation, and Synthesis

Time: 2:00pm - 4:00pm | Location: Salons A & B1

Moderator:

Sheldon Tan - *Univ. of California, Riverside*

Physical attacks on complex systems require ingenious attack implementations. Resilience against such attacks relies on efficient simulation, synthesis, and verification tools. This session starts with an efficient, high-resolution simulation method to automate electromagnetic side-channel leakage in cryptographic hardware. It also presents two papers on novel physical attacks: (1) fault injection attack on a deep neural network to disrupt the classification result and (2) a cache bank timing attack on AES to extract secret keys. Finally, the session introduces a new tool that adopts formal methods to synthesize circuitry for tracking timing flows.

2B.1 Efficient Simulation of EM Side-Channel Attack Resilience
Amit Kumar, Cody Scarborough, Ali Yilmaz, Michael Orshansky - *Univ. of Texas at Austin*

2B.2 Fault Injection Attack on Deep Neural Network
Yannan Liu, Lingxiao Wei, Bo Luo, **Qiang Xu** - *Chinese Univ. of Hong Kong*

2B.3 A Novel Cache Bank Timing Attack
Zhen Hang Jiang, Yunsi Fei - *Northeastern Univ.*

2B.4 Clepsydra: Modeling Timing Flows in Hardware Designs
Armaiti Ardeshiricham, Wei Hu, Ryan Kastner - *Univ. of California, San Diego*

Special Session 2C: 3D Integration Beyond TSVs

Time: 2:00pm - 4:00pm | Location: Salons B2 & C

Moderator:

Mark Yao - *Boeing Corporation*

Organizers:

Krishnendu Chakrabarty - *Duke Univ.*
Sheldon Tan - *UC Riverside*
Mehdi Tahoori - *Karlsruhe Institute of Technology (KIT)*

The continued down-scaling of nanoscale integrated circuits (IC) presents significant challenges with respect to manufacturability, reliability, cost, and power consumption. Recent work has therefore advanced the concept of "upscaling" through three-dimensional (3D) stacked ICs. Industry trends highlight the viability of 3D integration in actual products (e.g., the AMD Radeon R9 Fury X graphics card, Xilinx Virtex-7 2000T/H580T and Ultra-scale FPGAs). Flash memory vendors have announced multiple layers of memory in a single package, e.g., as many as 32 and 48 layers of Flash memory (Toshiba BiCS). Moore's law is now entering a new phase characterized by vertical integration ("3D Power Scaling" in the ITRS2.0 2015 report).

Special Session 2C: 3D Integration Beyond TSVs (Cont.)

Today's 3D integration technology is primarily based on die/wafer stacking since it does not require major changes to the existing fabrication flow or retooling of fabrication processes. However, the increase in fabrication cost (foundries report that TSV processing adds 10% to the wafer cost), the keep-out-zone (KOZ) required for TSVs, and limitations on the die alignment precision impose limits on the device integration density that can be achieved using TSV-based 3D stacking. For example, it has been reported that a minimum KOZ of 3 µm is required for ICs fabricated at the 20 nm technology node and the die alignment precision is imited to 0.5 µm. Newer technologies for 3D integration are therefore being explored to exploit up-scaling to the fullest possible extent.

This special session will present a vision into the future of 3D integration. Speakers will address emerging directions in 3D integration techniques and challenges beyond traditional TSV-based 3D integration. Specific topics to be covered include monolithic 3D integration, long-term reliability assessment and design for reliability of interconnects in next-generation 3D ICs, wireless 3D interconnects, and on-chip silicon-photonics 3D interconnects. Each presentation will provide technology overview, describe design, test, and reliability challenges, and highlight recent advances.

Attendees will get holistic insights through lively presentations that will encapsulate the latest cutting-edge research in these emerging topics. This session will inform and inspire academic researchers as well as industry practitioners towards new innovations in these directions.

2C.1 Design Automation and Testing of Monolithic 3D ICs: Opportunities, Challenges, and Solutions
Kyungwook Chang - *Georgia Institute of Technology*
Abhishek Abhishek Koneru, Krishnendu Chakrabarty - *Duke Univ.*
Sung-Kyu Lim - *Georgia Institute of Technology*

2C.2 Leveraging Recovery Effect to Reduce Electromigration Degradation in Power/Ground TSV
Shengcheng Wang - *Karlsruhe Institute of Technology*
Zeyu Sun - *Univ. of California, Riverside*
Yuan Cheng - *Shanghai Jiaotong Univ.*
Sheldon Tan - *Univ. of California, Riverside*
Mehdi Tahoori - *Karlsruhe Institute of Technology*

2C.3 Energy-Efficient and Robust 3D NoCs with Contactless Vertical Links
Srinivasan Gopal, Sourav Das, **Partha Pratim Pande**, Deuk Heo - *Washington State Univ.*

2C.4 Thermal-Sensitive Design and Power Optimization for a 3D Torus-Based Optical NoC
Kang Yao, Yaoyao Ye - *Shanghai Jiao Tong Univ.*
Sudeep Pasricha - *Colorado State Univ.*
Jiang Xu - *Hong Kong Univ. of Science and Technology*

All speakers are denoted in bold | * denotes Best Paper Candidate

Special Session 2D: AI for CPS: Machine Learning for Intelligent and Secure Cyber-Physical Systems

Time: 2:00pm - 4:00pm | Location: Newport & Marina

Moderator:

Deming Chen - *Univ. of Illinois, Urbana-Champaign*

Organizer:

Qi Zhu - *Univ. of California, Riverside*

With the proliferation of sensor data and advancement of processing power, machine learning techniques have shown great promise in cyber-physical systems (CPS) applications. These techniques are particularly effective for analyzing, controlling and optimizing complex CPS where the system dynamics and surrounding environment are hard to capture; however, applying them in practical systems often faces challenges from resource and timing constraints as well as reliability, predictability and security requirements. In this session, the four talks will introduce the application of machine learning techniques across a variety of CPS domains, including aerospace, agriculture, petroleum, and buildings and grid. They will demonstrate the effectiveness of using learning techniques, in particular those based on deep neural networks, to achieve artificial intelligence in CPS. They will discuss the encountered challenges in meeting system security, reliability and resource requirements, and present promising solutions.

2D.1 VoCaM: Visualization Oriented Convolutional Neural Network Acceleration on Mobile Systems
Zhuwei Qin, Zirui Xu - *George Mason Univ.*
Yiran Chen - *Duke Univ.*
Xiang Chen - *George Mason Univ.*

2D.2 An Autonomous Precision Irrigation Through Neural Reinforcement Learning
Jiang Hu - *Texas A&M Univ.*

2D.3 Offshore Oil Spill Monitoring and Detection: Improving Risk Management for Offshore Petroleum Cyber-Physical Systems
Xiaodao Chen, Dongmei Zhang, Lizhe Wang, Yuewei Wang - *China Univ. of Geosciences*
Albert Zomaya - *The Univ. of Sydney*
Shiyan Hu - *Michigan Technological Univ.*

2D.4 Deep Reinforcement Learning: Framework, Applications, and Embedded Implementations
Hongjia Li - *Syracuse Univ.*
Tianshu Wei - *Univ. of California, Riverside*
Ruizhe Cai - *Syracuse Univ.*
Qi Zhu - *Univ. of California, Riverside*
Yanzhi Wang - *Syracuse Univ.*

Session 3A - New Advances in Circuit Simulation

Time: 4:30pm - 6:00pm | Location: Salon E

Moderator:

Xin Li - *Duke Univ.*

With increased complexity of circuits and systems, efficient simulation continues to be critical yet challenging. The first paper describes an efficient methodology for sensitivity analysis of an event-driven objective function. The second paper proposes a novel algorithm combining exponential integrators and Krylov subspace algorithms for nonlinear circuit simulation. The final paper develops a fast approach for electromigration analysis of multi-branch interconnect trees.

3A.1 DAGSENS: Directed Acyclic Graph Based Direct and Adjoint Transient Sensitivity Analysis for Event-Driven Objective Functions
Karthik Aadithya, Eric Keiter, Ting Mei - *Sandia National Laboratories*

3A.2 Exploring the Exponential Integrators with Krylov Subspace Algorithms for Nonlinear Circuit Simulation
Xinyuan Wang - *Univ. of California, San Diego*
Hao Zhuang - *ANSYS, Inc.*
Chung-Kuan Cheng - *Univ. of California, San Diego*

3A.3 Fast Physics-based Electromigration Analysis for Multi-Branch Interconnect Trees
Xiaoyi Wang, Yan Yan, Jian He - *Beijing Advanced Innovation Center for Future Internet Technology & Beijing Univ. of Technology*
Sheldon X.-D. Tan, Chase Cook - *Univ. of California, Riverside*
Shengqi Yang - *Beijing Advanced Innovation Center for Future Internet Technology & Beijing Univ. of Technology*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 3B - Intelligent Control on Wheels

Time: 4:30pm - 6:00pm | Location: Salons A & B1

Moderator:

Umit Ogras - *Arizona State Univ.*

This session focuses on intelligent control techniques to improve automotive performance parameters such as delay, path tracking, and battery capacity.

The first two papers integrate Model Predictive Control in automotive use-cases and demonstrate message delay prediction in Controller Area Network and dynamic model reconfiguration in fine-grain and coarse-grain safety scenarios. The third paper presents an adaptive and cooperative quality-aware control for automotive cyber-physical systems.

3B.1 **Online Message Delay Prediction for Model Predictive Control over Controller Area Network**
Amith Kaushal Rao, Haibo Zeng - *Virginia Polytechnic Institute and State Univ.*

3B.2 **Hybrid State Machine Model for Fast Model Predictive Control: Application to Path Tracking**
Maral Amir, Tony Givargis - *Univ. of California, Irvine*

3B.3 **ACQUA: Adaptive and Cooperative Quality-Aware Control for Automotive Cyber-Physical Systems**
Korosh Vatanparvar, Mohammad Abdullah Al Faruque - *Univ. of California, Irvine*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 3C - Next Generation System Level Design Methods

Time: 4:30pm - 6:00pm | Location: Salons B2 & C

Moderator:

Christopher Harris - *Auburn Univ.*

This session explores the application of emerging tools and techniques to challenges in system level computer design. We feature the adoption of machine learning techniques to hardware design space exploration, the use of hardware construction languages (HCLs) to promote design reuse for increasingly heterogeneous digital designs, and the automatic parallelization of applications for NoC-based multicore architectures.

3C.1 Cross-Program Design Space Exploration by Ensemble Transfer Learning
Dandan Li, Shuzhen Yao - *Beihang Univ.*
Senzhang Wang - *Nanjing Univ. of Aeronautics and Astronautics*
Ying Wang - *Chinese Academy of Sciences*

3C.2 Hardware Reusability is FIRRTL Ground: Hardware Construction Languages, Compiler Frameworks, and Transformations
Adam Izraelevitz, Jack Koenig, Patrick S. Li, Richard Lin, Angie Wang, Albert Magyar, Donggyu Kim, Colin Schmidt, Chick Markley, Jim Lawson, Jonathan Bachrach - *Univ. of California, Berkeley*

3C.3 A Load Balancing Inspired Optimization Framework for Exascale Multicore Systems: A Complex Networks Approach
Yao Xiao, Yuankun Xue, Shahin Nazarian, Paul Bogdan - *Univ. of Southern California*

All speakers are denoted in bold | * denotes Best Paper Candidate

Special Session 3D: 2017 CAD Contest at ICCAD

Time: 4:30pm - 6:00pm | Location: Newport & Marina

Moderator:

Myung-Chul Kim - *IBM Corp.*

Organizers:

Myung-Chul Kim - *IBM Corp.*
Shih-Hsu Huang - *Chung Yuan Christian Univ.*
Rung-Bin Lin - *Yuan Ze Univ.*
Shigetoshi Nakatake - *The Univ. of Kitakyushu*

The CAD Contest at ICCAD is a challenging, multi-month R&D competition, focusing on modern and practical problems at the forefront of Electronic Design Automation (EDA). In its sixth year, the 2017 CAD Contest at ICCAD is among the premier worldwide academic programming contests, attracting 122 teams from 10 different regions/countries. This year, three contest problems in the areas of ECO logic synthesis, ECO routing and placement legalization for the advanced nodes are called for competition. This session gives an overview of the 2017 CAD Contest, presents the three contest problems and benchmarks, and announces the winners. It also provides a venue for the top-performing teams to showcase their key ideas via short video presentations. Based on the momentum accumulated by EDA contests, a talk on OpenDesign Flow Database 2.0 concludes the session by reporting recent progress towards building an academic infrastructure for VLSI design and EDA research.

3D.1 Overview of the 2017 CAD Contest at ICCAD

Myung-Chul Kim - *IBM Corp.*
Shih-Hsu Huang - *Chung Yuan Christian Univ.*
Rung-Bin Lin - *Yuan Ze Univ.*
Shigetoshi Nakatake - *Univ. of Kitakyushu*

3D.2 ICCAD-2017 CAD Contest in Resource-Aware Patch Generation

Ching-Yi Huang, Chih-Jen Hsu, Chi-An Wu - *Cadence Taiwan, Inc.*
Kei-Yong Khoo - *Cadence Design Systems, Inc.*

3D.3 ICCAD-2017 CAD Contest in Net Open Location Finder with Obstacles

Kai-Shun Hu, Ming-Jen Yang, Yu-Hui Huang, Bing-Yi Wong, Cindy Shen - *Synopsys Taiwan Co., Ltd.*

3D.4 ICCAD-2017 CAD Contest in Multi-Deck Standard Cell Legalization and Benchmarks

Nima Karimpour Darav - *Microsemi Corporation*
Ismail Bustany - *Mentor, A Siemens Business*
Andrew Kennings - *Univ. of Waterloo*
Ravi Mamidi - *Mentor, A Siemens Business*

3D.5 DATC RDF: Robust Design Flow Database

Jinwook Jung - *Korea Advanced Inst. of Science and Technology*
Pei-Yu Lee, Yan-Shiun Wu - *National Chiao Tung Univ.*
Nima Karimpour Darav - *Microsemi Corporation*
Iris Hui-Ru Jiang - *National Taiwan Univ.*
Victor N. Kravets - *IBM T.J. Watson Research Center*
Laleh Behjat - *Univ. of Calgary*
Yih-Lang Li - *National Chiao Tung Univ.*
Gi-Joon Nam - *IBM T.J. Watson Research Center*

Sponsored by:

All speakers are denoted in bold | * denotes Best Paper Candidate

Additional Meeting: EDA Megatrends: Enabling a Wide and Dynamic Range of Applications

Time: 6:00pm - 6:20pm | Location: Salons B2 & C

Speaker:

Alessandra Nardi - *Cadence Design Systems, Inc.*

Every industry follows trends, which are defined by the technological progress, society, culture. EDA industry is no exception here. However, EDA is a supplier to a much larger semiconductors industry serving itself a broad spectrum of applications, from consumer to automotive, from transistor to system-level. The challenge for EDA is to translate the markets needs into technology trends to be addressed or exploited to support the semiconductor industry and their customers. This presentation will have a brief overview of such challenges and opportunities and focus on few cases as example (e.g., enabling the fast expanding, high demand automotive market).

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Networking Reception

Time: 6:20pm - 6:50pm | Location: Salon E Foyer

Whatever your goal, networking receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day's presentations with the conference presenters. All attendees are invited.

Sponsored by: cadence® ACADEMIC NETWORK

Additional Meeting - ACM Student Research Competition Technical Presentations

Time: 6:30pm - 8:00pm | Location: Salon E

The ACM Student Research Competition allows both graduate and undergraduate students to discuss their research with student peers, as well as academic and industry researchers, in an informal setting, while enabling them to attend ICCAD.

This session is the final round of ACM SRC at ICCAD 2017. Each student will present for 10 minutes, followed by a 5-minute question and answer period. This session will be attended by the evaluators and any interested conference attendees. The top three winners in each category will be chosen based on these presentations.

The undergraduate and graduate finalists will be eligible to compete in the ACM SRC Grand Finals to be held in June 2018. More details can be found at: sigda.org/src

Sponsored by: STUDENT RESEARCH COMPETITION; Association for Computing Machinery, Advancing Computing as a Science & Profession; SPONSORED BY Microsoft

• TUESDAY SCHEDULE •

8:00 - 10:00am

Session 4A: Synthesis, Layout, and Crosspoint – Oh My!

Location: Salons A & B1

Session 4B: System Designs with Emerging Memory Technologies

Location: Salons B2 & C

Session 4C: Towards Building Next Generation Embedded Software and Systems

Location: Newport & Marina

Special Session 4D: Where Are the True Innovations and Potentials of IoT?

Location: SSR

10:00 - 10:30am

Coffee Break

Location: Salon E Foyer

10:30am - 12:00pm

Session 5A: Split Manufacturing

Location: Salons A & B1

Session 5B: Exploring Intricate Gate Level Optimization Trade-offs

Location: Salons B2 & C

Session 5C: X-learning for IoT

Location: Newport & Marina

Session 5D: New Directions in Secure Validation and Attestation

Location: SSR

12:00 - 12:30pm

Lunch

Location: Salon D

12:30 - 1:30pm

CEDA Invited Keynote: Socially Assistive Robotics: Creating Robots that Care and Shaping the Future of Work

Location: Salon D

Sponsored by: IEEE CEDA IEEE Council on Electronic Design Automation

1:45 - 3:45pm

Session 6A: Novel Frameworks and Optimizations in Hardware Synthesis

Location: Salons A & B1

Session 6B: New Advances in Approximate Computing and Neural Network Implementations

Location: Salons B2 & C

Session 6C: Power and Thermal Management for Cool Chips

Location: Newport & Marina

Special Session 6D: FPGA CAD: Emerging Challenges and Solutions

Location: SSR

3:45 - 4:15pm

Coffee Break

Location: Salon E Foyer

4:15 - 6:15pm

Session 7A: Taming Routability with Improved Placement

Location: Salons A & B1

Session 7B: X Marks the Spot: Computing and Crossbars

Location: Salons B2 & C

Special Session 7C: Cross-layer Dependability of Medical CPS

Location: Newport & Marina

Special Session 7D: Automotive EDA: Constructing the Intersection of Silicon Valley and Motor City

Location: SSR

6:15 - 6:45pm

Networking Reception

Location: Salon E Foyer

6:45 - 8:30pm

ACM/SIGDA Member Meeting

Location: Salon D

Sponsored by: Association for Computing Machinery

Session 4A - Synthesis, Layout, and Crosspoint – Oh My!

Time: 8:00am - 10:00am | Location: Salons A & B1

Moderator:

Xiaoqing Xu - *ARM, Inc.*

Synthesis and layout sit at the core of electronic design automation (EDA). This session considers synthesis techniques for memristor-based logic and optical circuits, as well as layout decomposition using block copolymer materials. Crosspoint architectures for emerging spin-orbit torque magnetic memories are also discussed.

4A.1 SIMPLE MAGIC: Synthesis and In-Memory Mapping of Logic Execution for Memristor Aided Logic

Rotem Ben Hur, Nimrod Wald, Nishil Talati, Shahar Kvatinsky - *Technion - Israel Institute of Technology*

4A.2 Dedicated Synthesis for MZI-Based Optical Circuits based on AND-Inverter Graphs

Arighna Deb - *KIIT Univ.*
Robert Wille - *Johannes Kepler Univ. Linz*
Rolf Drechsler - *Univ. of Bremen & DFKI GmbH*

4A.3 Simultaneous Template Assignment and Layout Decomposition Using Multiple BCP Materials in DSA-MP Lithography

Kuo-Hao Wu, Shao-Yun Fang - *National Taiwan Univ. of Science and Technology*

4A.4 PRESCOTT: Preset-based Cross-Point Architecture for Spin-Orbit-Torque Magnetic Random Access Memory

Liang Chang, Zhaohao Wang - *Beihang Univ.*
Alvin Oliver Glova - *Univ. of California, Santa Barbara*
Jishen Zhao - *Univ. of California, Santa Cruz*
Youguang Zhang - *Beihang Univ.*
Yuan Xie - *Univ. of California, Santa Barbara*
Weisheng Zhao - *Beihang Univ.*

Session 4B - System Designs with Emerging Memory Technologies

Time: 8:00am - 10:00am | Location: Salons B2 & C

Moderator:

Wujie Wen - *Florida International Univ.*

This session will explore innovative system designs and applications with emerging memory technologies. Techniques are proposed to create better memory systems with Phase Change Memory and Resistive Memory. An approximate image storage is built with multi-level cell STT-MRAM. Asymmetric cryptography is performed efficiently with modular multipliers based on Racetrack memory.

4B.1 Cost-Effective Write Disturbance Mitigation Techniques for Advancing PCM Density
Mohammad Khavari Tavana, David Kaeli - *Northeastern Univ.*

4B.2* Speeding Up Crossbar Resistive Memory by Exploiting In-Memory Data Patterns
Wen Wen, Lei Zhao, Youtao Zhang, Jun Yang - *Univ. of Pittsburgh*

4B.3 Approximate Image Storage with Multi-Level Cell STT-MRAM Main Memory
Hengyu Zhao - *Univ. of California, Santa Cruz*
Linuo Xue - *Univ. of California, Santa Barbara*
Ping Chi - *Intel Corp.*
Jishen Zhao - *Univ. of California, Santa Cruz*

4B.4 A Novel Two-Stage Modular Multiplier Based on Racetrack Memory for Asymmetric Cryptography
Tao Luo - *Nanyang Technological Univ. & Hong Kong Univ. of Science and Technology*
Wei Zhang - *Hong Kong Univ. of Science and Technology*
Bingsheng He - *National Univ. of Singapore*
Douglas L. Maskell - *Nanyang Technological Univ.*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 4C - Towards Building Next Generation Embedded Software and Systems

Time: 8:00am - 10:00am | Location: Newport & Marina

Moderator:

Kapil Dev - *Nvidia Corp.*

This session explores the challenges involved in developing next generation embedded software and systems, which include mobile platforms, learning algorithms and applications like Advanced Driver Assist Systems and Autonomous Driving. The development of these systems demands new frameworks and methods for architecture exploration, modeling, and validation. Virtual Test bench, Distributed Learning algorithms, Reliable Computation and benchmarking automotive applications are the highlights of the approaches presented in this session.

4C.1 VST: A Virtual Stress Testing Framework for Discovering Bugs in SSD Flash-Translation Layers

Ren-Shuo Liu, **Yun-Sheng Chang**, Chih-Wen Hung - *National Tsing Hua Univ.*

4C.2 AdaLearner: An Adaptive Distributed Mobile Learning System for Neural Networks

Jiachen Mao - *Duke Univ.*
Zhuwei Qin, Zirui Xu - *George Mason Univ.*
Kent W. Nixon - *Duke Univ.*
Xiang Chen - *George Mason Univ.*
Hai (Helen) Li, Yiran Chen - *Duke Univ.*

4C.3 NEMESIS: A Software Approach for Computing in Presence of Soft Errors

Moslem Didehban, Aviral Shrivastava, Sai Ram Dheeraj Lokam - *Arizona State Univ.*

4C.4 An Open Benchmark Implementation for Multi-CPU Multi-GPU Pedestrian Detection in Automotive Systems

Matina Maria Trompouki - *Univ. Politècnica de Catalunya*
Leonidas Kosmidis - *Barcelona Supercomputing Center (BSC)*
Nacho Navarro - *Barcelona Supercomputing Center (BSC) and Universitat Politècnica de Catalunya*

All speakers are denoted in bold | * denotes Best Paper Candidate

Special Session 4D - Where Are the True Innovations and Potentials of IoT?

Time: 8:00am - 10:00am | Location: SSR

Moderator:

Deming Chen - *Univ. of Illinois at Urbana-Champaign*

Organizer:

Deming Chen - *Univ. of Illinois at Urbana-Champaign*

The rise of the Internet of Things (IoT) has led to an explosion of new sensor computing platforms, that dramatically expand the domains of applications, design complexity and diversity, and new and stringent design requirements over conventional embedded systems. In a wide variety of application domains, IoT device manufacturers must design and release new IoT devices regularly with shorter product cycles to maintain competitive advantages, differentiate products, sustain growth, and protect market share. Meanwhile, in order for IoT to realize its true potential, the whole eco-system needs to be built where IoT edge devices, communication channels, and data centers all demand new technology for delivering low-power/energy, low latency, high-throughput solutions in terms of sensing, communication, data analysis, and decision making. This special session will present four important themes in terms of IoT design and research from both industrial and academic experts to demonstrate the current state-of-the-art solutions and propose future compelling research directions. This special session is important to the audience of ICCAD when IoT, big data, and deep learning become important topics for the conference. The special session is very timely to share the current-state-of-the-art, and motivate and propose new research solutions to face the IoT revolution.

4D.1 Novel Heterogeneous Computing Platforms and 5G Communications for IoT Applications
Yuichi Nakamura, Hideyuki Shimonishi, Kozo Satoda, Dai Kanetomo, Yuki Kobayashi, Yasuhiko Matsunaga - *NEC Corp.*

4D.2 Edge Segmentation: Empowering Mobile Telemedicine with Compressed Cellular Neural Networks
Xiaowei Xu, Qing Lu, Tianchen Wang, Jinglan Liu - *Univ. of Notre Dame*
Cheng Zhuo - *Zhejiang Univ.*
X. Sharon Hu, **Yiyu Shi** - *Univ. of Notre Dame*

4D.3 CNN-based Pattern Recognition on Nonvolatile IoT Platform for Smart Ultraviolet Monitoring
Jinyang Li, Qingwei Guo, Fang Su, Zhe Yuan, Jinshan Yue - *Tsinghua Univ.*
Jingtong Hu - *Univ. of Pittsburgh*
Huazhong Yang, **Yongpan Liu** - *Tsinghua Univ.*

4D.4 Machine Learning on FPGAs to Face the IoT Revolution
Anand Ramachandran, Di He - *Inspirit IoT, Inc.*
Xiaofan Zhang, Chuanhao Zhuge, Wei Zuo - *Univ. of Illinois at Urbana-Champaign*
Kyle Rupnow - *Inspirit IoT, Inc.*
Deming Chen - *Univ. of Illinois at Urbana-Champaign*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 5A - Split Manufacturing

Time: 10:30am - 12:00pm | Location: Salons A & B1

Moderator:

Ujjwal Guin - *Auburn Univ.*

Split manufacturing defends against fab-based malicious activities caused by untrusted foundries. The first presentation describes how to address manufacturability alongside security. The second work considers scenarios where the back-end-of-line is untrusted. The final paper describes layout protection techniques to reduce the effect of proximity attacks.

5A.1 Making Split Fabrication Synergistically Secure and Manufacturable

Lang Feng - *Texas A&M Univ.*
Yujie Wang - *Nankai Univ.*
Wai-Kei Mak - *National Tsing Hua Univ.*
Jeyavijayan Rajendran - *Univ. of Texas at Dallas*
Jiang Hu - *Texas A&M Univ.*

5A.2 Front-End-of-Line Attacks in Split Manufacturing

Yujie Wang - *Nankai Univ.*
Tri Cao - *Univ. of Texas at Dallas*
Jiang Hu - *Texas A&M Univ.*
Jeyavijayan Rajendran - *Univ. of Texas at Dallas*

5A.3 Rethinking Split Manufacturing: An Information-Theoretic Approach with Secure Layout Techniques

Abhrajit Sengupta, Satwik Patnaik - *New York Univ.*
Johann Knechtel, Mohammed Ashraf - *New York Univ., Abu Dhabi*
Siddharth Garg - *New York Univ.*
Ozgur Sinanoglu - *New York Univ., Abu Dhabi*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 5B - Exploring Intricate Gate Level Optimization Trade-Offs

Time: 10:30am - 12:00pm | Location: Salons B2 & C

Moderator:

Victor Kravets - *IBM T.J. Watson Research Center*

Advances in gate level optimizations require complex trade-offs that include tool efficiency, design accuracy, and circuit timing. The first paper presents a fast Lagrangian relaxation based gate sizer. The second paper uses statistical testing to generate approximate circuits that provide error guarantees with high confidence level. The final paper describes a timing-driven optimization that makes use of a pre-computed restructuring choices.

5B.1 Rapid Gate Sizing with Fewer Iterations of Lagrangian Relaxation
Ankur Sharma - *Iowa State Univ.*
David Chinnery, Shrirang Dhamdhere - *Mentor, A Siemens Business*
Chris Chu - *Iowa State Univ.*

5B.2 Statistically Certified Approximate Logic Synthesis
Gai Liu, Zhiru Zhang - *Cornell Univ.*

5B.3 Enabling Exact Delay Synthesis
Luca Amaru - *Synopsys, Inc.*
Mathias Soeken - *École Polytechnique Fédérale de Lausanne*
Patrick Vuillod, Jiong Luo - *Synopsys, Inc.*
Alan Mishchenko - *Univ. of California, Berkeley*
Pierre-Emmanuel Gaillardon - *Univ. of Utah*
Janet Olson - *Synopsys, Inc.*
Robert Brayton - *Univ. of California, Berkeley*
Giovanni De Micheli - *École Polytechnique Fédérale de Lausanne*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 5C - X-Learning for IoT

Time: 10:30am - 12:00pm | Location: Newport & Marina

Moderator:

Elaheh Bozorgzadeh - *Univ. of California, Irvine*

This session focuses on the use of machine intelligence to improve the energy efficiency and performance of IoT and wearable devices.

The first paper, "Learn-on-the-go", uses transfer learning to improve the classification accuracy through the collaboration of multiple wearable IoT devices. The second paper proposes a method for optimal energy allocation for energy-harvested wearable devices. The third paper uses Q-learning to achieve optimal checkpointing of intermittently-powered IoT devices.

5C.1 Learn-on-the-Go: Autonomous Cross-Subject Context Learning for Internet-of-Things Applications
Ramin Fallahzadeh, Parastoo Alinia, Hassan Ghasemzadeh - *Washington State Univ.*

5C.2 Near-Optimal Energy Allocation for Self-Powered Wearable Systems
Ganapati Bhat, Jaehyun Park, Umit Ogras - *Arizona State Univ.*

5C.3 Optimal Checkpointing for Secure Intermittently-Powered IoT Devices
Zahra Ghodsi, Siddharth Garg, Ramesh Karri - *New York Univ.*

Session 5D - New Directions in Secure Validation and Attestation

Time: 10:30am - 12:00pm | Location: SSR

Moderator:

Wei Hu - *Northwestern Polytechnical Univ.*

This session highlights three emerging topics in software and embedded security. It kicks off with a remote attestation technique that allows a trusted party to verify the integrity of the software running on a remote and potentially compromised device. This is followed by a security validation approach for Systems-on-Chips using static information flow analysis to detect data leakage, untrusted access, confidentiality and integrity. Finally, an approach to memory access control using self-verified address spaces is presented.

5D.1* ATRIUM: Runtime Attestation Resilient Under Memory Attacks
Shaza Zeitouni, Ghada Dessouky - *Technische Univ. Darmstadt*
Orlando Arias - *Univ. of Central Florida*
Dean Sullivan - *Univ. of Florida*
Ahmad Ibrahim - *Technische Univ. Darmstadt*
Yier Jin - *Univ. of Florida*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt*

5D.2 Hardening Extended Memory Access Control Schemes with Self-Verified Address Spaces
Jesse Elwell - *Vencore Labs & Binghamton Univ.*
Dmitry Evtyushkin - *College of William & Mary*
Nael Abu-Ghazaleh - *Univ. of California, Riverside*
Dmitry Ponomarev - *SUNY Binghamton*
Ryan Riley - *Carnegie Mellon Univ. in Qatar*

5D.3 Early SoC Security Validation by VP-Based Static Information Flow Analysis
Muhammad Hassan - *DFKI GmbH*
Vladimir Herdt, Hoang M. Le - *Univ. of Bremen*
Daniel Grosse, Rolf Drechsler - *Univ. of Bremen & DFKI GmbH*

Lunch

Time: 12:00pm - 12:30pm | Location: Salon D

Join fellow attendees for lunch in Salon D.

All speakers are denoted in bold | * denotes Best Paper Candidate

CEDA Invited Keynote: Socially Assistive Robotics: Creating Robots that Care and Shaping the Future of Work

Time: 12:30pm - 1:30pm | Location: Salon D

Speaker:

Maja Matarić - *Univ. of Southern California*

Robotics is booming all around us. A field that was originally driven by the desire to automate physical work is now raising concerns about the future of work. Less discussed but no more important are the implications on human health, as the science on longevity and resilience indicates that having the drive to work is key for health and wellness. However, robots, machines that were originally invented to automate work, are also becoming helpful by not doing any physical work at all, but instead by motivating and coaching us to do our own work, based on evidence from neuroscience and behavioral science demonstrating that human behavior is most strongly influenced by physically embodied social agents, including robots. The field of socially assistive robotics (SAR) focuses on developing intelligent socially interactive machine that that provide assistance through social rather than physical means. The robot's physical embodiment is at the heart of SAR's effectiveness, as it leverages the inherently human tendency to engage with lifelike (but not necessarily human-like or otherwise biomimetic) agents. People readily ascribe intention, personality, and emotion to robots; SAR leverages this engagement to develop robots capable of monitoring, motivating, and sustaining user activities and improving human learning, training, performance and health outcomes. Human-robot interaction (HRI) for SAR is a growing multifaceted research field at the intersection of engineering, health sciences, neuroscience, social, and cognitive sciences, with rapidly growing commercial spinouts. This talk will describe research into embodiment, modeling and steering social dynamics, and long-term adaptation and learning for SAR, grounded in projects involving multi-modal activity data, modeling personality and engagement, formalizing social use of space and non-verbal communication, and personalizing the interaction with the user over a period of months, among others. SAR systems have been validated with a variety of user populations, including stroke patients, children with autism spectrum disorders, elderly with Alzheimer's and other forms of dementia; this talk will cover the short, middle, and long-term commercial applications of SAR, as well as the frontiers of SAR research.

Biography: Maja Matarić is professor and Chan Soon-Shiong chair in Computer Science Department, Neuroscience Program, and the Department of Pediatrics at the University of Southern California, founding director of the USC Robotics and Autonomous Systems Center (RASC), co-director of the USC Robotics Research Lab and Vice Dean for Research in the USC Viterbi School of Engineering. She received her PhD in Computer Science and Artificial Intelligence from MIT in 1994, MS in Computer Science from MIT in 1990, and BS in Computer Science from the University of Kansas in 1987. She is a Fellow of the American Association for the Advancement of Science (AAAS), Fellow of the IEEE and AAAI, and recipient of the Presidential Awards for Excellence in Science, Mathematics & Engineering Mentoring (PAESMEM), the Anita Borg Institute Women of Vision Award for Innovation, Okawa Foundation Award, NSF Career Award, the MIT TR35 Innovation Award, and the IEEE Robotics and Automation Society Early Career Award. She served as the elected president of the USC faculty and the Academic Senate. At USC she has been awarded the Viterbi School of Engineering Service Award and Junior Research Award, the Provost's Mentoring Award and Center for Interdisciplinary Research Fellowship, the Mellon Mentoring Award, the Academic Senate Distinguished Faculty Service Award, and a Remarkable Woman Award. She is featured in the science documentary movie "Me & Isaac Newton", in The

New Yorker ("Robots that Care" by Jerome Groopman, 2009), Popular Science ("The New Face of Autism Therapy", 2010), the IEEE Spectrum ("Caregiver Robots", 2010), and is one of the LA Times Magazine 2010 Visionaries. Prof. Matarić is the author of a popular introductory robotics textbook, "The Robotics Primer" (MIT Press 2007), an associate editor of three major journals and has published extensively. She serves or has recently served on a number of advisory boards, including the National Science Foundation Computing and Information Sciences and Engineering (CISE) Division Advisory Committee, and the Willow Garage and Evolution Robotics Scientific Advisory Boards. Prof. Matarić is actively involved in K-12 educational outreach, having obtained federal and corporate grants to develop free open-source curricular materials for elementary and middle-school robotics courses in order to engage student interest in science, technology, engineering, and math (STEM) topics. Her Interaction Lab's research into socially assistive robotics is aimed at endowing robots with the ability to help people through individual non-contact assistance in convalescence, rehabilitation, training, and education. Her research is currently developing robot-assisted therapies for children with autism spectrum disorders, stroke and traumatic brain injury survivors, and individuals with Alzheimer's Disease and other forms of dementia.

Session 6A - Novel Frameworks and Optimizations in Hardware Synthesis

Time: 1:45pm - 3:45pm | Location: Salons A & B1

Moderator:

Tony Givargis - *Univ. of California, Irvine*

This session addresses a range of synthesis problems that span clockless paradigm, approximate computing, datapath optimization, and accurate modeling of HLS-generated accelerators. The first paper proposes a new framework for improving quality of asynchronous circuits leveraging a suite of existing tools. The paper on the approximate computing presents a new method synthesizing arithmetic circuits. The third paper exploits graph isomorphism to achieve more efficient resource sharing at bit-level. The final paper enables a fast design-space exploration for C-based HLS by accurately modeling the generated accelerators.

6A.1 Data Path Optimisation and Delay Matching for Asynchronous Bundled-Data Balsa Circuits
Norman Kluge, - *Hasso-Plattner-Institut & IHP Microelectronics*
Ralf Wollowski - *Hasso-Plattner-Institut*

6A.2 Approximating Complex Arithmetic Circuits with Formal Error Guarantees: 32-bit Multipliers Accomplished
Milan Ceska, Jiri Matyas, **Vojtech Mrazek**, Lukas Sekanina, Zdenek Vasicek, Tomas Vojnar - *Brno Univ. of Technology*

6A.3 Advanced Datapath Synthesis Using Graph Isomorphism
Cunxi Yu - *Univ. of Massachusetts, Amherst*
Mihir Choudhury, Andrew Sullivan - *IBM T.J. Watson Research Center*
Maciej Ciesielski - *Univ. of Massachusetts, Amherst*

6A.4* COMBA: A Comprehensive Model-Based Analysis Framework for High Level Synthesis of Real Applications
Jieru Zhao, Liang Feng - *Hong Kong Univ. of Science and Technology*
Sharad Sinha - *Nanyang Technological Univ.*
Wei Zhang - *Hong Kong Univ. of Science and Technology*
Yun (Eric) Liang - *Peking Univ.*
Bingsheng He - *National Univ. of Singapore*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 6B - New Advances in Approximate Computing and Neural Network Implementations

Time: 1:45pm - 3:45pm | Location: Salons B2 & C

Moderator:

Muhammad Shafique - *Vienna Univ. of Technology*

This session has four papers that contribute new advances in approximating and neural networks. The first paper presents a new technique to approximate mathematical functions using Taylor series and look-up tables. The second paper proposes a novel method to generate approximate data processing given arbitrary data flow graphs as inputs. The third paper presents a new spiking neural network model and a back-propagation algorithm with much improved accuracy. The fourth paper presents a new approach based on block-circulant matrices to achieve highly compressed, high-performance, and energy efficient deep neural network implementations.

6B.1 ApproxLUT: A Novel Approximate Lookup Table-Based Accelerator
Ye Tian, Ting Wang, Qian Zhang, Qiang Xu - *Chinese Univ. of Hong Kong*

6B.2 Energy Efficient Runtime Approximate Computing on Data Flow Graphs
Mingze Gao, Gang Qu - *Univ. of Maryland, College Park*

6B.3 MT-Spike: A Multilayer Time-Based Spiking Neuromorphic Architecture with Temporal Error Backpropagation
Tao Liu, Zihao Liu - *Florida International Univ.*
Fuhong Lin - *Univ. of Science & Technology Beijing*
Yier Jin - *Univ. of Central Florida*
Gang Quan, Wujie Wen - *Florida International Univ.*

6B.4 Energy-Efficient, High-Performance, Highly-Compressed Deep Neural Network Design Using Block-Circulant Matrices
Siyu Liao - *City Univ. of New York*
Zhe Li - *Syracuse Univ.*
Xue Lin - *Northeastern Univ.*
Qinru Qiu, Yanzhi Wang - *Syracuse Univ.*
Bo Yuan - *City Univ. of New York*

Session 6C - Power and Thermal Management for Cool Chips

Time: 1:45pm - 3:45pm | Location: Newport & Marina

Moderator:

Siddharth Garg - *New York Univ.*

Efficient power and thermal modeling is key for designing high performance chips without breaking the cooling limits. This session looks into power and thermal management at various level of granularity. The first paper deals with managing workload so that the supply voltage variation remains within the specified limit. The second paper exploits unique thermal characteristics of STTMRAM for energy efficiency. Thermal management of mobile SoCs is the focus of the third paper and the final paper introduces a computationally-efficient thermal modeling methodology.

6C.1 Power Scheduling with Active Power Grids
Zahi Moudallal, Farid N. Najm - *Univ. of Toronto*

6C.2 Thermosiphon: A Thermal Aware NUCA Architecture for Write Energy Reduction of the STT-MRAM based LLCs
Bi Wu, Yuanqing Cheng, Pengcheng Dai, Jianlei Yang, Youguang Zhang - *Beihang Univ. & Fert Beijing Institute*
Dijun Liu - *China Academy Of Telecommunications Technology*
Ying Wang - *Chinese Academy of Sciences & Institute of Computing Technology*
Weisheng Zhao - *Beihang Univ & Fert Beijing Institute.*

6C.3 Thermal Modeling and Design on Smartphones with Heat Pipe Cooling Technique
Hong-Wen Chiou - *National Chiao Tung Univ. & Industrial Technology Research Institute*
Yu-Min Lee, Hsuan-Hsuan Hsiao - *National Chiao Tung Univ.*
Liang-Chia Cheng - *Industrial Technology Research Institute*

6C.4 Computationally Efficient Standard-Cell FEM-Based Thermal Analysis
Yi-Chung Chen - *Univ. of Manchester & State Univ. of New York at New Paltz*
Scott Ladenheim, Harry Kalargaris, Milan Mihajlovic, **Vasilis Pavlidis** - *Univ. of Manchester*

Special Session 6D – FPGA CAD: Emerging Challenges and Solutions

Time: 1:45pm - 3:45pm | Location: SSR

Moderator:

Sabya Das - *Xilinx Inc.*

Organizers:

Evangeline F.Y. Young - *The Chinese Univ. of Hong Kong*
Bei Yu - *The Chinese Univ. of Hong Kong*
Wei Zhang - *Hong Kong Univ. of Science and Technology*

Field Programmable Gate Arrays (FPGA) finds wider applications nowadays with the advancement in technology and gains increasing interests in heterogeneous computing and energy efficiency acceleration. FPGAs have evolved from simple programmable logic fabrics to replacing custom designs and processors for signal processing and other wide spreading applications. New generations of FPGA target at implementing the whole system on a single device, and various resources like LUT, flip-flop, RAM, DSP, as well as CPUs are placed at different locations of the device. The trend is bigger and faster in general. These advances in FPGA technology have posed many new challenges to the system and synthesis level design tools. FPGA tools nowadays need to handle various objectives like power, timing, routability and wire length, on top of other challenges like clock net construction, resource allocation, run time reduction, etc. This session highlights new CAD frameworks and techniques, in both front-end to back-end stages, for today's large scale heterogeneous FPGAs.

6D.1 Deep Learning Challenges and Solutions with Xilinx FPGAs
Elliott Delaye, Chaithanya Dudha, Ashish Sirasao, Sabya Das - *Xilinx Inc.*

6D.2 FPGA Placement and Routing
Shih-Chun Chen, Yao-Wen Chang - *National Taiwan Univ.*

6D.3 UTPlaceF 3.0: A Parallelization Framework for Modern FPGA Global Placement
Wuxi Li, Meng Li, Jiajun Wang, David Z. Pan - *Univ. of Texas at Austin*

6D.4 Clock-Aware UltraScale FPGA Placement with Machine Learning Routability Prediction
Chak-Wa Pui, Gengjie Chen, Yuzhe Ma, Evangeline F. Y. Young, Bei Yu - *Chinese Univ. of Hong Kong*

6D.5 A Hybrid Approach to Cache Management in Heterogeneous CPU-FPGA Platforms
Liang Feng - *Hong Kong Univ. of Science and Technology*
Sharad Sinha - *Nanyang Technological Univ.*
Wei Zhang - *Hong Kong Univ. of Science and Technology*
Yun Liang - *Peking Univ.*

Session 7A - Taming Routability with Improved Placement

Time: 4:15pm - 6:15pm | Location: Salons A & B1

Moderator:

Stephen Yang - *Xilinx Inc.*

From ASICs to FPGAs, this session showcases the heterogeneous nature of placement to handle the critical issue of routing congestion. The first two papers perform macro-block placement to address routing challenges. The third paper propagates pins on fixed macros for better routing, and the final paper describes a clock-aware placement algorithm for large-scale heterogeneous FPGAs.

7A.1 An Integrated-Spreading-Based Macro-Refining Algorithm for Large-Scale Mixed-Size Circuit Designs
Szu-To Chen, Yao-Wen Chang - *National Taiwan Univ.*
Tung-Chieh Chen - *Maxeda Technology, Inc.*

7A.2 A Novel Damped-Wave Framework for Macro Placement
Chin-Hao Chang, Yao-Wen Chang - *National Taiwan Univ.*
Tung-Chieh Chen - *Maxeda Technology, Inc.*

7A.3 GRASP based Metaheuristics for Layout Pattern Classification
Mingyu Woo, Seungwon Kim, Seokhyeong Kang - *Ulsan National Institute of Science and Technology (UNIST)*

7A.4 Clock-Aware Placement for Large-Scale Heterogeneous FPGAs
Yun-Chih Kuo, Chau-Chin Huang, Shih-Chun Chen, Chun-Han Chiang, Yao-Wen Chang, Sy-Yen Kuo - *National Taiwan Univ.*

Session 7B - X Marks the Spot: Computing and Crossbars

Time: 4:15pm - 6:15pm | Location: Salons B2 & C

Moderator:

Yang (Cindy) Yi - *Virginia Polytechnic Institute and State Univ.*

This session focuses on the recent advances enabled by resistive random-access memory (RRAM) technology -- that could help to overcome the "memory wall" associated with von Neumann computing architectures. Papers in this session will consider memristive crossbar devices and their applications to routing, neuromorphic systems, weight stability, and perceptron classifiers.

7B.1 RRAM-Based Reconfigurable In-Memory Computing Architecture with Hybrid Routing
Yue Zha, Jing Li - *Univ. of Wisconsin–Madison*

7B.2 TraNNsformer: Neural Network Transformation for Memristive Crossbar based Neuromorphic System Design
Aayush Ankit, Abhronil Sengupta, Kaushik Roy - *Purdue Univ.*

7B.3 A Closed-Loop Design to Enhance Weight Stability of Memristor Based Neural Network Chips
Bonan Yan - *Duke Univ.*
Jianhua (Joshua) Yang - *Univ. of Massachusetts*
Qing Wu - *Air Force Research Lab*
Yiran Chen, Hai (Helen) Li - *Duke Univ.*

7B.4 Memristor-Based Perceptron Classifier: Increasing Complexity and Coping with Imperfect Hardware
Farnood Merrikh Bayat, Mirko Prezioso, Bhaswar Chakrabarti - *Univ. of California, Santa Barbara*
Irina Kataeva - *DENSO Corp.*
Dmitri Strukov - *Univ. of California, Santa Barbara*

All speakers are denoted in bold | * denotes Best Paper Candidate

Special Session 7C – Cross-layer Dependability of Medical CPS

Time: 4:15pm - 6:15pm | Location: Newport & Marina

Moderator:

Yu Jiang - *Tsinghua Univ.*

Organizers:

Lui Sha - *Univ. of Illinois at Urbana-Champaign*
Shangping Ren - *Illinois Institute of Technology*

Medical Cyber-Physical Systems are safety-critical interconnected, intelligent systems of medical devices and applications, and have witnessed breakthroughs in interacting with patients in medical and healthcare. Originally, medical CPS design is a cross-layer effort requiring expertise from completely different fields: from high level models and treatment guidelines, implemented by software code and protocols, running on hardware platforms. These multiple layers of abstraction with well-defined interfaces allow these groups to work independently. However, as technology scaling, these independently designed layers pose a serious dependability problem. For example, high level models assume sensor values being instantaneously available to the controller, or software often assumes an error-free operation from hardware. As implementation platforms become more complex and distributed, these assumptions are increasingly not true. As a result, a provably dependable medical device controller at the model level might not perform as desired in a concrete implementation. This problem is slowly extending to the circuit and semiconductor level because of semiconductor aging, soft errors and manufacturing variabilities stemming from semiconductor scaling. As a result, the underlying hardware processor platform in the future cannot assumed to be fault free and this has to be accounted for at the higher layers of design abstraction. Therefore, we have a great necessity to explore and exploit the challenges and solutions in this cross-layer dependability of medical CPS. This special session contains four presentations, focuses on bringing together current research ideas and techniques from researchers and practitioners, with the final goal of sharing their specific challenges and solutions for cross-layer dependability of safety-critical medical CPS, starting from high-level models, to software code, architectures, protocol, and finally to circuits and semiconductors

7C.1 An Assessment of Vulnerability of Hardware Neural Networks to Dynamic Voltage and Temperature Variations
Xun Jiao, Mulong Luo, Jeng-Hau Lin, Rajesh K Gupta - *Univ. of California, San Diego*

7C.2 Dependable Integrated Clinical System Architecture with Runtime Verification
Yu Jiang, Mingzhe Wang, Han Liu - *Tsinghua Univ.*
Mohammad Hosseini - *Univ. of Illinois at Urbana-Champaign*
Jiaguang Sun - *Tsinghua Univ.*

7C.3 Toward Safe Interoperations in Network Connected Medical CPS Using Open-Loop Safe Protocol
Andrew Y.-Z Ou - *Univ. of Illinios at Urbana-Champaign*
Maryam Rahmaniheris - *Univ. of Illinois at Urbana Champaign*
Yu Jiang - *Tsinghua Univ.*
Po-Liang Wu, Lui Sha - *Univ. of Illinois at Urbana-Champaign*

7C.4 Model and Integrate Medical Resource Availability into Verifiably Correct Executable Medical Guidelines
Chunhui Guo, Zhicheng Fu, Zhenyu Zhang, Shangping Ren - *Illinois Institute of Technology*
Lui Sha - *Univ. of Illinois at Urbana-Champaign*

All speakers are denoted in bold | * denotes Best Paper Candidate

Special Session 7D - Automotive EDA: Constructing the Intersection of Silicon Valley and Motor City

Time: 4:15pm - 6:15pm | Location: SSR

Moderator:
Shiyan Hu - *Michigan Technological Univ.*

Organizer:
Huafeng Yu - *Boeing*

The design and implementation of an automotive vehicle have become increasingly challenging, with growing functional complexity in scale and features, the adoption of more distributed and networked architectural platforms, and stringent demands on various design constraints posed by performance, fault tolerance, reliability, extensibility and security. The aforementioned trend on growing complexity presents tremendous design and validation challenges and calls for an immediate attention to this emerging area for developing radically new EDA methodologies and practices, as well as enormous opportunities that have been rarely explored in the past. This special session is proposed to report the state-of-the-art advances in research and development for automotive EDA recently made by both academia and industry.

Compared to other special sessions in the automotive domain, our proposed special session carries two unique features:

- Connection to circuit-level EDA: While most automotive research focuses on system-level issues, this special session particularly emphasizes the important connection between automotive EDA and circuit-level CAD. As a modern vehicle is composed of more and more electric devices, the device- and circuit-level non-idealities of integrated circuits (e.g., circuit aging) play an increasingly important role for automotive systems even though these issues have been rarely discussed in the past. For this reason, all hierarchical layers of the CAD community must be involved to efficiently address today's grant challenges for automotive EDA.
- Connection to EDA company: The proposed special session invites EDA company (i.e., Cadence in this case) to discuss the commercial R&D efforts for automotive EDA. Instead of asking automotive manufacturers and suppliers to describe their needs, it is now the time for EDA companies to showcase their commercial products and solutions that can directly benefit the automotive industry. It, in turn, would attract a large number of researchers and engineers from both the EDA and automotive communities.

7D.1 Functional Safety Methodologies for Automotive Applications
Alessandra Nardi, Antonio Armato - *Cadence Design Systems, Inc.*

7D.2 Impact of Circuit Non-Idealities on Vision-Based Autonomous Driving Systems
Handi Yu - *Duke Kunshan Univ.*
Changhao Yan, Xuan Zeng - *Fudan Univ.*
Xin Li - *Duke Kunshan Univ. & Duke Univ.*

7D.3 Timing and Security Analysis Framework for VANET-Based Intelligent Transportation Systems
Bowen Zheng - *Univ. of California, Riverside*
Muhammed O. Sayin - *Univ. of Illinois at Urbana-Champaign*
Chung-Wei Lin, Shinichi Shiraishi - *Toyota InfoTechnology Center*
Qi Zhu - *Univ. of California, Riverside*

All speakers are denoted in bold | * denotes Best Paper Candidate

Networking Reception

Time: 6:15pm - 6:45pm | Location: Salon E Foyer

Whatever your goal, networking receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day's presentations with the conference presenters. All attendees are invited.

ACM/SIGDA Member Meeting

Time: 6:45pm - 8:30pm | Location: Salon D

The annual ACM/SIGDA Member Meeting will be held on Tuesday evening from 6:45-8:30pm. The meeting is open for ACM SIGDA members to attend. Members of the Electronic Design Automation community who would like to learn more about SIGDA or get involved with SIGDA activities are also invited. Dinner and beverages will be served.

The meeting will begin with a brief overview of SIGDA, including its organization, activities, volunteering opportunities, and member benefits. We will then introduce this year's SIGDA Pioneering Achievement award recipient with an informal presentation on her life-long achievements. Next, the Outstanding New Faculty Award winner will present a brief talk on his work. Finally, we will end the evening with the announcement of the winners of ACM Design Automation Student Research Competition taking place at this year's ICCAD. We hope to see you there!

Sponsored by: Association for Computing Machinery

- WEDNESDAY SCHEDULE -

8:45 - 9:45am

Keynote: How EDA Could Save the World (of Computing)

Location: Salons A & B1

9:45 - 10:15am

Coffee Break

Location: Salon E Foyer

10:15am - 12:15pm

Session 8A: Advanced Routing Across Different Application Domains

Location: Salons A & B1

Session 8B: Right Timing for Power!

Location: Salons B2 & C

Session 8C: Biochips, Neuromorphic and Stochastic Computing

Newport & Marina

Embedded Tutorial 8D: Predictive Process Design Kit (PDK) to Accelerate Academic Research in VLSI Design and CAD

Location: SSR

12:30 - 1:30pm

Lunch

Location: Salon D

1:45 - 3:45pm

Session 9A: Errors are Evil: Design for Reliability!

Location: Salons A & B1

Session 9B: Application Mapping and Estimation Methods for Heterogeneous Platforms

Location: Salons B2 & C

Special Session 9C: HDSLs: Domain Specific Languages for Hardware and SoC Design

Location: Newport & Marina

Embedded Tutorial 9D: Critical Infrastructure Safety and Security - Challenges and Research Opportunities

Location: SSR

3:45 - 4:15pm

Coffee Break

Location: Salon E Foyer

4:15 - 5:45pm

Session 10A: Counteracting and Preventing Hardware Trojans

Location: Salons A & B1

Session 10B: Next Generation System Level Technologies

Location: Salons B2 & C

Session 10C: Frameworks and Methodologies for Heterogeneous Computing

Location: Newport & Marina

Session 10D: Emerging Design Methodologies for Analog/RF/Mixed-Signal Circuits and Systems

Location: SSR

5:45 - 6:15pm

Networking Reception

Location: Salon E Foyer

Keynote: How EDA Could Save the World (of Computing)

Time: 8:45am - 9:45am | Location: Salons A & B1

Speaker:

Todd Austin - *Univ. of Michigan*

With the end of Moore's Law arriving soon, there is much concern for the future of computing. Rightly, much of the research community's focus has turned toward heterogeneous parallel architectures, whose application-specialized designs hold the promise to overcome the lost benefits of silicon dimensional scaling. In this talk, I will make the case that the future success of computing has less to do with "how" we design these architectures and more about "how much" will it cost to bring them to the market. My claim is that unless the EDA community can develop technologies and methodologies to lower design costs by at least 100x, no affordable solutions will emerge to close the Moore's Law scaling gap. To get people thinking in this direction, I will present five new research directions that could slash the cost of future hardware designs, ideas that run the gamut from reusable accelerators, to fabless custom silicon, and open-source hardware.

Biography: Todd Austin is a Professor of Electrical Engineering and Computer Science at the University of Michigan in Ann Arbor. His research interests include computer architecture, robust and secure system design, hardware and software verification, and performance analysis tools and techniques. Currently Todd is director of C-FAR, the Center for Future Architectures Research, a multi-university SRC/DARPA funded center that is seeking technologies to scale the performance and efficiency of future computing systems. Prior to joining academia, Todd was a Senior Computer Architect in Intel's Microcomputer Research Labs, a product-oriented research laboratory in Hillsboro, Oregon. Todd is the first to take credit (but the last to accept blame) for creating the SimpleScalar Tool Set, a popular collection of computer architecture performance analysis tools. Todd is co-author (with Andrew Tanenbaum) of the undergraduate computer architecture textbook, "Structured Computer Architecture, 6th Ed." In addition to his work in academia, Todd is founder and President of SimpleScalar LLC and co-founder of InTempo Design LLC. In 2002, Todd was a Sloan Research Fellow, and in 2007 he received the ACM Maurice Wilkes Award for "innovative contributions in Computer Architecture including the SimpleScalar Toolkit and the DIVA and Razor architectures." Todd received his PhD in Computer Science from the University of Wisconsin in 1996.

Session 8A - Advanced Routing Across Different Application Domains

Time: 10:15am - 12:15pm | Location: Salons A & B1

Moderator:

Bei Yu - *Chinese Univ. of Hong Kong*

To get the best out of technology scaling, and meet the application needs, routing needs to be looked at carefully. The papers in this session look at different approaches ranging from post-placement to routing stages to meet complex tradeoffs across different application requirements. We start the session by addressing the problem of leakage power in modern power gated systems on chip. Then, we address the 3D integration problem from a unified RDL routing approach. The last two papers tackle the time-consuming routing process by more efficient topology generation and parallelization algorithms.

8A.1 **Switch Cell Optimization of Power-Gated Modern System-on-Chips**
Dongyoun Yi - *Samsung Electronics Co., Ltd.*
Taewhan Kim - *Seoul National Univ.*

8A.2 **Redistribution Layer Routing for Wafer-Level Integrated Fan-Out Package-on-Packages**
Ting-Chou Lin, Chia-Chih Chi, Yao-Wen Chang - *National Taiwan Univ.*

8A.3* **SALT: Provably Good Routing Topology by a Novel Steiner Shallow-Light Tree Algorithm**
Gengjie Chen, Peishan Tu, Evangeline F.Y. Young - *Chinese Univ. of Hong Kong*

8A.4 **A Coordinated Synchronous and Asynchronous Parallel Routing Approach for FPGAs**
Minghua Shen - *Sun Yat-sen Univ.*
Guojie Luo - *Peking Univ.*

Session 8B - Right Timing for Power!

Time: 10:15am - 12:15pm | Location: Salons B2 & C

Moderator:

Zhiyu Zeng - *Cadence Design Systems, Inc.*

The session is dedicated to advances in static timing and power analysis, which are the key steps of modern design timing closure and signoff flows. The first paper attempts to combine the accuracy benefits of path-based analysis with the good performance of graph based analysis. The second paper of the session describes an advanced constraint-based methodology in power grid verification. The third paper proposes a general graph sparsification methodology, applicable to solving large power grids. Finally the last paper suggest a novel problem formulation and approaches to improve designs through optimizing state retention registers.

8B.1 **Scalable N-Worst Algorithms for Dynamic Timing and Activity Analysis**
Hari Cherupalli, John Sartori - *Univ. of Minnesota, Twin Cities*

8B.2 **Power Grid Verification Under Transient Constraints**
Mohammad Fawaz, Farid N. Najm - *Univ. of Toronto*

8B.3 **SAMG: Sparsified Graph Theoretic Algebraic Multigrid for Solving Large Symmetric Diagonally Dominant (SDD) Matrices**
Zhiqiang Zhao, Yongyu Wang, Zhuo Feng - *Michigan Technological Univ.*

8B.4 **State Retention for Power Gated Design with Non-Uniform Multi-Bit Retention Latches**
Guo-Gin Fan, **Mark Po-Hung Lin** - *National Chung Cheng Univ.*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 8C - Biochips, Neuromorphic and Stochastic Computing

Time: 10:15am - 12:15pm | Location: Newport & Marina

Moderator:

Luca Amaru - *Synopsys, Inc.*

This session discusses novel computing paradigms and applications. The first two papers propose methodologies for the design of novel biochip architectures and techniques for online error recovery for biochips. The third paper describes an implementation of an LSTM neural network on the IBM True North architecture. The final paper presents a novel random number generator for use in stochastic computing.

8C.1* **Adaptive Error Recovery in MEDA Biochips Based on Droplet-Aliquot Operations and Predictive Analysis**
Zhanwei Zhong, Zipeng Li, Krishnendu Chakrabarty - *Duke Univ.*

8C.2 **Sortex: Efficient Timing-Driven Synthesis of Reconfigurable Flow-Based Biochips for Scalable Single-Cell Screening**
Mohamed Ibrahim, Aditya Sridhar, Krishnendu Chakrabarty - *Duke Univ.*
Ulf Schlichtmann - *Technische Univ. München*

8C.3 **A Spike-Based Long Short-Term Memory on a Neurosynaptic Processor**
Amar Shrestha, Khadeer Ahmed - *Syracuse Univ.*
David P. Widemann, Adam T. Moody, Brian C. Van Essen - *Lawrence Livermore National Lab*
Yanzhi Wang, **Qinru Qiu** - *Syracuse Univ.*

8C.4 **Design of Accurate Stochastic Number Generators with Noisy Emerging Devices for Stochastic Computing**
Weikang Qian, Meng Yang - *Shanghai Jiao Tong Univ.*
John Hayes - *Univ. of Michigan*
Deliang Fan - *Univ. of Central Florida*

All speakers are denoted in bold | * denotes Best Paper Candidate

Embedded Tutorial 8D - Predictive Process Design Kit (PDK) to Accelerate Academic Research in VLSI Design and CAD

Time: 10:15am - 12:15pm | Location: SSR

Organizer:
Saurabh Sinha - *ARM Inc.*

Moderator:
Xiaoqing Xu - *ARM, Inc.*

Academic research in VLSI design and CAD, especially for advanced technology nodes has been severely limited by the lack of quality process design kit (PDK). Most advanced technology circuit and CAD research employ either SPICE-only predictive technology models or scale 45nm OpenPDK libraries to sub-10 or 7nm node dimensions. These methods omit important effects such as layout-dependent middle-of-line (MOL) parasitics, BEOL parasitics, multiple patterning effects, etc. As a result, even though academics pursue relevant CAD and VLSI research topics, the results and observations are not always reliable. For CAD research, utilizing scaled GDS/LEF layout files from 45nm technology node to sub-14nm dimensions can lead to erroneous conclusions and the researchers might not be even targeting the relevant problems. To bridge this gap, the ASAP7 PDK targeting the 7nm process node was developed in 2016 as a joint collaboration between ARM and Arizona State University. This session will cover the latest development for the ASAP PDK, including ASAP5 targeting the 5nm technology node, standard cell library development using the ASAP7 PDK and a case study exploring 3D-IC research using the ASAP library.

The primary goal of this session is to improve the awareness of the ICCAD audience regarding the potential of a 'realistic' process design kit for advanced circuit design and CAD research. The three papers will cover all aspects of the PDK, beginning from PDK development; technology assumptions and tool-flows to standard cell library development and design case-studies.

8D.1 ASAP7 Predictive Design Kit Development And Cell Design Technology Co-Optimization
Vinay Vashishtha, Manoj Vangala, Lawrence Clark - *Arizona State Univ.*

8D.2 Standard Cell Library Design and Optimization Methodology for ASAP7 PDK
Xiaoqing Xu, Nishi Shah, Andrew Evans, Saurabh Sinha, Brian Cline, Greg Yeric - *ARM Inc.*

8D.3 Full-Chip Monolithic 3D IC Design and Power Performance Analysis with ASAP7 Library
Kyungwook Chang, Bon Woong Ku - *Georgia Institute of Technology*
Saurabh Sinha - *ARM Inc.*
Sung Kyu Lim - *Georgia Institute of Technology*

Lunch

Time: 12:30pm - 1:30pm | Location: Salon D

Join fellow attendees for lunch in Salon D. There will be a short presentation from 1:00 - 1:15pm given by David J. Goldstein, IEEE Lead Director, on XplorerCode Ocean "Authors & Reproducibility".

Session 9A - Errors are Evil: Design for Reliability!

Time: 1:45pm - 3:45pm | Location: Salons A & B1

Moderator:

Samah Saeed - *Univ. of Washington*

Multiple factors can cause circuits and memories to fail --- aging, stress, defects and layout imperfectness all play a role. This session aims to alleviate these reliability and yield challenges. The first paper presents a procedure for evaluating the performance of 3D-stacked wide-I/O DRAMs under process-induced stress. The second paper combines multiple ideas to implement a dynamic partitioning scheme in dense memories that can better address clustered stuck-at faults. The third paper presents a fast algorithm for electromigration-induced IR-drop degradation in an on-chip power grid. The last paper introduces multi-row detailed placement that mitigates neighbor diffusion effect for yield improvement.

9A.1 Stress-Aware Performance Evaluation of 3D-Stacked Wide I/O DRAMs
Tengtao Li, Sachin Sapatnekar - *Univ. of Minnesota*

9A.2 Dynamic Partitioning to Mitigate Stuck-at Faults in Emerging Memories
Jiangwei Zhang - *National Univ. of Defense Technology & Univ. of Pittsburgh*
Donald Kline Jr. - *Univ. of Pittsburgh*
Liang Fang - *National Univ. of Defense Technology*
Rami Melhem, Alex Jones - *Univ. of Pittsburgh*

9A.3 Fast Physics-Based Electromigration Assessment by Efficient Solution of Linear Time-Invariant (LTI) Systems
Sandeep Chatterjee - *Univ. of Toronto*
Valeriy Sukharev - *Mentor, A Siemens Business*
Farid N. Najm - *Univ. of Toronto*

9A.4 Optimal Multi-Row Detailed Placement for Yield and Model-Hardware Correlation Improvements in Sub-10nm VLSI
Changho Han - *Samsung Electronics Co., Ltd.*
Kwangsoo Han, Andrew B. Kahng, Hyein Lee, **Lutong Wang**, Bangqi Xu - *Univ. of California, San Diego*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 9B - Applicaiton Mapping and Estimation Methods for Heterogeneous Platforms

Time: 1:45pm - 3:45pm | Location: Salons B2 & C

Moderator:

Kia Bazargan - *Univ. of Minnesota*

Two major challenges for wide adoption of heterogeneous platforms are accurate estimation of design metrics and high quality mapping of applications. The first paper discusses a novel SAT-based method for application mapping to CGRA platforms. The second paper improves cross platform power and performance prediction by neural networks. Another paper in the session addresses the shortcomings of performance estimation in HLS flows. The last paper presents a new methodology for dealing with big data in a streaming way.

9B.1 SAT-Based Compilation to a non-vonNeumann Processor
Samit Chaudhuri - *Wave Computing*
Asmus Hetzel - *Amazon Development Center*

9B.2 P4: Phase-Based Power/Performance Prediction of Heterogeneous Systems via Neural Network
Yeseong Kim, Pietro Mercati - *Univ. of California, San Diego*
Ankit More, Emily Shriver - *Intel Corp.*
Tajana Rosing - *Univ. of California, San Diego*

9B.3 HLScope+: Fast and Accurate Performance Estimation for FPGA HLS
Young-kyu Choi - *Univ. of California, Los Angeles*
Peng Zhang - *Falcon Computing Solutions, Inc.*
Peng Li - *Tsinghua Univ.*
Jason Cong - *Univ. of California, Los Angeles*

9B.4 A Streaming Clustering Approach Using a Heterogeneous System for Big Data Analysis
Dajung Lee, Alric Althoff, Dustin Richmond, Ryan Kastner - *Univ. of California, San Diego*

Special Session 9C - HDSLs: Domain Specific Languages for Hardware and SoC Design

Time: 1:45pm - 3:45pm | Location: Newport & Marina

Moderator:

Rainer Doemer - *Univ. of California, Irvine*

Organizers:

Wolfgang Ecker - *Infineon Technologies*
Jürgen Teich - *Friedrich-Alexander-Univ. Erlangen-Nürnberg*

Model Driven Architecture (MDA) is an Object Management Group (OMG) vision for the automation of software design that is almost 15 years old. Recently, a new version 2.0 was published, which takes care of the demand for an even higher level of flexibility. Companions of MDA are so called domain specific languages (DSLs). These languages differ from general purpose languages such as Java, C++ and Python as they are much smaller in terms of constructs and concepts and tailored to specific domains and to specific target hardware architectures.

In the last years, some domain specific languages for hardware design (HDSLs) have been published. All these approaches have proven their benefit in industry grade designs in synthesizing RTL code and/or firmware. In this sense, also the C, C++ and SystemC subsets used by HLS tools are a kind of HDSL targeting control/data-path architectures.

The remaining question is whether HDSLs can cover all design domains above RTL to establish a new layer of abstraction and automation? Is it possible to invent these languages, provide automation tools, and are they economically viable? Is there a need for convergence of HDSLs, since the existing approaches differ in underlying concepts, models and target architectures? To address these questions, this session presents prominent HDSL approaches, shows their use cases and takes a look ahead on new HDSL application areas where HDSLs can be utilized to improve design productivity and design quality.

9C.1 Cyclist: Accelerating Hardware Development
Jonathan Bachrach, Albert Magyar, Palmer Dabbelt, Patrick Li, Richard Lin, Krste Asanovic - *Univ. of California, Berkeley*

9C.2 Python based Framework for HDSLs in an Industrial Design Flow
Wolfgang Ecker, Keerthikumara Devarajegowda - *Infineon Technologies & Technische Univ. München*
Johannes Schreiner - *Infineon Technologies*
Rainer Findenig - *DICE*

9C.3 Spatial - A Domain Specific Language for Programming Configurable Accelerators
Kunle Olukotun - *Stanford Univ.*

9C.4 Generating FPGA-Based Image Processing Accelerators with HIPAcc
Oliver Reiche, M. Akif Özkan - *Friedrich-Alexander-Univ. Erlangen-Nürnberg*
Richard Membarth - *DFKI GmbH*
Jürgen Teich, Frank Hannig - *Friedrich-Alexander-Univ. Erlangen-Nürnberg*

All speakers are denoted in bold | * denotes Best Paper Candidate

Embedded Tutorial 9D - Critical Infrastructure Safety and Security - Challenges and Research Opportunities

Time: 1:45pm - 3:45pm | Location: SSR

Moderator:

Mohammad Al Faruque - *Univ. of California, Irvine*

Organizers:

Mohammad Al Faruque - *Univ. of California, Irvine*
Sandip Ray - *NXP Semiconductors*
Marilyn Wolf - *Georgia Institute of Technology*

The nation's critical infrastructure backbone of a nation's economy, security, and health. In USA, provides the essential services that underpin the society and serve as the 16 critical infrastructure sectors have been identified by the Department of Homeland Security (DHS). We know it as the power we use in our homes, the water we drink, the transportation that moves us, the stores we shop in, and the communication systems we rely on to stay in touch with friends and family. Most of these sectors are cyber-physical in nature. Therefore, due to the tight integration of various cyber and physical domains, these sectors have become vulnerable to many security threats. Today, government in every country has considered the security issues of these sectors as the highest priority. The objective of this tutorial is to perform in-depth overview of critical infrastructure safety and security, the architectures and design flow and evaluate the safety and security requirements in design framework using threat models. Furthermore, the tutorial will investigate emerging security solutions to provide enhanced level of security and trust.

9D.1 Critical Infrastructure Safety and Security - Introduction
Mohammad Al Faruque - *Univ. of California, Irvine*

9D.2 Safe and Secure Cyber-Physical Systems for Smart Grids
Marilyn Wolf - *Georgia Institute of Technology*

9D.3 Transportation Security in the Era of Autonomous Vehicles: Challenges and Practice
Sandip Ray - *NXP Semiconductors*

9D.4 Security Trends and Advances in Manufacturing Systems in the Era of Industry 4.0
Sujit Rokka Chhetri, Sina Faezi, Nafiul Rashid, **Mohammad Abdullah Al Faruque** - *Univ. of California, Irvine*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 10A - Counteracting and Preventing Hardware Trojans

Time: 4:15pm - 5:45pm | Location: Salons A & B1

Moderator:

Tauhidur Rahman - *Univ. of Florida*

Hardware trojans are a serious threat for circuit designers.

The first paper in this session proposes a novel technique for injecting hardware trojans exploiting don't cares. The second paper presents how to automate the process of detecting Trojans hiding in unspecified functionalities, while the third paper describes efficient techniques for detecting analog and digital malicious modifications.

10A.1 Why You Should Care About Don't Cares: Exploiting Internal Don't Care Conditions for Hardware Trojans

Wei Hu - *Univ. of California, San Diego*
Lu Zhang - *Northwestern Polytechnical Univ.*
Armaiti Ardeshiricham, Jeremy Blackstone - *Univ. of California, San Diego*
Bochuan Hou, Yu Tai - *Northwestern Polytechnical Univ.*
Ryan Kastner - *Univ. of California, San Diego*

10A.2 Mining Mutation Testing Simulation Traces for Security and Testbench Debugging

Nicole Fern - *Univ. of California, Santa Barbara & Hong Kong Univ. of Science and Technology*
Tim Cheng - *Hong Kong Univ. of Science and Technology*

10A.3 ACE: Adaptive Channel Estimation for Detecting Analog/RF Trojans in WLAN Transceivers

Kiruba Sankaran Subramani, Angelos Antonopoulos, Ahmed Attia Abotabl, Aria Nosratinia, Yiorgos Makris - *Univ. of Texas at Dallas*

Session 10B - Next Generation System Level Technologies

Time: 4:15pm - 5:45pm | Location: Salons B2 & C

Moderator:

Jishen Zhao - *Univ. of California, Santa Cruz*

This session brings together new advances in technologies and architectures that enable a new generation of highly efficient system-level optimizations that were previously not possible. The first paper conducts a comparison of performance and cost evaluation for traditional 2D monolithic SoCs, 2.5D passive interpose and 2.5/3D active interposer and evaluates their tradeoffs. The session goes on with a presentation based on a hybrid STT-RAM/SRAM register file exploiting the advantages of both technologies to enable an efficient warp scheduler that significantly improves system performance and energy efficiency. The third paper proposes a novel NoC architecture that allows a single-cycle multi-hop and thereby allows for a novel tradeoff between latency and energy-efficiency.

10B.1* Cost-Effective Design of Scalable High-Performance Systems Using Active and Passive Interposers
Dylan Stow, Yuan Xie - *Univ. of California, Santa Barbara*
Taniya Siddiqua, Gabriel H. Loh - *Advanced Micro Devices, Inc.*

10B.2 Towards Warp-Scheduling Friendly STT-MRAM/SRAM Hybrid GPGPU Register File Design
Quan Deng - *National Univ. of Defense Technology & Univ. of Pittsburgh*
Youtao Zhang - *Univ. of Pittsburgh*
Minxuan Zhang - *National Univ. of Defense Technology*
Jun Yang - *Univ. of Pittsburgh*

10B.3 A Case for Low Frequency Single Cycle Multi Hop NOCs for Energy Efficiency and High Performance
Monodeep Kar, Tushar Krishna - *Georgia Institute of Technology*

Session 10C - Frameworks and Methodologies for Heterogeneous Computing

Time: 4:15pm - 5:45pm | Location: Newport & Marina

Moderator:
Guojie Luo - *Peking Univ.*

Heterogeneous computing is difficult. Thus, frameworks and methodologies require constant innovation to facilitate the use heterogeneous platforms. The first paper discusses a general distributed mobile computing system for deployment of large scale deep neural networks. The second paper proposes a general distributed programming environment inspired by EDA applications. The final paper introduces a method to protect IP of convolutional neural networks.

10C.1 MeDNN: A Distributed Mobile System with Enhanced Partition and Deployment for Large-Scale DNNs
Jiachen Mao - *Duke Univ.*
Zhongda Yang - *Univ. of Pittsburgh*
Wei Wen, Chunpeng Wu, Linghao Song, Kent W. Nixon - *Duke Univ.*
Xiang Chen - *George Mason Univ.*
Hai (Helen) Li, Yiran Chen - *Duke Univ.*

10C.2 DtCraft: A Distributed Execution Engine for Compute-intensive Applications
Tsung-Wei Huang, Chun-Xun Lin, Martin Wong - *Univ. of Illinois at Urbana-Champaign*

10C.3 AEP: An Error-bearing Neural Network Accelerator for Energy Efficiency and Model Protection
Lei Zhao, Youtao Zhang, Jun Yang - *Univ. of Pittsburgh*

All speakers are denoted in bold | * denotes Best Paper Candidate

Session 10D - Emerging Design Methodologies for Analog/RF/Mixed-Signal Circuits and Systems

Time: 4:15pm - 5:45pm | Location: SSR

Moderator:

Parijat Mukherjee - *Intel Corp.*

The advances of emerging analog/RF/mixed-signal circuits and systems call for radically new design methodologies. The first paper presents a new optimization algorithm to program re-configurable RF systems. The second paper proposes a reliability-aware design methodology for emerging FinFET technology. The final paper develops an intelligent machine learning approach for yield learning.

10D.1 Efficient Programming of Reconfigurable Radio Frequency (RF) Systems
Mohamed B. Alawieh, Fa Wang, Jun Tao, Shihui Yin, Minhee Jun - *Carnegie Mellon Univ.*
Xin Li - *Duke Univ & Duke Kunshan Univ.*
Tamal Mukherjee, Rohit Negi - *Carnegie Mellon Univ.*

10D.2 Towards Reliability-Aware Circuit Design in Nanoscale FinFET Technology — New-Generation Aging Model and Circuit Reliability Simulator
Shaofeng Guo, Runsheng Wang, Zhuoqing Yu, Peng Hao, Pengpeng Ren, Yangyuan Wang - *Peking Univ.*
Siyu Liao, Chunyi Huang, Tianlei Guo, Alvin Chen, Jushan Xie - *Cadence Design Systems, Inc.*
Ru Huang - *Peking Univ.*

10D.3 Online and Incremental Machine Learning Approaches for IC Yield Improvement
Hongge Chen, Duane Boning - *Massachusetts Institute of Technology*

Networking Reception

Time: 5:45pm - 6:15pm | Location: Salon E Foyer

Whatever your goal, networking receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day's presentations with the conference presenters. All attendees are invited.

All speakers are denoted in bold | * denotes Best Paper Candidate

8:00am - 5:00pm

Hardware and Algorithms for Learning On-a-Chip (HALO)

Location: Salons F & G1

International Workshop on Design Automation for Analog and Mixed-Signal Circuits

Location: Salons G2 & H

10th IEEE/ACM Workshop on Variability, Modeling, and Characterization (VMC)

Location: Salons A & B1

Design Automation for Quantum Computers

Location: Salons B2 & C

EDA/CAD in the IoT eHealth Era: From Devices to Architectures, Applications, and Data Analytics

Location: Newport & Marina

Workshop on Non-conventional Approaches to Hard Optimization (NAHO)

Location: SSR

11:30am - 1:30pm

Lunch

Location: Salon E Foyer

Workshop 1 - Hardware and Algorithms for Learning On-a-Chip (HALO)

Time: 8:00am - 5:00pm | Location: Salons F & G1

Organizers:

Jae-sun Seo - *Arizona State Univ.*
Yu (Kevin) Cao - *Arizona State Univ.*
Xin Li - *Duke Univ.*

Machine learning algorithms, such as those for image based search, face recognition, multi-category classification, and scene analysis, are being developed that will fundamentally alter the way individuals and organizations live, work, and interact with each other. However, their computational complexity still challenges the state-of-the-art computing platforms, especially when the application of interest is tightly constrained by the requirements of low power, high throughput, small latency, etc.

In recent years, there have been enormous advances in implementing machine learning algorithms with application-specific hardware (e.g., FPGA, ASIC, etc.). There is a timely need to map the latest learning algorithms to physical hardware, in order to achieve orders of magnitude improvement in performance, energy efficiency and compactness. Recent progress in computational neurosciences and nanoelectronic technology, such as resistive memory devices, will further help shed light on future hardware-software platforms for learning on-a-chip.

The overarching goal of this workshop is to explore the potential of on-chip machine learning, to reveal emerging algorithms and design needs, and to promote novel applications for learning. It aims to establish a forum to discuss the current practices, as well as future research needs in the fields below.

Speakers:

Kaushik Roy - *Purdue Univ.*
Karam Chatha - *Qualcomm, Inc.*
Paul Whatmough - *ARM, Inc.*
Hai Li - *Duke Univ.*
Gert Cauwenberghs - *Univ. of California, San Diego*
Yongpan Liu - *Tsinghua Univ.*
Bipin Rajendran - *New Jersey Institute of Technology*
Farinaz Koushanfar - *Univ. of California, San Diego*
Mike Davies - *Intel*

Workshop 2 - International Workshop on Design Automation for Analog and Mixed-Signal Circuits

Time: 8:00am - 5:00pm | Location: Salons G2 & H

Organizers:

Zhuo Feng - *Michigan Technological Univ.*
Xin Li - *Duke Univ.*

Growing digitization of integrated circuits has contributed to making system-on-chips ever more complex. Yet, a substantial portion of a chip consists of analog and mixed-signal (AMS) circuits that provide critical functionality like signal conversion. Over the past several decades, aggressive scaling of IC technologies, as well as advancing the integration of heterogeneous physical domains on chip, substantially complicates the design of AMS components. On the one hand, their modeling and design becomes extremely complex. On the other hand, their interplay with the rest of the system-on-chip challenges design, verification and test.

The new technology trends bring enormous challenges and opportunities for AMS design automation. This is reflected by an increase in research activity on AMS CAD worldwide. The purpose of this workshop is to bring together academic and industrial researchers from both design and CAD communities to report recent advances and motivate new research topics and directions in this area.

Speakers:

Sachin Sapatnekar - *Univ. of Minnesota*
Jie Gu - *Northwestern Univ.*
Rafa Castro - *Seville Institute of Microelectronics*
Hai Li - *Duke Univ.*
Minsik Cho - *IBM Research*
Zhiru Zhang - *Cornell Univ.*
Farinaz Koushanfar - *Univ. of California, San Diego*
Kaiyuan Yang - *Rice Univ.*
Jeyavijayan Rajendran - *The Univ. of Texas at Dallas*

Workshop 3 - 10th IEEE/ACM Workshop on Variability, Modeling, and Characterization (VMC)

Time: 8:00am - 5:00pm | Location: Salons A & B1

Organizers:

Rasit Topaloglu - *IBM*
Takashi Sato - *Kyoto Univ.*
Ibrahim Elfadel - *Masdar Inst. of Sci. and Tech.*

This workshop provides a forum to discuss current practice as well as near future research needs in the long-term trend of variability/reliability and their impact on design performance and cost, as well as detailed technical aspects of variability/reliability characterization, compact modeling, statistical simulation, test structure design, CAD, as well as resilient design. The workshop also provides an opportunity to discuss emerging modeling and characterization needs in emerging devices. The following are the key areas that will be covered. Compared to other workshops, we strive to establish the links among technology, device physics, device modeling, EDA tools, and related circuit design issues.

- Fundamental device physics and device engineering
- CAD tools: modeling, simulation, and tool integration
- Design interface: design impact and characterization techniques

We pick three focus topics each year on joint technology-design efforts. The rest of the workshop will be formatted as open call-for-poster format. Short oral presentations will be given by all the poster presenters in advance of the poster session.

This year, we plan to focus on the following topics:

- Ising Computing
- In-Memory Computing
- MEMS

Speakers:

Fadi Kurdahi - *Univ. of California, Irvine*
Yoshio Mita - *Univ. of Tokyo*
Haitong Li - *Stanford Univ.*
Hai Li - *Duke Univ.*
Vijay Narayanan - *Pennsylvania State Univ.*
Tajana Simunic Rosing - *Univ. of California, San Diego*
Rajiv Joshi - *IBM Corp.*
Peter McMahon - *Stanford Univ.*
Hidetoshi Onodera - *Kyoto Univ.*

Workshop 4 - Design Automation for Quantum Computers

Time: 8:00am - 5:00pm | Location: Salons B2 & C

Organizers:

Martin Roetteler - *Microsoft Research*
Mathias Soeken - *EPFL*

The workshop aims to bring together researchers from quantum computing, electronic design automation, and compiler construction. Open questions that we anticipate this group to tackle include new methods for circuit synthesis and optimization, optimizations and rewriting, techniques for verifying the correctness of quantum programs, and new techniques for compiling efficient circuits and protocols regarding fault-tolerant and architecture constraints. Currently, only very few opportunities exist to bring together experts from the fields of quantum computing and design automation; to give them the opportunity to engage in exchange of ideas; and to report on progress for both theoretical and implementation aspects. We also expect a vibrant open problems session as well as exchange of benchmarks, i.e., for the best known circuits for some classes of transformations that are important for the synthesis of large quantum algorithms. The invited speakers cover the whole design flow of quantum computing, starting from the design of quantum algorithms to the actual physical devices. The range further covers, quantum programming languages, reversible logic synthesis, quantum circuit optimization, aspects of fault-tolerant quantum computing, and verification of quantum circuits. The talks introduce the state-of-the-art of each field, describe present challenges, and outline opportunities for design automation.

Speakers:

Matthew Amy - *Univ. of Waterloo, Institute for Quantum Computing*
Andrew Cross - *IBM Corp.*
Simon Devitt - *Macquarie Univ. & Turing, Inc.*
Olivia Di Matteo - *Univ. of Waterloo, Institute for Quantum Computing*
Jungsang Kim - *Duke Univ.*
Alan Mishchenko - *Univ. of California, Berkeley*
Matthew Neeley - *Google, Inc.*
Jennifer Paykin - *Univ. of Pennsylvania*
Benoît Valiron - *Univ. Paris-Sud*
Mingsheng Ying - *Univ. of Technology Sydney*
Will Zeng - *Rigetti Computing*

Workshop 5 - EDA/CAD in the IoT eHealth Era: From Devices to Architectures, Applications, and Data Analytics

Time: 8:00am - 5:00pm | Location: Newport & Marina

Organizers:

Farshad Firouzi - *MSG Group*
Krishnendu Chakrabarty - *Duke Univ.*
Sani Nassif - *Radyalis*
Mohammad Al Faruque - *Univ. of California, Irvine*

The interaction between technology and healthcare has a long history. Recent years have seen rapid growth in the Internet of Things (IoT) paradigm, the advent of miniature wearable biosensors, and research advances in "Big Data" techniques for effective manipulation of large, multiscale, multimodal, distributed and heterogeneous data sets. These advances have generated new and exciting opportunities for personalized precision eHealth and mHealth services. IoT heralds a paradigm shift in the healthcare horizon by providing many advantages, including availability and accessibility, ability to personalize and tailor content, and cost-effective delivery. Although IoT eHealth has vastly expanded the possibilities to fulfill a number of existing healthcare needs, many challenges must still be addressed in order to develop consistent, suitable, safe, flexible and power-efficient systems that are suitable for medical needs. To enable this transformation, it is necessary for technological advancements in both hardware and software, and for these communities to work together. Breakthroughs in areas ranging from bioelectronics to communication devices, software and networking, pattern recognition, data-analytics, Big Data, and cloud computing are needed to enable next-generation sensing, control, and computing, and to realize the IoT vision for smarter healthcare. This workshop will address all these important aspects of novel IoT eHealth technologies. It will encompass smart healthcare-wearable sensors, body area sensors, advanced pervasive healthcare systems, and Big Data analytics. Then workshop will identifying new perspectives, and highlight compelling research issues and challenges such as scalability, interoperability, device-network-human interfaces, and security, with various case studies. In addition, through this workshop, we will show how knowledge from CAD areas such as large-scale analysis and optimization techniques can be applied to the important problems of eHealth

Speakers:

Ken Shepard - *Columbia Univ.*
Majid Sarrafzadeh - *Univ. of California, Los Angeles*
Lou Scheffer - *Howard Hughes Medical Institute*
Nikil Dutt - *Univ. of California, Irvine*
Natasha Balac - *Univ. of California, San Diego*

Program Committee:

Tsung-Yi Ho - *National Tsing Hua Univ.*
Bahar Farahani - *Univ. of Tehran*
Kunal Mankodiya - *Univ. of Rhode Island*

Workshop 6 - Workshop on Non-conventional Approaches to Hard Optimization (NAHO)

Time: 8:00am - 5:00pm | Location: SSR

Organizers:

X. Sharon Hu - *Univ. of Notre Dame*
Zoltan Toroczkai - *Univ. of Notre Dame*

Constrained optimization problems are at the heart of many decision, scheduling, error-correction and cyber security applications. Constrained optimization is also a major component in most fundamental EDA problems. Many constrained optimizations are NP-hard in nature, which makes solving them extremely resource demanding, either in terms of computation time or hardware components or energy. Given the importance of these problems, any improvements in efficiency in solving such problems are in great need. As an example, there is a world-wide competition taking place every two years, devoted to finding the best solvers for one of the representative NP-hard constrained optimization problems, i.e., Boolean Satisfiability (SAT).

Most of the efforts on improving solvers for constrained optimization problems aim at developing more effective search algorithms with the understanding that these algorithms would eventually be implemented on modern general-purpose digital computing platforms such as multi-core or many-core processors. Several researchers have investigated implementing such essentially digital algorithms on application specific integration circuits, hence achieving better performance, but at a higher cost. These approaches have been enjoying good success, as they readily benefit from the continuous improvements in CMOS technology that have been governed by Moore's Law.

However, with Moore's Law coming to an end, exploring novel computational paradigms (e.g., quantum computing and neuromorphic computing) is more imperative than ever. Recently there has been increased interest in designing analog, or mixed-signal solvers for some specific NP-hard optimization problems based on continuous–time dynamical systems. Furthermore, a number of researchers are investigating approaches that exploit intrinsic properties exhibited by certain beyond-CMOS devices to solve NP-hard optimization problems.

The purpose of NAHO workshop is to bring together researchers who work on all these aspects employing various approaches for solving hard constraint satisfaction and optimization problems. The workshop will provide a platform for these researchers to exchange advances in each of their respective areas, compare and critique each other's approaches, and forge new collaborative relationships. NAHO is a 1-day event including formal presentations followed by discussion panels and poster presentations by students or junior researchers. All the speakers will be invited.

Speakers:

Sankar Basu - *National Science Foundation*
Olivier Bournez - *Ecole Polytechnique, Paris-Saclay*
Gert Cauwenberghs - *Univ. of California, San Diego*
Peter McMahon - *Stanford Univ.*
Arijit Raychowdhury - *Georgia Institute of Technology*
Sanjit A. Seshia - *Univ. of California, Berkeley*
Zoltan Toroczkai - *Univ. of Notre Dame*

Lunch

Time: 11:30am - 1:30pm | Location: Salon E Foyer

Lunch will be served from the Salon E Foyer. You may then enjoy your lunch in the workshop room that you are attending.

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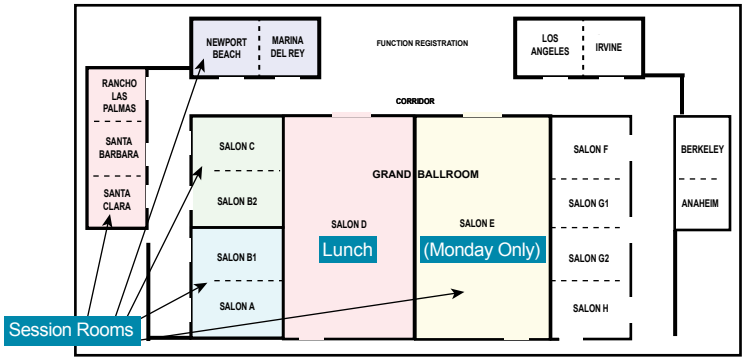

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