THE PREMIER CONFERENCE FOR ELECTRONIC DESIGN TECHNOLOGY

CONFERENCE PROGRAM

November 2-6, 2014
Hilton San Jose, San Jose, California

Sponsored by: IEEE CAS CEDA Association for Computing Machinery sigda

In cooperation with: IEEE Electron Devices Society SSCS

www.ICCAD.com

The Premier Conference Devoted to Technical Innovations in Electronic Design Automation

Yao-Wen Chang
General Chair
National Taiwan Univ., Dept. of Electrical Engineering

Welcome to the 33rd ICCAD!

Welcome to San Jose, California for the 33rd ICCAD, held from November 2nd to 6th, 2014. Like its 32 predecessors, ICCAD 2014 provides a premier forum to explore emerging challenges, present cutting-edge R&D solutions, record theoretical and empirical advances, and identify future roadmaps for design automation. Furthermore, ICCAD 2014 is co-located with the Phil Kaufman Award ceremony, IEEE CEDA CAD Contests, ACM CADathlon Contest and Student Research Competition, the Sunday full-day workshop on TCAD simulation, and five Thursday full-day workshops on design automation for analog and mixed-signal circuits, EDA research in the dark silicon era, variability modeling and characterization, process design kit automation, and heterogeneous computing, an attempt to collaborate with related organizations for higher impact on our community.

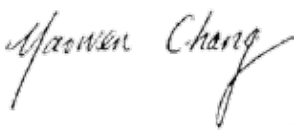
We had 304 worldwide submissions in review by 106 outstanding TPC members organized into 17 subcommittees. After a rigorous double-blind review process that culminated in a full-day physical meeting of the entire TPC in San Francisco, only 77 regular papers were selected for inclusion, making the acceptance rate of only 25%. Besides the 23 sessions for regular papers, the program is further enriched with three keynotes, two designer tracks, four embedded tutorials, seven special sessions, and one Monday evening panel.

Overall, the scope spans all aspects of modern problems in design automation, with forward-looking applications such as internet of things, automotive electronic designs, hardware security, smart energy, sub-10nm-node design-for-manufacturability (DFM), and massive open online courses (MOOCs) on EDA. This year a fast track is introduced to provide a mini preview of the regular-paper presentations for the day.

Since 2012, ICCAD has become a crucial platform for holding annual highly competitive EDA contests, co-hosted by IEEE CEDA and Taiwan Ministry of Education, on modern topics to foster research advancements. This year three contest problems on logic synthesis, timing-driven placement, and DFM flow attracted 93 participating teams worldwide, achieving a greater success for this tradition. The contest results are announced in the Tuesday contest session, along with the release of contest benchmarks.

It is our greatest honor to invite three distinguished keynote speakers: The Monday keynote is by Dr. Peter van Staa, Vice President of Robert Bosch GmbH in Germany, on automotive EDA. On Tuesday, the IEEE CEDA Luncheon Distinguished Lecture is presented by Prof. Rob Rutenbar, Head of the CS Department of UIUC, on EDA MOOCs. On Wednesday, Prof. Srinivas Devadas, the Webster Professor of EECS at MIT, gives the keynote on cybersecurity hardware design. These keynotes provide key insights into crucial future directions for ICCAD to move forward.

We are grateful to our sponsors and all friends involved with ICCAD 2014 for making this conference another successful event. Enjoy your week at ICCAD!



Yao-Wen Chang, *ICCAD 2014 General Chair*

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Speakers / Presenters

SPEAKERS' BREAKFAST
Room: **Santa Clara 1 & 2**
Please attend the day of your presentation!

Monday, November 3	7:30 - 8:30am
Tuesday, November 4	7:30 - 8:30am
Wednesday, November 5	7:30 - 8:30am

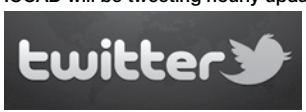
Need Practice?

A/V Practice Rooms are available to all speakers and presenters
Rooms: **Pacific, Univ. & Executive Rooms**

Monday, November 3	7:00am - 6:00pm
Tuesday, November 4	7:00am - 6:00pm
Wednesday, November 5	7:00am - 4:00pm

Twitter: @ICCAD

Connect with ICCAD through Twitter @ICCAD
ICCAD will be tweeting hourly updates and conference highlights!



General Information

CONFERENCE REGISTRATION HOURS
Room: **Almaden Foyer**

Sunday, November 2	7:00am – 4:00pm
Monday, November 3	7:00am – 6:00pm
Tuesday, November 4	7:00am – 6:00pm
Wednesday, November 5	7:00am – 6:00pm
Thursday, November 6	7:00am – 3:00pm

Parking

Attendees who park in the Hilton parking lot receive a discounted parking fee of $10 per day. Hilton parking is located under the Hotel, and the entrance to the Hotel lot is located off of San Carlos Street.

Please Note: If you enter the parking lot off of Almaden Boulevard, that is the Convention Center parking lot, and your discount will not apply.

Conference Management: MP Associates, Inc.

Our mission is to facilitate networking, education and marketing with efficiency and precision in order to maximize customer experiences, and client profitability and recognition. We accomplish this by having a committed staff of trade show production organizers with the training, technology tools, processes and experience to offer the best service in the industry. www.mpassociates.com

Gold Standards Simulations
The Fast Track to Innovation

Live Demonstrations!
Monday - Wednesday, 9:00am - 7:00pm
Location: Almaden Foyer

GSS provides a chain of simulation products that starts with the accurate and predictive simulation of Process and Statistical Variability and Reliability at transistor level.

Using sophisticated statistical compact model extraction techniques implemented in our advanced statistical circuit extraction engine we propagate the results of the physical variability and reliability simulations in industrial strength statistical compact models.

The simulation tool flow captures the correlations between different sources of process variability, the interplay between process and statistical variability and the impact of both on statistical reliability associated with discrete charge trapping. The script-based flow control system parses and generates input files for all simulators and extractors, automatically submits jobs to a large cluster of processors and monitors the job execution. The database control system harvests, annotates and stores data, which can be readily accessed by the different components of the tool flow.

The fully automated GSS tool flow bridges the gap between Technology Computer Aided Design (TCAD) at the transistor level, and circuit simulations and verification. The tool flow allows:

- Rapid simulation-based Design-Technology Co-Optimisation (DTCO)
- Generation of accurate TCAD based compact models for Preliminary Design Kit (PDK) development at the early stages of new technology development.

The use of the tools chain reduces technology development time and costs and products time to market.

Best Paper Candidates/Award Committees

IEEE/ACM William J. McCalla Best Paper Candidates:

Tuesday

Front End Candidate

4C.3: Using Multi-Level Cell STT-RAM for Fast and Energy-Efficient Local Checkpointing
Ping Chi, Cong Xu, Yuan Xie - *Pennsylvania State Univ.*
Tao Zhang - *NVIDIA Corp.*
Xiangyu Dong - *Google, Inc.*

Back End Candidate

4D.1: Modeling and Analysis of Nonstationary Low-Frequency Noise in Circuit Simulators: Enabling Non Monte Carlo Techniques
Ahmet Gokcen Mahmutoglu, Alper Demir - *Koc Univ.*

Back End Candidate

4D.3: Fast Statistical Analysis of Rare Circuit Failure Events via Subset Simulation in High Dimensional Variation Space
Shupeng Sun, Xin Li - *Carnegie Mellon Univ.*

Front End Candidate

6C.3: Constrained Interpolation for Guided Logic Synthesis
Ana Petkovska, David Novo, Paolo Ienne - *Ecole Polytechnique Fédérale de Lausanne*
Alan Mishchenko - *Univ. of California, Berkeley*

Wednesday

Back End Candidate

8D.1: Asynchronous Circuit Placement by Lagrangian Relaxation
Gang Wu, Tao Lin, Chris Chu - *Iowa State Univ.*
Hsin-Ho Huang, Peter Beerel - *Univ. of Southern California*

IEEE/ACM William J. McCalla ICCAD Best Paper Award Selection Committee:

Front End

Alan Hu - Chair - *Univ. of British Columbia*
Igor Markov - *Univ. of Michigan*
Marc Riedel - *Univ. of Minnesota*
Yiran Chen - *Univ. of Pittsburgh*
Steven Nowick - *Columbia Univ.*
Jörg Henkel - *Karlsruhe Institute of Technology*

Back End

Andrew B. Kahng – Chair - *Univ. of California at San Diego*
Peter Feldmann - *D. E. Shaw Research*
Jiang Hu - *Texas A&M Univ.*

Ten-Year Retrospective Most Influential Paper Award Selection Committee:

Hidetoshi Onodera - Chair - *Kyoto Univ.*
Niraj Jha - *Princeton Univ.*
Wolfgang Kunz - *Univ. of Kaiserslautern*
Sachin Sapatnekar - *Univ. of Minnesota*

Sunday, November 2

Workshop 1:

TCAD to EDA: Processes, Devices and Compact Models Simulation Strategies for Contemporary and Future Semiconductor Technology and Circuits
8:00am - 5:00pm
Room: Santa Clara 1 & 2

CADathlon at ICCAD:

8:00am - 5:00pm
Room: Almaden Ballroom

Registration: 7:00am - 4:00pm - Almaden Foyer
Parking: $10 per day with in and out privileges

W1 TCAD to EDA: Processes, Devices and Compact Models Simulation Strategies for Contemporary and Future Semiconductor Technology and Circuits

Room: Santa Clara 1 & 2

Organizers:

Salvatore Maria Amoroso - *Univ. of Glasgow*
Asen Asenov - *Univ. of Glasgow*
Sani Nassif - *Radyalis LLP*

This workshop is complimentary to the first 50 registrants, after the workshop has reached 50, the regular workshop fees will apply.

A premiere list of speakers from academia and industry will deliver a series of talks focused on the frontiers of semiconductor technology modeling, from processes to devices simulation, from compact models up to parameters extraction. The topics treated in the workshop will provide the CAD community with a primer toolkit for a solid understanding of advance simulation strategies for the development of contemporary and future MOSFET technology and circuits.

- A first section on Semiconductor Processes Simulation will provide insights on the modeling challenges for novel CMOS technologies. The emphasis will be on addressing the numerical simulation of the several steps necessary to realize modern MOSFET devices, including the modeling of nanolithography in the subwavelength regime. The importance of process technology variation and its modeling will be stressed. Advanced Kinetic Monte Carlo techniques will be presented for the simulation of growth and diffusion processes in semiconductors.

- A second section will address the simulation of novel MOSFET devices. The Drift-Diffusion simulation approach will be introduced as the most widely adopted tool within the semiconductor industry, highlighting its strengths and deficiency in properly capturing the device electrical behavior at the nanometric scale. The Monte Carlo transport simulation will be then presented as the most advanced classical method for studying the electrons motion in scaled devices. Finally, Non Equilibrium Green Function techniques will be shown for tackling the understanding of quantum effects ruling the transport properties below the decananometer regime.

- A third section will then present the derivation of compact models for studying the device electrical behavior at a circuit level in Spice-like environments. The importance of correctly modeling extrinsic effect related to parasitic elements and interconnects will be stressed. Finally, compact modeling strategies for addressing the statistical variability and reliability of nanoscale MOSFETs will be presented.

- Last but not least, a fourth section will present parameters extraction and optimization techniques for the computer-aided design of novel and future semiconductor systems. The development of model-simulator interfaces and the current status on model standardization procedure will be considered in details.

Speakers:

Robert Dutton - *Stanford Univ.*
Jean-Marie Brunet - *Mentor Graphics Corporation*
Jin Cho - *GLOBALFOUNDRIES*
Martin Giles - *Intel Corp.*
Mark Law - *Univ. of Florida*
Cory Weber - *Intel Corp.*
Craig Alexander - *Gold Standard Simulations Ltd.*
Gerhard Klimeck - *Purdue Univ.*
Colin McAndrew - *Freescale Semiconductor, Inc.*
Asen Asenov - *Univ. of Glasgow*
Hajdin Ceric - *Vienna Univ. of Technology*
Lianfeng Yang - *ProPlus Design Solutions, Inc.*
Joddy Wang - *Synopsys, Inc., Inc.*

Sponsored By: CEDA IEEE Council on Electronic Design Automation; Electron Devices Society; GSS; Mentor Graphics; PROPLUS The DFY Technology Provider

CADathlon at ICCAD

8:00am - 5:00pm
Room: Almaden Ballroom

The CADathlon is a challenging, all-day, programming competition focusing on practical problems at the forefront of Computer-Aided Design, and Electronic Design Automation in particular. The contest emphasizes the knowledge of algorithmic techniques for CAD applications, problem-solving and programming skills, as well as teamwork.

In its thirteenth year as the "Olympic games of EDA," the contest brings together the best and the brightest of the next generation of CAD professionals. It gives academia and the industry a unique perspective on challenging problems and rising stars, and it also helps attract top graduate students to the EDA field.

The contest is open to two-person teams of graduate students specializing in CAD and currently full-time enrolled in a Ph.D. granting institution in any country. Students are selected based on their academic backgrounds and their relevant EDA programming experiences. Travel grants are provided to qualifying students. The **CADathlon**competition consists of six problems in the following areas:

(1) Circuit analysis
(2) Physical design
(3) Logic and behavioral synthesis
(4) System design and analysis
(5) Functional verification
(6) Future technologies (Bio-EDA, Security, etc.)

More specific information about the problems and relevant research papers will be released on the Internet one week prior to the competition. The writers and judges that construct and review the problems are experts in EDA from both academia and industry. At the contest, students will be given the problem statements and example test data, but they will not have the judges' test data. Solutions will be judged on correctness and efficiency. Where appropriate, partial credit might be given. The team that earns the highest score is declared the winner. In addition to handsome trophies, the first place team's prize is a $2,000 cash award. The second place team's prize is a $1,000 cash award.

Contest winners will be announced at the ICCAD Opening Session on Monday morning and celebrated at the ACM/SIGDA Dinner and Member Meeting on Monday evening.

The CADathlon competition is sponsored by ACM/SIGDA and several Computer and EDA companies. For detailed contest information and sample problems from last year's competition, please visit the ACM/ SIGDA website at:

www.sigda.org/programs/cadathlon

ORGANIZING COMMITTEE:
Chair, Myung-Chul Kim
Vice Chair, Jarrod A. Roy
Vice Chair, Luis Angel D. Bathen

Sponsored By:

Monday, November 3

TIME	ALMADEN BALLROOM			
8:15 - 8:40am	**Opening Sessions / Awards:** **Yao-Wen Chang - General Chair,** *National Taiwan Univ.*			
8:40 - 9:30am	**Keynote Address:** **Can EDA Solve the Problems of Electronic Designs for the Cars of the Future?** **Peter van Staa,** *Robert Bosch GmbH*			
	ALMADEN 1	**ALMADEN 2**	**WINCHESTER**	**MARKET 1 & 2**
9:30- 10:00am	**Fast Track:** **Monday Regular Paper Presentations**			
10:30am - 12:00pm	Session 1A: Enhancing Correctness of Advanced Design	Session 1B: CAD for Next-Generation Vehicles	Session 1C: Emerging Reconfigurable Array Technologies	Designer Track 1D: Challenges and Techniques for High Level Design
12:00 - 1:00pm	**Lunch:** Hyatt Hotel - Grand Hall			
1:30 - 3:30pm	Embedded Tutorial 2A: Adaptive Designs in Computing, Power Management and Communication for Low-Power Circuits and Systems with Ultra-Wide Dynamic Ranges	Special Session 2B: Design, Modeling and Tools for Video Analytics Using Emerging Devices	Session 2C: Patterns and Placement	Session 2D: Energy, Performance and Security for Embedded Systems
4:00 - 6:00pm	Special Session 3A: Can One SHIELD Integrated Circuits and Systems from Supply Chain Attacks?	Special Session 3B: Smart Energy System: Electric Vehicle, Home, HVAC, Hybrid System and Cybersecurity	Session 3C: Analysis and Optimization of Timing, Noise, and Power	Session 3D: What is Behind the Mask?
6:00 - 6:30pm	**Networking Reception:** Almaden Foyer			
6:30 - 7:45pm	**Panel:** **Moore's Law is Dying, Long Live EDA!**			

ACM Student Research Competition Poster Session: Santa Clara 1 & 2, *1:00 - 3:00pm*

Opening Session & Award Presentations

Room: Almaden Ballroom

Opening Remarks -

Kick off the conference with opening remarks from the ICCAD Executive Committee members and hear the highlights of the conference. IEEE/ACM William J. McCalla ICCAD Best Paper award will be announced along with other award presentations from IEEE and ACM.

Yao-Wen Chang - General Chair - *National Taiwan Univ.*

Award Presentations -

IEEE/ACM William J. McCalla ICCAD Best Paper Award

This award is given in memory of William J. McCalla for his contribution to ICCAD and his CAD technical work throughout his career.

Front End

4C.3: Using Multi-Level Cell STT-RAM for Fast and Energy-Efficient Local Checkpointing

Ping Chi, Cong Xu, Yuan Xie - *Pennsylvania State Univ.*
Tao Zhang - *NVIDIA Corp.*
Xiangyu Dong - *Google, Inc.*

Back End

4D.1: Modeling and Analysis of Nonstationary Low-Frequency Noise in Circuit Simulators: Enabling Non Monte Carlo Techniques

Ahmet Gokcen Mahmutoglu, Alper Demir - *Koc Univ.*

ICCAD Ten Year Retrospective Most Influential Paper Award

This award is being given to the paper judged to be the most influential on research and industrial practice in computer-aided design of integrated circuits over the ten years since its original appearance at ICCAD.

2004 Paper Titled: A Thermal-Driven Floorplanning Algorithm for 3D ICs

Authors: Jason Cong, Jie Wei, and Yan Zhang - *Univ. of California, Los Angeles*
Publication: ICCAD 2004, pp. 306 – 313

IEEE CEDA Early Career Award

Shobha Vasudevan, *Univ. of Illinois at Urbana-Champaign*
For outstanding contributions to design verification including automatic invariant generation, coverage analysis, timing verification and analog verification.

2014 SIGDA Pioneering Achievement Award

John Hayes, *Claude E. Shannon Professor of Engineering Science, Department of Electrical Engineering and Computer Science, Univ. of Michigan, Ann Arbor*
For his pioneering contributions to logic design, fault tolerant computing, and testing.

SIGDA Distinguished Service Award

Massoud Pedram, *Univ. of Southern California*
For his many years of service as Editor in Chief for the ACM Transactions on Design Automation in Electronic Systems (TODAES)

ACM/SIGDA CADathlon

Introduction of the 2014 winners.

Keynote

Can EDA Solve the Problems of Electronic Designs for the Cars of the Future?

Peter van Staa - *Robert Bosch GmbH*

Room: Almaden Ballroom

Electronic systems in modern cars contribute with more than 80% to the innovation of the Automotive industry – probably being already the most complex systems in products of today. This complexity is not due to the sheer number of components in each device, but by the number of devices, and their heterogeneous nature combining analogue and digital circuits with sensors, actuators and software. In addition the very high demand on robustness and reliability to assure safety and availability at any time and everywhere under rough working conditions requires specific effort in the quality management of the electronics. While in the past a car was more or less a closed system today the use of any kind of multimedia, the communication with the internet and – increasingly - with all parts of the surrounding traffic has becoming a key asset of the development of modern cars. All these aspects have to be addressed by an EDA system which is essential for an electronics design in due time with respect to continuously shorter design cycles in parallel to larger product spectra and high pressure on the development costs due to the increasing competition on the world market. A further challenge for an EDA environment in the automotive design chain is the management of a large number of players with a different background over a broad spectrum of abstraction levels.

The speech gives an overview over the state of the art, actual developments and experiences in EDA and shows trends for the cars of the future. Finally an outlook will be given about the challenges and chances for EDA as a key enabler for the development of future cars.

Biography: Peter van Staa studied Physics at the Universities of Göttingen and Münster, where he received the diploma in 1977 and the Dr. rer. nat. with a thesis on semiconductor physics in 1983. Subsequently he joined the Microelectronics Division of the Robert Bosch GmbH in Reutlingen. After different management functions in EDA, IC qualification and Test today he heads the cross-functional department which has to provide the enabling technologies for the ASIC-design, namely new tools and methods for automated IC design, EDA-support as well as technology assessment, library development, and IC packaging. In addition he is member of different steering groups in European programs which support the innovation in Microelectronics technologies and design automation.

FAST TRACK 9:30 - 10:00am - ROOM: ALMADEN BALLROOM *Come see a mini preview of the presentations for the day.*

MONDAY, NOVEMBER 3 - 10:30am - 12:00pm

1A Enhancing Correctness of Advanced Design
Room: Almaden 1

Moderators:
Vijay Sundararajan - *Broadcom Corp.*
Jie-Hong (Roland) Jiang - *National Taiwan Univ.*

The first paper of the section addresses the increasing demand of protection of memories against soft and hard errors. A fully automated RTL-based verification flow is proposed. The second paper addresses the validation challenges of HW/SW integration. The approach requires minimum human effort and detects DMA interface bugs in both the devices and drivers. The last paper addresses the runtime complexity issues of CMOS-circuit simulation. The proposed high-throughput switch-level simulator uses GPU parallelization.

1A.1 Automated Detection and Verification of Parity-Protected Memory Elements
Shiri Moran, Eli Arbel, Shlomit Koyfman - *IBM Corp.*
Prabhakar Kudva - *IBM T.J. Watson Research Center*

1A.2 Validating Direct Memory Access Interfaces with Conformance Checking
Li Lei, Kai Cong, Zhenkun Yang, Fei Xie - *Portland State Univ.*

1A.3 Data-Parallel Simulation for Fast and Accurate Timing Validation of CMOS Circuits
Eric Schneider - *Univ. of Stuttgart*
Stefan Holst, Xiaoqing Wen - *Kyushu Institute of Technology*
Hans-Joachim Wunderlich - *Univ. of Stuttgart*

1B CAD for Next-Generation Vehicles
Room: Almaden 2

Moderators:
Wenchao Li - *SRI International*
Armin Wasicek - *Univ. of California, Berkeley*

Design of next-generation vehicles presents many challenges in realtime security, electrical energy efficiency, multi-physical design metrologies/tools, and so forth. In this session, three papers introduce security-aware design methods for TDMA-based systems, reinforcement learning for hybrid electric vehicle energy management, and compilation/high-level synthesis of multi-physical systems for automotive applications.

1B.1 Security-Aware Mapping for TDMA-Based Real-Time Distributed Systems
Chung-Wei Lin - *Univ. of California, Berkeley*
Qi Zhu - *Univ. of California, Riverside*
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley*

1B.2 Reinforcement Learning Based Power Management for Hybrid Electric Vehicles
Xue Lin, **Yanzhi Wang**, Paul Bogdan - *Univ. of Southern California*
Naehyuck Chang - *Korea Advanced Institute of Science and Technology*
Massoud Pedram - *Univ. of Southern California*

1B.3 Functional Modeling Compiler for System-Level Design of Automotive Cyber-Physical Systems
Arquimedes Canedo - *Siemens Corp.*
Jiang Wan, Mohammad Abdullah Al Faruque - *Univ. of California, Irvine*

All speakers are denoted in bold | * - denotes best paper candidate

1C Emerging Reconfigurable Array Technologies
Room: Winchester

Moderator:
Dimin Niu - *Samsung Research America*

This session covers new CAD techniques for emerging reconfigurable array technologies. The first paper discusses BDD based logic synthesis approaches for SET arrays. The next paper performs a design space exploration for emerging vertical resistive memory arrays. The last paper in the session discusses algorithmic techniques to mitigate IR drop issues in memristor based neuromorphic computing arrays.

1C.1 BDD-Based Synthesis of Reconfigurable Single-Electron Transistor Arrays
Zheng Zhao - *Shanghai Jiao Tong Univ.*
Chian-Wei Liu, Chun-Yao Wang - *National Tsing Hua Univ.*
Weikang Qian - *Shanghai Jiao Tong Univ.*

1C.2 Architecting 3D Vertical Resistive Memory for Next-Generation Storage Systems
Cong Xu - *Pennsylvania State Univ.*
Pai-Yu Chen - *Arizona State Univ.*
Dimin Niu - *Samsung Semiconductor, Inc.*
Yang Zheng - *Pennsylvania State Univ.*
Shimeng Yu - *Arizona State Univ.*
Yuan Xie - *Pennsylvania State Univ.*

1C.3 Reduction and IR-Drop Compensations Techniques for Reliable Neuromorphic Computing Systems
Beiye Liu - *Univ. of Pittsburgh*
Xin Li - *Carnegie Mellon Univ.*
Tingwen Huang - *Texas A&M Univ.*
Qing Wu, Mark Barnell - *Air Force Research Lab*
Hai Li, Yiran Chen - *Univ. of Pittsburgh*

All speakers are denoted in bold | * - denotes best paper candidate

1D Designer Track: Challenges and Techniques for High Level Design
Room: Market 1 & 2

Moderator:
Umit Ogras - *Arizona State Univ.*
Organizer:
Frank Liu - *IBM Research - Austin*

With the emerging heterogeneous computing systems, many design decisions are made at high level, involving not only VLSI hardware, but also software and firmware. The first presentation in this Designer Track describes an application driven approach for software and system co-optimization. The second presentation describes a top-down methodology for low-power wearable and IoT systems. The last presentation describes the challenges and progress in system-level power modeling for SoC design.

1D.1 Application Driven High Level Design in the Era of Heterogeneous Computing
Ruchir Puri - *IBM T.J. Watson Research Center*

1D.2 High Level Design for Wearables and IoT
Yatin Hoskote - *Intel Corp.*
Ilya Klotchkov - *Intel Corp.*

1D.3 Towards a Standard Flow for System Level Power Modeling
Nagu Dhanwada - *IBM Corp.*
Rhett Davis - *North Carolina State Univ.*
Jerry Frenkil - *Silicon Integration Initiative, Inc.*

ACM Student Research Competition Poster Session

Room: Santa Clara 1 & 2

Sponsored by Microsoft Research, the ACM Student Research Competition (SRC) is an internationally recognized venue enabling undergraduate and graduate students who are members of ACM and ACM SIGDA to:

- Experience the research world—for many undergraduates this is a first!
- Share research results and exchange ideas with other students, judges, and conference attendees.
- Rub shoulders with academic and industry luminaries.
- Understand the practical applications of their research.
- Perfect their communication skills.
- Receive prizes and gain recognition from ACM, and the greater computing community.

ACM SRC has three rounds: (1) abstract review; (2) poster session (this session); and (3) technical presentation.

In the first round, 2-page research abstracts are evaluated by EDA experts from academia and industry to select participants for the second round (this session). For the ACM SRC at ICCAD 2014 competition, 33 abstracts were received out of which 20 participants were invited to present their research at ICCAD. The posters are evaluated by EDA experts to select 5 participants in graduate and undergraduate categories to advance to the final round (technical presentation round). Students are expected to discuss their work with judges. Each judge will rate the student's visual presentation based on the criteria of uniqueness of the approach, the significance of the contribution, visual presentation, and quality of presentation.

More details can be found at: www.sigda.org/src

Sponsored By:

Microsoft Research

acm Association for Computing Machinery

2A Embedded Tutorial: **Adaptive Designs in Computing, Power Management and Communication for Low-Power Circuits and Systems with Ultra-Wide Dynamic Ranges**

Room: Almaden 1

Moderators:

Arijit Raychowdhury - *Georgia Institute of Technology*
Shreyas Sen - *Intel Corp.*

In this tutorial we will describe current and on-going research on various aspects of low-power adaptive designs targeted for computation, power management as well as communication. In the first half of the tutorial we will focus on various adaptation techniques in typical computing blocks consisting of logic and memory; as well as adaptive control in linear voltage regulators embedded within logic. The second half of the tutorial will focus on the need and role of adaptation in communication circuits. We will describe how system/circuit co-design can lead to adaptive wireless circuits that can adapt to both channel-variations as well as process-variations to enable low-power SISO and MIMO systems using built-in circuit tuning knobs, channel and process sensors and closed loop run-time control. The tutorial will conclude with a summary of the current adaptive techniques and illustrate the need for closed loop control at various levels of the design hierarchy.

2A.1 The Role of Adaptation and Resiliency in Computation and Power Management
Arijit Raychowdhury, Saad Bin Nasir - *Georgia Institute of Technology*
Samantak Gangopadhyay - *Qualcomm India Pvt. Ltd.*

2A.2 Channel-Adaptive Zero-Margin & Process-Adaptive Self-Healing Communication Circuits/Systems
Shreyas Sen - *Intel Corp.*

2B Special Session: **Design, Modeling and Tools for Video Analytics Using Emerging Devices**

Room: Almaden 2

Moderator:

Vijaykrishnan Narayanan - *Pennsylvania State Univ.*

This session will feature design automation tools and modeling support required for enabling complex video analytics tasks. The first talk will provide insight to design challenges and automation efforts in embedding human-like vision intelligence in mobile embedded platforms. The second talk will focus on the transformation and mapping of traditional vision algorithms on brain-like neuromorphic fabrics made of arrays of phase-change memory. The third talk will highlight modeling efforts of large arrays of oscillators in implementing vision algorithms. The fourth talk will reveal on how unique device characteristics of steep slope devices can enhance efficiency of supporting new variants of cellular neural networks. The final talk provides perspective on embedding configurable accelerators for vision.

2B.1 Playing Games with the Development of Machine Vision Algorithms Using ViPER
Benjamin Wheeler - *Naval Surface Warfare Center Dahlgren Division*

2B.2 Mapping Vision Algorithms on a Neuromorphic Array Architecture
Siddarth Joshi - *Univ. of California at San Diego*
S. Burc Eryilmaz - *Stanford Univ.*
Gert Cauwenberghs - *Univ. of California at San Diego*
H.S. Philip Wong - *Stanford Univ.*

2B.3 Modeling Oscillator Arrays for Video Analytic Applications
Yan Fang, Victor V. Yashin, Andrew J. Seel, Donald M. Chiarulli,
Steven P. Levitan - *Univ. of Pittsburgh*
Brandon Jennings - *Univ. of Pittsburgh*
Reggie Barnett - *Univ. of Pittsburgh*

2B.4 Cellular Neural Networks for Image Analysis Using Steep Slope Devices
Indranil Palit, Qiuwen Lou, **X. Sharon Hu**, Joseph Nahas, Michael Niemier, Behnam Sedighi - *Univ. of Notre Dame*

2B.5 A Hardware Accelerated Multilevel Visual Classifier for Embedded Visual-Assist Systems
Matthew Cotter, Siddarth Advani, **Jack Sampson** - *Pennsylvania State Univ.*
Kevin Irick - *Siliconscapes LLC*
Vijaykrishnan Narayanan - *Pennsylvania State Univ.*

All speakers are denoted in bold | * - denotes best paper candidate

2C Patterns and Placement
Room: Winchester

Moderator:

Rani Ghaida - *GLOBALFOUNDRIES*

Printability of layout patterns will continue to be the core issue in design for manufacturability. Methods to tie patterns to more traditional design rule-based flows are in demand. Furthermore, IC manufacturing requires new lithography techniques including triple-patterning and e-beam. Placement is emerging as an important area within these new techniques. The first paper is focused on the fast detection of hotspots (features difficult to print) using incomplete layout patterns. The second and third patterns address layout printability improvements using placement techniques that are well-aware of multiple lithographic patterning. Certain patterns are known to be more optimal, thereby designs are optimized as early as the technology and standard-cell development stage; the last paper targets this problem.

2C.1 DRC-Based Hotspot Detection Considering Edge Tolerance and Incomplete Specification
Yen-Ting Yu - *National Chiao Tung Univ.*
Yumin Zhang - *Synopsys, Inc., Inc.*
Iris Hui-Ru Jiang - *National Chiao Tung Univ.*
Charles Chang - *Synopsys, Inc., Inc.*

2C.2 Triple Patterning Lithography Aware Optimization for Standard Cell Based Design
Jian Kuang, **Wing-Kai Chow**, Evangeline F.Y. Young - *Chinese Univ. of Hong Kong*

2C.3 Triple Patterning Aware Detailed Placement With Constrained Pattern Assignment
Haitong Tian, Yuelin Du - *Univ. of Illinois at Urbana-Champaign*
Hongbo Zhang - *Synopsys, Inc., Inc.*
Zigang Xiao, Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign*

2C.4 Sub-20 nm Design Technology Co-Optimization for Standard Cell Logic
Kaushik Vaidyanathan - *Carnegie Mellon Univ.*
Lars Liebmann - *IBM Corp.*
Andrzej Strojwas, Larry Pileggi - *Carnegie Mellon Univ.*

2D Energy, Performance and Security for Embedded Systems
Room: Market 1 & 2

Moderator:

Yang Ge - *Broadcom Corp.*

Essential to modern Embedded Systems are Energy Efficiency, Performance and Security. The first paper proposes an energy efficient on-chip hybrid architecture. The second improves performance by the use of compressed last level caches. The final two papers examine security issues, the first of which proposes an ultra-small ultra-low power memorister based PUF without helper data and the second advances a high performance and highly flexible cryptographic processor.

2D.1 Energy-Efficient Architecture for Advanced Video Memory
Felipe Sampaio - *Univ. Federal do Rio Grande do Sul*
Muhammad Shafique - *Karlsruhe Institute of Technology*
Bruno Zatt - *Univ. Federal de Pelotas*
Sergio Bampi - *Univ. Federal do Rio Grande do Sul*
Joerg Henkel - *Karlsruhe Institute of Technology*

2D.2 Compaction-Free Compressed Cache for High Performance Multi-Core System
Po-Yang Hsu, Pei-Lan Lin, TingTing Hwang - *National Tsing Hua Univ.*

2D.3 A Non-Volatile Memory Based Physically Unclonable Function Without Helper Data
Wenjie Che - *Univ. of New Mexico*
Swarup Bhunia - *Case Western Reserve Univ.*
Jim Plusquellic - *Univ. of New Mexico*

2D.4 Cryptoraptor: High Throughput Reconfigurable Cryptographic Processor
Gokhan Sayilar - *Univ. of Texas at Austin*
Derek Chiou - *Microsoft Research, Univ. of Texas at Austin*

All speakers are denoted in bold | * - denotes best paper candidate

3A Special Session: **Can One SHIELD Integrated Circuits and Systems from Supply Chain Attacks?**
Room: Almaden 1

Moderator:
Ramesh Karri - *New York Univ.*

Organizers:
Ramesh Karri - *New York Univ.*
Farinaz Koushanfar - *Rice Univ.*

When an indelible and unclonable integrated circuit (IC) identifier is combined with an encryption engine, one can establish a secure communication channel between the IC and an off-chip database for verification of the identifier. This hardware security primitive can support identification, authentication, metering, and tracing of the IC as it makes its way through the potentially untrustworthy semiconductor supply chain. The DARPA SHIELD program is developing a low-cost, low-power, and attack-resilient SHIELD security primitive with these capabilities. This session will highlight the requirements – ability to create an unclonable, indelible, and unique identifier, design of an ultra-low power encryption engine, assessment of realistic threats against the shield, possible metrics to evaluate the security strength of SHIELD against these threats, and ultra-low power defenses against the considered threats.

3A.1 Semiconductor Supply Chain Risks and DARPA SHIELD Program
Saverio Fazzari - *Booz Allen Hamilton, Inc.*

3A.2 BIST-PUF: Online, Hardware-based Evaluation of Physically Unclonable Circuit Identifiers
Farinaz Koushanfar, Siam U. Hussain, Sudha Yellapantula - *Rice Univ.*
Mehrdad Majzoobi - *Mesh Motion Inc.*

3A.3 EDA Perspective on Trojans and Supply Chain Security
Serge Leef - *Mentor Graphics Corporation*

3A.4 Shielding and Securing Integrated Circuits Using Sensors
Davood Shahrjerdi, Jeyavijayan Rajendran, Siddharth Garg - *New York Univ.*
Farinaz Koushanfar - *Rice Univ.*
Ramesh Karri - *New York Univ.*

All speakers are denoted in bold | * - denotes best paper candidate

3B Special Session: **Smart Energy System: Electric Vehicle, Home, HVAC, Hybrid System and Cybersecurity**
Room: Almaden 2

Moderator:
Tsung-Yi Ho - *National Chiao Tung Univ.*

Organizer:
Shiyan Hu - *Michigan Technological Univ.*

Developing smart energy system is a key step towards building a smart grid to improve the flexibility, controlability, reliability, and security of the traditional grid. This special session consists of four invited talks, giving introductions and discussions on a variety of smart energy system related methodologies in a bottom up fashion including smart battery, electric vehicle, smart home, HVAC, smart building and smart power distribution system. In addition, cyber attacks on the smart energy system will be discussed, and a set of novel defense technologies will be developed. The special session will describe in details how the innovative computer aided design techniques can be developed to tackle the new challenges in the circuit, electronics and embedded system modeling and optimization in the smart energy system.

3B.1 Power Consumption Characterization, Modeling and Estimation of Electric Vehicles
Naehyuck Chang, Donkyu Baek, Jeongmin Hong - *KAIST*

3B.2 Vulnerability Assessment and Defense Technology for Smart Home Cybersecurity Considering Pricing Cyberattacks
Yang Liu, **Shiyan Hu** - *Michigan Technological Univ.*
Tsung-Yi Ho - *National Chiao Tung Univ.*

3B.3 Co-Scheduling of HVAC Control, EV Charging and Battery Usage for Building Energy Efficiency
Tianshu Wei, **Qi Zhu** - *Univ. of California, Riverside*
Mehdi Maasoumy - *C3 Energy*

3B.4 Real Time Anomaly Detection in Wide Area Monitoring of Smart Grids
Jie Wu - *Missouri Univ. of Science and Technology*
Jinjun Xiong - *IBM Corp.*
Prasenjit Shil - *Ameren Corp.*
Yiyu Shi - *Missouri Univ. of Science and Technology*

3C Analysis and Optimization of Timing, Noise, and Power
Room: Winchester

Moderators:

Igor Keller - *Cadence Design Systems, Inc.*
Mondira Pant - *Intel Corp.*

This session features four papers dealing with the analysis and the optimization of performance, noise, and power from different perspectives. The first paper deals with the problem of calculating the optimal threshold for on-chip sensors. The second one proposes a power-optimal placement of retention registers for power-gated designs. The third paper a novel graph sparsification approach based on spectral techniques that allows managing very large power grids. The last paper presents a learning-based algorithm to adaptively determine the optimal voltage swing for interconnects in 2.5D circuits.

3C.1 Variation Aware Optimal Threshold Voltage Computation for On-Chip Noise Sensors
Tao Wang, Chun Zhang - *Missouri Univ. of Science and Technology*
Jinjun Xiong - *IBM Research*
Pei-Wen Luo, Liang-Chia Cheng - *Industrial Technology Research Institute*
Yiyu Shi - *Missouri Univ. of Science and Technology*

3C.2 More Effective Power-Gated Circuit Optimization with Multi-Bit Retention Registers
Shu-Hung Lin, **Mark Po-Hung Lin** - *National Chung Cheng Univ.*

3C.3 An Efficient Spectral Graph Sparsification Approach to Scalable Reduction of Large Flip-Chip Power Grids
Xueqian Zhao, Zhuo Feng - *Michigan Technological Univ.*
Cheng Zhuo - *Intel Corp.*

3C.4 Reinforcement Learning based Self-adaptive Voltage-swing Adjustment of 2.5D I/Os for Many-core Microprocessor and Memory Communication
Huang Hantao, **Sai Manoj P.D.** - *Nanyang Technological Univ.*
Dongjun Xu - *Nanyang Technological Univ., Xi'an Univ. of Technology*
Hao Yu - *Nanyang Technological Univ.*
Zhigang Hao - *MediaTek, Singapore Pte. Ltd.*

All speakers are denoted in bold | * - denotes best paper candidate

3D What is Behind the Mask?
Room: Market 1 & 2

Moderators:

Luigi Capodieci - *GLOBALFOUNDRIES*
Ibrahim (Abe) Elfadel - *Masdar Institute of Science and Technology*

Mask design is becoming ever more challenging given the well know limitations on optical lithography and the sensitivity of deeply scaled designs to variations in optical sources. Therefore, mask optimization for optical lithography as well as optimization in other forward- looking techniques such as electron-based lithography are becoming important. The first two papers of this session address the problem of mask optimization in the presence of process variations by proposing fast techniques for minimizing edge placement errors while taking into account process variation bands. The third paper presents optimal benchmarks for evaluating mask fracturing aimed at reducing the number of shots used by mask writers. The final paper is concerned with improving stencil planning in e-beam lithography.

3D.1 Fast Lithographic Mask Optimization Considering Process Variation
Yu-Hsuan Su, Yu-Chen Huang, Liang-Chun Tsai, Yao-Wen Chang - *National Taiwan Univ.*
Shayak Banerjee - *Ambient.me*

3D.2 A Fast Process Variation and Pattern Fidelity Aware Mask Optimization Algorithm
Ahmed Awad, Atsushi Takahashi - *Tokyo Institute of Technology*
Satoshi Tanaka, Chikaaki Kodama - *Toshiba Corp.*

3D.3 Benchmarking of Mask Fracturing Heuristics
Tuck Boon Chan - *Univ. of California at San Diego*
Puneet Gupta - *Univ. of California, Los Angeles*
Kwangsoo Han - *Univ. of California at San Diego*
Abde Ali Kagalwalla - *Univ. of California, Los Angeles*
Andrew Kahng - *Univ. of California at San Diego*
Emile Sahouria - *Mentor Graphics Corporation*

3D.4 Overlapping-Aware Throughput-Driven Stencil Planning for E-Beam Lithography
Jian Kuang, **Evangeline F.Y. Young** - *Chinese Univ. of Hong Kong*

Special Session and Panel: Moore's Law is Dying, Long Live EDA!

Room: Almaden Ballroom

Moderator:

William Joyner - *Semiconductor Research Corp.*

After five decades of continuous progress, scaling has become increasingly difficult due to mounting technology challenges and prohibitive financial costs. The slowdown of scaling has brought big changes in the semiconductor industry landscape, as well as priority shifts in academic research funding. As a key player in enabling the benefits of Moore's Law, EDA is also at a crossroad. Will Moore's Law stop, or it is already dead? Will new technology such as EUV, DSA, or 450mm wafer save Moore's Law? What will the future of EDA look like? Will the new technology bring a big slew of new EDA problems? Will the slowdown give the EDA a good chance to close the "productivity-gap"? There are many questions which need to be answered.

The first part of this special session/panel is a presentation on the findings of CCC workshops on extreme scale design automation. Funded by NSF, this series of workshops lasted three years with the participation of over 50 industry and academic experts. In the second part of the program, six experts from the semiconductor industry, EDA companies and academia will provide their views on what the future looks like for EDA. Audience are welcome to participate in the discussion.

CCC Workshop Presentation: Alex Jones, *Univ. of Pittsburgh*

Panelists:

Todd Austin - *Univ. of Michigan*
Luigi Capodieci - *GLOBALFOUNDRIES*
Patrick Groeneveld - *Synopsys, Inc., Inc.*
Alex Jones - *Univ. of Pittsburgh*
Leon Stok - *IBM Corp.*
Jacob White - *Massachusetts Institute of Technology*

Tuesday, November 4

TIME	ALMADEN 1	ALMADEN 2	WINCHESTER	MARKET 1 & 2
9:00 - 9:30am	**Fast Track:** Tuesday Regular Paper Presentations			
10:00am - 12:00pm	Session 4A: Detection & Prevention of IC Security Threats	Embedded Tutorial 4B: Design Automation for Biochemistry Synthesis on a Digital Microfluidic Lab-on-a-Chip	Session 4C: Runtime Optimizations for Emerging Memory and On-Chip Systems	Session 4D: Noise and Variability
11:45am - 1:15pm	**IEEE CEDA Luncheon Presentation:** Hyatt Hotel - Grand Hall **Teaching EDA at Planetary Scale: Reflections on the First EDA MOOCs** **Rob Rutenbar** - *Univ. of Illinois at Urbana-Champaign* Sponsored: CEDA			
1:30 - 3:00pm	Session 5A: Advanced Verification and Diagnosis Techniques	Special Session 5B: 2014 CAD Contest	Session 5C: Emerging Applications of Networked Cyberphysical Systems	Session 5D: Routing in EDA and Beyond
3:30 - 5:30pm	Special Session 6A: CAD for the Internet of Things	Embedded Tutorial 6B: Full-Chip Electromigration Assessment and System-Level EM Reliability Management	Session 6C: Advances in Logic Synthesis	Session 6D: How to Keep Chip Aging at Bay
5:30 - 6:00pm	**Networking Reception:** Almaden Foyer			
6:00 - 7:15pm	**ACM/SIGDA Member Meeting:** Santa Clara 1 & 2			
6:30 - 9:30pm	**19th Annual Phil Kaufman Award Dinner:** San Jose Marriott *Tickets available at the door.*			

ACM Student Research Competition Technical Presentations: Santa Clara 1 & 2, *3:30 - 5:00pm*

TUESDAY, NOVEMBER 4 - 10:00 - 11:30am

4A Detection & Prevention of IC Security Threats
Room: Almaden 1

Moderators:
Celia Merzbacher - *Semiconductor Research Corp.*
Sandeep Goel - *Taiwan Semiconductor Manufacturing Co., Ltd.*

Are your sure you can trust your chips? Come and discover the latest challenges in security threats. See the latest advances in countermeasures and prevention against IC counterfeiting, hardware Trojans, and reverse engineering.

4A.1 Protecting Integrated Circuits from Piracy with Test-Aware Logic Locking
Stephen Plaza - *Janelia Farm, Howard Hughes Medical Institute*
Igor L. Markov - *Univ. of Michigan*

4A.2 Hardware Obfuscation Using PUF-Based Logic
James Bradley Wendt, Miodrag Potkonjak - *Univ. of California, Los Angeles*

4A.3 On Trojan Side Channel Design and Identification
Jie Zhang - *Chinese Univ. of Hong Kong*
Guantong Su - *Tsinghua Univ.*
Yannan Liu, Lingxiao Wei, **Feng Yuan** - *Chinese Univ. of Hong Kong*
Guoqiang Bai - *Tsinghua Univ.*
Qiang Xu - *Chinese Univ. of Hong Kong*

4B Embedded Tutorial: Design Automation for Biochemistry Synthesis on a Digital Microfluidic Lab-on-a-Chip
Room: Almaden 2

Moderator:
Krishnendu Chakrabarty - *Duke Univ.*
Organizers:
Krishnendu Chakrabarty - *Duke Univ.*
Bhargab B. Bhattacharya - *Indian Statistical Institute*
Ansuman Banerjee - *Indian Statistical Institute*

The emerging microfluidic technology now provides a viable option of automating biochemistry protocols to be implemented on a chip, known as a lab-on-a-chip (LoC). These chips can be used for DNA analysis, toxicity grading, drug design and delivery, for conducting low-cost pathological tests, and for providing a wide range of point-of-care health services. The complexity and safety issues in biochemical assays mandate the use of various design automation tools while building such chips.

In this tutorial, we will introduce the architectures of droplet-based (digital) microfluidic LoC and highlight several optimization issues concerning resource allocation, placement, and droplet routing. Next, we will discuss several algorithms that are used for on-chip sample preparation, and finally, we will demonstrate how the correctness of on-chip protocol realizations can be checked using a formal verification framework.

4B.1 Design Automation for Biochemistry Synthesis on a Digital Microfluidic Lab-on-a-Chip
Krishnendu Chakrabarty - *Duke Univ.*
Bhargab B. Bhattacharya, Ansuman Banerjee - *Indian Statistical Institute*

4C Runtime Optimizations for Emerging Memory and On-Chip Systems

Room: Winchester

Moderators:

Timothy Kam - *Intel Corp.*
Umit Ogras - *Arizona State Univ.*

This session highlights system-level adaptations in emerging memory technologies and router configurations. The first paper provides a epoch-based adaptation for on-chip network connectivity. The second paper provides an adaptive refresh mechanism based on data access patterns for 3D DRAMs. The third paper presents a runtime local checkpointing approach that exploits multi-level cell properties of STT-RAMs.

4C.1 High-Radix On-Chip Networks with Low-Radix Routers
Animesh Jain, Ritesh Parikh, Valeria Bertacco - *Univ. of Michigan*

4C.2 Data-Aware DRAM Refresh to Squeeze the Margin of Retention Time in Hybrid Memory Cube
Yinhe Han, Ying Wang, Huawei Li, Xiaowei Li - *Chinese Academy of Sciences*

***4C.3 Using Multi-Level Cell STT-RAM for Fast and Energy-Efficient Local Checkpointing**
Ping Chi, Cong Xu - *Pennsylvania State Univ.*
Tao Zhang - *NVIDIA Corp.*
Xiangyu Dong - *Google, Inc.*
Yuan Xie - *Pennsylvania State Univ.*

4D Noise and Variability

Room: Market 1 & 2

Moderators:

Chirayu Amin - *Intel Corp.*
Eric Keiter - *Sandia National Laboratories*

The session focuses on advanced simulation techniques for capturing noise and variability in circuits. The first paper introduces rigorous models of random telegraph and 1/f noise that are compatible with non-Monte Carlo simulation techniques. The next two papers describe advanced sampling techniques, one focusing on computing statistical moments, the other capturing rare SRAM failure events.

***4D.1 Modeling and Analysis of Nonstationary Low-Frequency Noise in Circuit Simulators: Enabling Non Monte Carlo Techniques**
Ahmet Gokcen Mahmutoglu, Alper Demir - *Koc Univ.*

4D.2 MPME-DP: Multi-Population Moment Estimation via Dirichlet Process for Efficient Validation of Analog/Mixed-Signal Circuits
Manzil Zaheer, Xin Li - *Carnegie Mellon Univ.*
Chenjie Gu - *Intel Corp.*

***4D.3 Fast Statistical Analysis of Rare Circuit Failure Events via Subset Simulation in High-Dimensional Variation Space**
Shupeng Sun, Xin Li - *Carnegie Mellon Univ.*

Invited Luncheon Keynote

Sponsored by: CEDA

CEDA Teaching EDA at Planetary Scale: Reflections on the First EDA MOOCs

Room: Hyatt Hotel - Grand Hall

Rob Rutenbar - *Univ. of Illinois at Urbana-Champaign*

It is IEEE CEDA's greatest honor to have Prof. Rob Rutenbar, Head of the Computer Science Department of Univ. of Illinois at Urbana–Champaign as the invited Keynote speaker for their luncheon.

Summary of Talk: Massive Open Online Courses (MOOCs) can deliver advanced class material at planetary scale, combining internet-based video and cloud-based assignments. In 2013, I taught the world's first EDA MOOC, called "VLSI CAD: Logic to Layout", based on 20 years teaching EDA the traditional way. In 2014, I offered the MOOC again. Over 25,000 learners registered for these MOOCs – a number amazingly close to the total estimated population of EDA professionals on planet Earth. This talk summarizes my experience designing and delivering this material at this unprecedented scale: how we covered the key algorithms of a standard ASIC flow; how we architected cloud solutions that let students work with tools and automatically grade realistic software projects. Finally, I will discuss what MOOCs could mean to the future of EDA as a discipline.

Biography: Rob A. Rutenbar received the PhD in 1984 from the Univ. of Michigan, and spent the next 25 years on the faculty at Carnegie Mellon. In 1998 he cofounded Neolinear, Inc. to commercialize tools for custom analog, and served as Chief Scientist until its acquisition by Cadence in 2004. He has also worked extensively on nanoscale statistics. Since 2010 he is Head of Computer Science at the Univ. of Illinois at Urbana-Champaign. He has won many awards, including 3 DAC Best Papers, and an SRC Aristotle Award for the impact of his students on the US Semiconductor industry. His work has been featured in venues ranging from EETimes to the Economist.

5A Advanced Verification and Diagnosis Techniques
Room: Almaden 1

Moderators:
Miroslav Velev - *Aries Design Automation, LLC*
Rolf Drechsler - *Univ. of Bremen*

This session gives three interesting papers which advance the state-of-the-art of formal analysis and diagnosis methodologies. The first paper introduces an effective method which significantly reduces the complexity of formal analysis by generating sequential embedding of a concurrent program. The second paper introduces a general framework for formal analysis of probabilistic design and gives connections between probabilistic property analysis and existing solving techniques. The third paper presents a novel interpolation-based framework which formalizes the propagation of state information across timing widows in execution traces targeting silicon fault diagnosis.

5A.1 Removing Concurrency for Rapid Functional Verification
Stephen Longfield, Jr. - *Cornell Univ.*
Rajit Manohar - *Cornell Tech*

5A.2 Towards Formal Evaluation and Verification of Probabilistic Design
Nian-Ze Lee, **Jie-Hong Roland Jiang** - *National Taiwan Univ.*

5A.3 Silicon Fault Diagnosis Using Sequence Interpolation with Backbones
Charlie Shucheng Zhu - *Princeton Univ.*
Georg Weissenbacher - *Vienna Univ. of Technology*
Sharad Malik - *Princeton Univ.*

5B Special Session: 2014 CAD Contest
Room: Almaden 2

Moderators:
Iris Hui-Ru Jiang - *National Chiao Tung Univ.*
Natarajan Viswanathan - *IBM Systems and Technology Group*

Organizers:
Tai-Chen Chen - *National Central Univ.*
Jin-Fu Li - *National Central Univ.*

Contests and their benchmarks have become an important driving force to push our EDA domain forward in different areas lately.

The CAD Contest at ICCAD originates from the Taiwan CAD Contest and has been internationalized under the joint sponsorship of IEEE CEDA and Taiwan MOE since 2012. Continuing its great success in 2012 and 2013, the 2014 CAD contest attracts 93 teams from 9 regions. Three contest problems on verification, incremental placement, and mask optimization are called for competition this year.

This session presents the three contest problems, releases their benchmarks, and announces the contest results. This session also provides a forum for top final teams to disclose their key ideas and algorithms through video presentations.

5B.1 The Overview of 2014 CAD Contest at ICCAD
Iris Hui-Ru Jiang - *National Chiao Tung Univ.*
Natarajan Viswanathan - *IBM Systems and Technology Group*
Tai-Chen Chen, Jin-Fu Li - *National Central Univ.*

5B.2 ICCAD-2014 CAD Contest in Simultaneous CNF Encoder Optimization with SAT Solver Setting Selection and Benchmark Suite
Chih-Jen Hsu, Wei-Hsun Lin, Chi-An Wu - *Cadence Design Systems, Inc.*
Kei-Yong Khoo - *Cadence Design Systems, Inc.*

5B.3 ICCAD-2014 CAD Contest in Incremental Timing-Driven Placement and Benchmark Suite
Myung-Chul Kim - *IBM Systems and Technology Group*
Jin Hu - *IBM Systems and Technology Group*
Natarajan Viswanathan - *IBM Systems and Technology Group*

5B.4 ICCAD-2014 CAD Contest in Design for Manufacturability Flow for Advanced Semiconductor Nodes and Benchmark Suite
Rasit O. Topaloglu - *IBM Systems and Technology Group*

All speakers are denoted in bold | * - denotes best paper candidate

5C Emerging Applications of Networked Cyberphysical Systems

Room: Winchester

Moderators:

Arquimedes Canedo - *Siemens Corp.*
Shiyan Hu - *Michigan Technological Univ.*

Use of networked cyberphysical systems creates design challenges but can provide great opportunities beyond conventional design methods. This session introduces power management techniques of mobile devices using the cloud environment and smart grid optimization based on CAD technologies.

5C.1 Optimal Offloading Control for a Mobile Device Based on a Realistic Battery Model and Semi-Markov Decision Process
Shuang Chen, Yanzhi Wang, Massoud Pedram - *Univ. of Southern California*

5C.2 A Learning-on-Cloud Power Management Policy for Smart Devices
Gung-Yu Pan, Bo-Cheng Charles Lai, Sheng-Yen Chen - *National Chiao Tung Univ.*
Jing-Yang Jou - *National Central Univ. and National Chiao Tung Univ.*

5C.3 Smart Grid Load Balancing Techniques via Simultaneous Switch/Tie-line/Wire Configurations
Iris Hui-Ru Jiang - *National Chiao Tung Univ.*
Gi-Joon Nam - *IBM Research*
Hua-Yu Chang - *National Taiwan Univ.*
Sani R. Nassif - *Radyalis LLP*
Jerry Hayes - *IBM Research*

5D Routing in EDA and Beyond

Room: Market 1 & 2

Moderators:

Yih-Lang Li - *National Chiao Tung Univ.*
Li Li - *Synopsys, Inc., Inc.*

This session presents routing techniques in EDA and Biochips. The first paper presents a multithreaded parallel technique to speed up the congestion estimation with any global router. The second paper provides a multi-commodidty flow formulation for detailed router. The last paper proposes to apply SAT Modulo Theory (SMT) to solve the routing problem for digital microfluidic biochips.

5D.1 A Resource-Level Parallel Approach for Global-Routing-Based Routing Congestion Estimation and a Method to Quantify Estimation Accuracy
Wen-Hao Liu - *Cadence Design Systems, Inc.*
Zhen-Yu Peng, Ting-Chi Wang - *National Tsing Hua Univ.*

5D.2 MCFRoute: A Detailed Router Based on Multi-Commodity Flow Method
Xiaotao Jia, Yici Cai, Qiang Zhou - *Tsinghua Univ.*
Gang Chen, Zhuoyuan Li, Zuowei Li - *Nimbus Automation Technologies*

5D.3 Exact Routing for Digital Microfluidic Biochips with Temporary Blockages
Oliver Keszocze, **Robert Wille**, Rolf Drechsler - *Univ. of Bremen*

ACM Student Research Competition Technical Presentations

Room: Santa Clara 1 & 2

Organizers:

Miroslav Velev - *Aries Design Automation, LLC*
Tsung-Yi Ho - *National Cheng Kung Univ.*

The ACM Student Research Competition allows both graduate and undergraduate students to discuss their research with student peers, as well as academic and industry researchers, in an informal setting, while enabling them to attend ICCAD.

This session is the final round of ACM SRC at ICCAD 2014. Each student will present for 10 minutes, followed by a 5-minute question and answer period. This session will be attended by the evaluators and any interested conference attendees. The top three winners in each category will be chosen based on these presentations.

The undergraduate and graduate finalists will be eligible to compete in the ACM SRC Grand Finals to be held in June 2015.

More details can be found at: www.sigda.org/src

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6A Special Session: **CAD for the Internet of Things**

Room: Almaden 1

Moderator:
Farinaz Koushanfar - *Rice Univ.*

Organizer:
Miodrag Potkonjak - *Univ. of California, Los Angeles*

The Internet of Things (IoT) is the next big research and development frontier. Cisco estimates that there will be 50 billion IoT devices connected to the Internet by 2020. Currently there are 2 billion desktops and 5 billion mobile phones. Applications will include medical devices, car electronics, embedded sensing systems, personal wearable gadgets, and home electronics.

This session aims to provide the initial impetus for creators and developers of CAD concepts, algorithms, models, and tool developers to prepare for the new technological revolution. The three papers will provide survey of CAD tasks pertinent for design and analysis of IoT devices and systems, requirement and opportunities related to IoT security, privacy, and trust issues with emphasis on hardware-based techniques, and essential issues with respect to development of IoT embedded software.

6A.1 Design Things for the Internet of Things -- An EDA Perspective
Gang Qu - *Univ. of Maryland*
Lin Yuan - *Atoptech, Inc.*

6A.2 Security of IoT systems: Design Challenges and Opportunities
Teng Xu, **James B. Wendt**, Miodrag Potkonjak - *Univ. of California, Los Angeles*

6A.3 Towards a Rich Sensing Stack for IoT Devices
Chenguang Shen, Haksoo Choi, Supriyo Chakraborty, Mani Srivastava - *Univ. of California, Los Angeles*

6B Embedded Tutorial: **Full-Chip Electromigration Assessment and System-Level EM Reliability Management**

Room: Almaden 2

Moderator:
Valeriy Sukharev - *Mentor Graphics Corporation*

Organizer:
Sheldon Tan - *Univ. of California, Riverside*

Electromigration (EM)-induced reliability becomes a major design constraint in the current and future nanometer VLSI technologies. But existing EM models and assessment techniques based on Black's and Blech equations lead to conservative and over design solutions, which will be no longer an option in current and future technologies because 2X-3X added guard bands required from the over design will significantly increase the buffer sizes and many other aspects of chips, which will lead to substantially increasing costs and powers of the chips

In this embedded tutorial, we first describe a novel approach and technique for chip-scale IR-drop based electromigration assessment considering the parametric failure of power grid networks. Then we will present a new technique to optimize the lifetime of embedded systems considering the electromigration effects by dynamic power management. Finally, we present a technique for accurate simulation of the power map, current densities, temperature, and IR-drop for accurate electromigration assessment.

6B.1 IR-Drop Based Electromigration Assessment: Parametric Failure Chip-Scale Analysis
Valeriy Sukharev - *Mentor Graphics Corporation*
Xin Huang, Haibao Chen, Sheldon Tan - *Univ. of California, Riverside*

6B.2 Lifetime Optimization for Real-Time Embedded Systems Considering Electromigration Effects
Taeyoung Kim, Bowen Zheng, Haibao Chen, Qi Zhu - *Univ. of California, Riverside*
Valeriy Sukharev - *Mentor Graphics Corporation*
Sheldon Tan - *Univ. of California, Riverside*

6B.3 Accurate Full-Chip Estimation of Power Map, Current Densities and Temperature for EM Assessment
Marko Chew, Ara Aslyan, Jun-ho Choy, Xin Huang - *Mentor Graphics Corporation*

All speakers are denoted in bold | * - denotes best paper candidate

6C Advances in Logic Synthesis
Room: Winchester

Moderators:
Sergio Bampi - *Univ. Federal do Rio Grande do Sul*
Li-C Wang - *Univ. of California, Berkeley*

This session presents recent advances in logic synthesis. The first paper proposes a novel gate-to-gate transformation from a combinational circuit to a delay-insensitive asynchronous circuit. The second paper presents a method of integrating physically unclonable functions to maximize the joint entropy and minimize the physical overhead. The third paper presents a new technique for restructuring circuits based on Shannon expansion and Craig Interpolation. The final paper deals with synthesis for memristor circuits.

6C.1 TonyChopper: A Desynchronization Package
Zhao Wang - *Univ. of Texas at Dallas*
Xiao He - *Cisco Systems, Inc.*
Carl Sechen - *Univ. of Texas at Dallas*

6C.2 SuperPUF: Integrating Heterogeneous Physically Unclonable Functions
Michael Wang, Andrew Yates, **Igor L. Markov** - *Univ. of Michigan*

***6C.3 Constrained Interpolation for Guided Logic Synthesis**
Ana Petkovska, David Novo - *Ecole Polytechnique Fédérale de Lausanne*
Alan Mishchenko - *Univ. of California, Berkeley*
Paolo Ienne - *Ecole Polytechnique Fédérale de Lausanne*

6C.4 Logic Synthesis and a Generalized Notation for Memristor-Realized Material Implication Gates
Anika Raghuvanshi, Marek Perkowski - *Portland State Univ.*

6D How to Keep Chip Aging at Bay
Room: Market 1 & 2

Moderator:
Zhiru Zhang - *Cornell Univ.*
Eli Chiprout - *Intel Corp.*

Parameter shift due to aging and variations continues to be a real threat to modern circuit reliability. This session presents practical solutions to model, simulate, monitor and adaptively manage these undesirable phenomena. The first paper presents a holistic approach to model multiple sources of chip aging. The second paper focuses on interconnect electromigation issues in standard cells. A sensor calibration method is discussed in the third paper, while the fourth paper accomplishes efficient sensorless variation estimation through inference.

6D.1 Towards Interdependencies of Aging Mechanisms
Hussam Amrouch, Victor M. van Santen, Thomas Ebi, Volker Wenzel, Joerg Henkel - *Karlsruhe Institute of Technology*

6D.2 A Systematic Approach for Analyzing and Optimizing Cell-Internal Signal Electromigration
Gracieli Posser - *Univ. Federal do Rio Grande do Sul*
Vivek Mishra - *Univ. of Minnesota*
Palkesh Jain - *Texas Instruments, Inc.*
Ricardo Reis - *Univ. Federal do Rio Grande do Sul*
Sachin S. Sapatnekar - *Univ. of Minnesota*

6D.3 ReSCALE: Recalibrating Sensor Circuits for Aging and Lifetime Estimation Under BTI
Deepashree Sengupta, Sachin S. Sapatnekar - *Univ. of Minnesota*

6D.4 Sensorless Estimation of Global Device-Parameters Based on Fmax Testing
Michihiro Shintani, Takashi Sato - *Kyoto Univ.*

ACM/SIGDA Event

Room: Santa Clara 1 & 2

The annual ACM/SIGDA Member Meeting will be held on Tuesday evening from 6:00 - 7:15pm. The meeting is open to everyone in the EDA community and we especially encourage ACM SIGDA members (or those considering becoming members) to attend. Light Hors d'oeuvres and beverages will be served.

The meeting will begin with a brief overview of our group, including its organization, activities, volunteering opportunities, member benefits, etc. We will then introduce this year's SIGDA Pioneering Achievement award recipient, Professor John Hayes. With this award, he is being recognized for his pioneering work in logic design, fault tolerant computing, and testing for electronic design automation. Once introduced, Prof. Hayes will present an informal talk on his work.

Finally, we will end the evening with the announcement of this year's winners of the ACM design automation Student Research Competition taking place at this year's ICCAD. We hope to see you there!

Sponsored By:

Wednesday, November 5

TIME	ALMADEN BALLROOM			
8:30 - 9:30am	**Keynote Address:** **What Role Can Hardware Design Play in Cybersecurity?** **Srinivas Devadas**, *Massachusetts Institute of Technology*			
TIME	**ALMADEN 1**	**ALMADEN 2**	**WINCHESTER**	**MARKET 1 & 2**
9:30 - 10:00am	**Fast Track: Wednesday Regular Paper Presentations**			
10:30am - 12:00pm	Session 7A: Approximate and Stochastic Circuits	Session 7B: Cool Technologies for Cool Chips	Session 7C: Design and CAD to Enable 3D Integration	Designer Track 7D: DFM for Extreme Technology Nodes
12:00 - 1:00pm	**Lunch:** Hyatt Hotel - Grand Hall			
1:30 - 3:30pm	Embedded Tutorial 8A: Automated and Quality-Driven Requirement Engineering	Special Session 8B: Pessimism Removal During Timing Analysis	Session 8C: Emulation, Modeling and Simulation of Analog Systems	Session 8D: Advanced Placement
4:00 - 5:30pm	Special Session 9A: Advances in Debug and Formal Verification	Session 9B Mathematical Methods for Interconnect Modeling and Low Power Design	Session 9C: Software for Management of Parallelism and Data Integrity in Embedded Systems	Session 9D: Clock Network Design and Timing
5:30 - 6:00pm	**Networking Reception:** Almaden Foyer			

Keynote

What Role Can Hardware Design Play in Cybersecurity?

Srinivas Devadas - *Massachusetts Institute of Technology*

Room: Almaden Ballroom

Nary a day goes by without hearing about break-ins into software systems, with personal or confidential data being compromised. Yet, as time goes on, we are trusting the cloud more and more to perform sensitive operations for us. emanding more trust in software systems appears to be a recipe for disaster.

Can hardware rescue us? Suppose we only trust hardware manufacturers and cryptographers, and not system software developers, application programmers, or other software vendors. It will be the hardware manufacturer's job to produce a piece of hardware that provides some security properties. The additional physical security that comes with hardware is a bonus; however, there is still a leap of faith! We must trust that the hardware's security guarantees really do take software out of the loop.

This poses a challenging problem. Software that operates on our data is assumed to be curious or malicious. To make matters worse, the cloud service provider can also be malicious and can run whatever program it wants on our data. How can we ensure privacy of data despite the practically infinite number of malicious programs out there? In this talk, processor architectures being developed in academia and industry will be described that are attempting to address cybersecurity and privacy challenges through innovative hardware design.

Biography: Srinivas Devadas is the Webster Professor of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology (MIT). He received his MS and PhD from the Univ. of California, Berkeley in 1986 and 1988, respectively. He joined MIT in 1988 and served as Associate Head of the Department of Electrical Engineering and Computer Science, with responsibility for Computer Science, from 2005 to 2011. Devadas's research interests span Computer-Aided Design (CAD), computer security and computer architecture. In CAD, his work on logic synthesis and power estimation resulted in several best paper awards at the Design Automation Conference and in IEEE Transactions. Devadas was elected a Fellow of the IEEE in 1999 for contributions to design automation. He received the IEEE Computer Society Technical Achievement Award in 2014 for inventing Physical Unclonable Functions and single-chip secure processor architectures. Devadas's work on hardware information flow tracking published in the 2004 ASPLOS received the ASPLOS Most Influential Paper Award in 2014.

WEDNESDAY, NOVEMBER 5 - 10:30am - 12:00pm

7A Approximate and Stochastic Circuits
Room: Almaden 1

Moderators:

Sergio Bampi - *Univ. Federal do Rio Grande do Sul*
Iris Hui-Ru Jiang - *National Chiao Tung Univ.*

This session presents innovations in approximate and stochastic circuits. Approximate circuits allow precision to be trade-off for improvements in area, delay and power. Stochastic circuits use random bitstreams to encode values -- the value encoded is the probability any given bit of the stream is 1. The first paper describes multi-level logic synthesis techniques for approximate circuits that handle user-provided constraints on error magnitudes and frequency. The second paper describes models for the error characteristics of approximate adders and presents a new approximate adder design. The last paper offers an approach to reduce the silicon area required to generate multiple stochastic bitstreams having different probabilities.

7A.1 Multi-Level Approximate Logic Synthesis Under General Error Constraints
Jin Miao, Andreas Gerstlauer, Michael Orshansky - *Univ. of Texas at Austin*

7A.2 On Error Modeling and Analysis of Approximate Adders
Li Li - *Synopsys, Inc., Inc.*
Hai Zhou - *Northwestern Univ.*

7A.3 Generating Multiple Correlated Probabilities for MUX-Based Stochastic Computing Architecture
Yili Ding, Yi Wu, **Weikang Qian** - *Shanghai Jiao Tong Univ.*

7B Cool Technologies for Cool Chips
Room: Almaden 2

Moderators:

Ravishankar Rao - *Synopsys, Inc.*
Muhammad Shafique - *Karlsruhe Institute of Technology*

Thermal management is critical to virtually all chips and electronic systems, from mobile devices to supercomputers. The papers in this session present various technologies for thermal modeling and management. The first paper proposes a modeling framework for an integrated microfludic cooling and power delivery system. The second paper deals with thermoelectric cooling and integrates a thermal simulator with thermoelectric device models. The third paper improves the accuracy of thermal measurements of integrated circuits by modeling thermal emissivity.

7B.1 PowerCool: Simulation of Integrated Microfluidic Power Generation in Bright Silicon MPSoCs
Arvind Sridhar - *IBM Research and Ecole Polytechnique Fédérale de Lausanne*
Mohamed M. Sabry - *Ecole Polytechnique Fédérale de Lausanne*
Patrick Ruch - *IBM Research*
David Atienza - *Ecole Polytechnique Fédérale de Lausanne*
Bruno Michel - *IBM Research*

7B.2 Workload Dependent Evaluation of Thin-Film Thermoelectric Devices for On-Chip Cooling and Energy Harvesting
Sri Harsha Choday, Kon-Woo Kwon, Kaushik Roy - *Purdue Univ.*

7B.3 Fast and Accurate Emissivity and Absolute Temperature Maps Measurement for Integrated Circuits
Hsueh-Ling Yu - *Industrial Technology Research Institute*
Yih-Lang Li - *National Chiao Tung Univ.*
Tzu-Yi Liao - *GEL/ITRI*
Tianchen Wang, Yiyu Shi - *Missouri Univ. of Science and Technology*
Shu-Fei Tsai - *Industrial Technology Research Institute*

7C Design and CAD to Enable 3D Integration
Room: Winchester

Moderators:
Hai Li - *Univ. of Pittsburgh*
Siddharth Garg - *Univ. of Waterloo*

This session focuses on the design and CAD skills for emerging vertical structures. The first paper discusses a layout CAD flow for vertical channel devices. The second paper talks how to efficiently integrate photonic ring resonators in the vertical structure and alleviate the thermal issue. The third paper expands the discussion to full chip power delivery network in 3D ICs.

7C.1 Efficient Layout Generation and Evaluation of Vertical Channel Devices
Wei-Che Wang, Puneet Gupta - *Univ. of California, Los Angeles*

7C.2 Thermal-Aware Synthesis of Integrated Photonic Ring Resonators
Christopher Condrat - *Calypto Design Systems, Inc.*
Priyank Kalla, Steve Blair - *Univ. of Utah*

7C.3 Full Chip Impact Study of Power Delivery Network Designs in Monolithic 3D ICs
Sandeep Kumar Samal - *Georgia Institute of Technology*
Kambiz Samadi, Pratyush Kamal, Yang Du - *Qualcomm Technologies, Inc.*
Sung Kyu Lim - *Georgia Institute of Technology*

7D Designer Track: DFM for Extreme Technology Nodes
Room: Market 1 & 2

Moderator:
David Pan - *Univ. of Texas at Austin*
Organizer:
Frank Liu - *IBM Research - Austin*

As the technology approaches 10nm process nodes and beyond, complex Design-for-Manufacturability techniques and processes have to be adopted to ensure the correctiveness and yield of the semiconductor product. In this designer track session, three industrial presenters will describe the challenges and solutions from different perspectives.

7D.1 Evolving Physical Design Paradigms in the Transition from 20/14 to 10nm Process Technology Nodes
Luigi Capodieci - *GLOBALFOUNDRIES*

7D.2 Design and Manufacturing Process Co-optimization in Nano-Technology
Meng-Kai Hsu, Nitesh Katta, Tzu-Hen Lin, Yen-Hung Lin, King Ho Tam, **Chung-Hsing Wang** - *Taiwan Semiconductor Manufacturing Co., Ltd.*

7D.3 Design and Technology Co-Optimization Near Single-Digit Nodes
Lars Liebmann, **Rasit Topaloglu** - *IBM Corp.*

8A

Embedded Tutorial: **Automated and Quality-Driven Requirement Engineering**
Room: Almaden 1

Moderator:
Robert Wille - *Univ. of Bremen*

Organizer:
Robert Wille - *Univ. of Bremen*

The design flow for complex safety critical systems starts way before the implementation phase. A considerate amount of time is spent on extracting and organizing requirements from several documents that are provided by the stakeholders and customers. This process is called requirement engineering and usually carried out manually thus far. Some software tools, in particular IBM Rational DOORS1, are available that mainly focus on providing methods to organize requirements and link them to artifacts of the design flow. Besides extracting and organizing requirements, designers also link them to model elements, code blocks, and verification plans such they can be traced during the implementation phase. In this tutorial, we present (automatic) methods which ease this flow, i.e. (i) analysis schemes checking whether requirements are indeed formulated according to proper guidelines, (ii) automatic approaches for the extraction of requirements from customer specifications, and (iii) verification methods that check the extracted requirements for consistency. Natural language processing tools and formal methods are used for this purpose.

8A.1 Automated and Quality-Driven Requirement Engineering
Rolf Drechsler, Mathias Soeken, Robert Wille - *Univ. of Bremen*

8B

Special Session: **Pessimism Removal During Timing Analysis**
Room: Almaden 2

Moderator:
Jin Hu - *IBM Corp.*

Organizers:
Jin Hu - *IBM Corp.*
Debjit Sinha - *IBM Corp.*
Igor Keller - *Cadence Design Systems, Inc.*
Chirayu Amin - *Intel Corp.*

Static timing analysis is a key component of any integrated circuit (IC) chip design-closure flow, and is employed (i) to obtain bounds on the fastest (early) and slowest (late) signal transition times for various timing tests and paths and (ii) drive various physical synthesis and physical design optimizations. Growing chip design sizes and complexities (e.g., increased number of clock domains, increased significance of crosstalk coupling, voltage islands), as well as more complex and accurate timing models (e.g., current source models) lead to longer timing analysis run-times, thereby hindering designer productivity.

Trade-offs are naturally performed on timing model complexity to achieve practical turnaround-times for chip static timing analysis. To margin against the ignored (or traded-off or uncertain) modeling limitations that are not explicitly and accurately modeled in the native timing models, early and late signal propagation delays (for both gates and wires) are made further pessimistic by the addition of extra guard bands. While these forced early-late splits provide the desired safety margins, applying the splits for the full path of some timing test introduces excessive and undesired pessimism if the data path shares an overlap with the clock path. Common path pessimism removal (CPPR) attempts to remove this pessimism by tracing these potentially problematic paths and discarding some of the early-late difference along the common sub-path. This session will showcase the techniques and methods used by the top-performing contestants of the TAU 2014 Timing Contest to perform CPPR.

8B.1 TAU 2014 Contest on Removing Common Path Pessimism during Timing Analysis
Jin Hu, Debjit Sinha - *IBM Corp.*
Igor Keller - *Cadence Design Systems, Inc.*

8B.2 Common Path Pessimism Removal: An Industry Perspective
Vibhor Garg - *Cadence Design Systems, Inc.*

8B.3 Fast Path-Based Timing Analysis for CPPR
Tsung-Wei Huang, Pei-Ci Wu, Martin D.F. Wong
Univ. of Illinois at Urbana-Champaign

8B.4 iTimerC: Common Path Pessimism Removal Using Effective Reduction Methods
Yu-Ming Yang, Yu-Wei Chang, Iris Hui-Ru Jiang - *National Chiao Tung Univ.*

8B.5 TKtimer: Fast & Accurate Clock Network Pessimism Removal
Christos Kalonakis, Charalampos Antoniadis, **Panagiotis Giannakou**, Dimos Dioudis - *Univ. of Thessaly*
George Pinitas - *Delft Univ. of Technology*
George Stamoulis - *Univ. of Thessaly*

8C Emulation, Modeling and Simulation of Analog Systems

Room: Winchester

Moderators:

Ting Mei - *Sandia National Labs*
Jaijeet Roychowdhury - *Univ. of California, Berkeley*

The first two papers present formulations for analysing the steady-state and transient behavior of oscillatory systems. The third paper describes a technique for embedding high-frequency nonidealities in a standard BSIM model using measurement data. The final paper describes a technique for mapping behavioral models of AMS systems onto FPGAs for fast emulation.

8C.1 A Novel Linear Algebra Method for the Determination of Periodic Steady States of Nonlinear Oscillators
Haotian Liu, Kim Batselier, Ngai Wong - *Univ. of Hong Kong*

8C.2 A Unifying and Robust Method for Efficient Envelope-Following Simulation of PWM/PFM DC-DC Converters
Ya Wang, Peng Li, Suming Lai - *Texas A&M Univ.*

8C.3 Large-Signal MOSFET Modeling Using Frequency-Domain Nonlinear System Identification
Moning Zhang, Yang Tang, Zuochang Ye - *Tsinghua Univ.*

8C.4 Pragma-Based Floating-to-Fixed Point Conversion for the Emulation of Analog Behavioral Models
Frank Austin Nothaft, Luis Fernandez, Stephen Cefali, Nishant Shah, Luke Darnell, Jacob Rael - *Broadcom Corp.*

8D Advanced Placement

Room: Market 1 & 2

Moderators:

Ismail Bustany - *Mentor Graphics Corporation*
Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign*

In this session, we have four interesting papers on circuit placement. The first one gives a Lagrangian Relaxation method to solve the asynchronous circuit placement problem. The second one is on large scale FPGA packing and placement. The third paper is placement for regularity. The last one is power clamp placement for ESD protection.

***8D.1 Asynchronous Circuit Placement by Lagrangian Relaxation**
Gang Wu, Tao Lin - *Iowa State Univ.*
Hsin-Ho Huang - *Univ. of Southern California*
Chris Chu - *Iowa State Univ.*
Peter Beerel - *Univ. of Southern California*

8D.2 Efficient and Effective Packing and Analytical Placement for Large-Scale Heterogeneous FPGAs
Yu-Chen Chen - *National Taiwan Univ.*
Sheng-Yen Chen - *National Chiao Tung Univ.*
Yao-Wen Chang - *National Taiwan Univ.*

8D.3 A Hierarchical Approach for Generating Regular Floorplans
Javier De San Pedro, Jordi Cortadella, Antoni Roca - *Univ. Politècnica de Catalunya*

8D.4 Planning and Placing Power Clamps for Effective CDM Protection
Hsin-Chun Lin - *National Chiao Tung Univ. and Global Unichip Corp.*
Shih-Ying Liu, Hung-Ming Chen - *National Chiao Tung Univ.*

9A Special Session: Advances in Debug and Formal Verification

Room: Almaden 1

Moderator:
Yirng-An Chen - *Marvell Semiconductor, Inc.*

Organizer:
Miroslav Velev - *Aries Design Automation, LLC*

The four papers in the session present recent advances in debug and formal verification. The first paper, entitled "On Application of Data Mining Methods in Functional Debug," investigates the use of data mining in functional debug of microprocessors. The second paper, entitled "Improving the Efficiency of Automated Debugging of Pipelined Microprocessors by Symmetry Breaking in Modular Schemes for Boolean Encoding of Cardinality," presents a method for symmetry breaking when encoding cardinality constraints in debug of pipelined microprocessors that are formally verified by Correspondence Checking and exploiting the property of Positive Equality. The third paper, entitled "Multiple Clock Domain Synchronization in a QBF-based Verification Environment," introduces a novel framework for verifying designs with multiple clocks using Quantified Boolean satisfiability (QBF). The fourth paper, entitled "Probabilistic Model Checking for Comparative Analysis of Automated Air Traffic Control System Configurations," explores techniques for probabilistic model checking of the Automated Airspace Concept (AAC) system.

9A.1 On Application of Data Mining in Functional Debug
Kuo-Kai Hsieh, Wen Chen, **Li-C. Wang** - *Univ. of California, Santa Barbara*
Jayanta Bhadra - *Freescale Semiconductor, Inc.*

9A.2 Improving the Efficiency of Automated Debugging of Pipelined Microprocessors by Symmetry Breaking in Modular Schemes for Boolean Encoding of Cardinality
Miroslav Velev, Ping Gao - *Aries Design Automation, LLC*

9A.3 Multiple Clock Domain Synchronization in a QBF-Based Verification Environment
Djordje Maksimovic, Bao Le, **Andreas Veneris** - *Univ. of Toronto*

9A.4 Probabilistic Model Checking for Comparative Analysis of Automated Air Traffic Control System
Yang Zhao - *Microsoft Corp.*
Kristin Yvonne Rozier - *NASA*

9B Mathematical Methods for Interconnect Modeling and Low Power Design

Room: Almaden 2

Moderators:
Wenjian Yu - *Tsinghua Univ.*
Eli Chiprout - *Intel Corp.*

This session contains papers addressing mathematical methods in the areas of interconnect modeling and low power design. The first paper develops a nonlinear zonotoped macromodel for verifying high-speed I/O links under variations, able to generate worst-case eye diagram parameters with small error and much faster than Monte Carlo. The second paper addresses accurate parasitic extraction for high-density cylindrical ITVs by efficient techniques based on the floating random walk method, consuming much less memory than Monte Carlo methods. The third paper presents a self-learning methodology leading to optimal configurations for channel-adaptive process-resilient low-power MIMO front-ends.

9B.1 A Zonotoped Macromodeling for Reachability Verification of Eye-Diagram in High-Speed I/O Links with Jitter
Sai Manoj PD, Hao Yu - *Nanyang Technological Univ.*
Chenji Gu, Cheng Zhuo - *Intel Corp.*

9B.2 Random Walk Based Capacitance Extraction for 3D ICs with Cylindrical Inter-Tier-Vias
Wenjian Yu, Chao Zhang, Qing Wang - *Tsinghua Univ.*
Yiyu Shi - *Missouri Univ. of Science and Technology*

9B.3 Self-Learning MIMO-RF Receiver Systems: Process Resilient Real-Time Adaptation to Channel Conditions for Low Power Operation
Debashis Banerjee, Barry Muldrey - *Georgia Institute of Technology*
Shreyas Sen - *Intel Corp.*
Xian Wang, **Abhijit Chatterjee** - *Georgia Institute of Technology*

All speakers are denoted in bold | * - denotes best paper candidate

9C Software for Management of Parallelism and Data Integrity in Embedded Systems

Room: Winchester

Moderator:

Jose Ayala - *Complutense Univ. of Madrid*

This session tackles the problem of managing the parallel execution and the data integrity issues in embedded systems by means of novel software techniques. The first paper proposes a context-switch-enabled pipelining approach for the synthesis of data-parallel kernels. It formulates a scheduling problem for minimizing the context-switching cost of the multithreaded pipeline with an exact formulation and an efficient heuristic to solve the optimization problem. The second paper extends previously proposed analytical modeling techniques in the field of floating-point to fixed-point conversion to a larger class of programs. This approach extracts a compact, graph-based representation of the program. Finally, it is presented a warranty-aware page management design to mitigate the operation overhead required for managing the endurance issue in PCM-based embedded systems.

9C.1 Multithreaded Pipeline Synthesis for Data-Parallel Kernels

Mingxing Tan - *Cornell Univ.*
Bin Liu - *Micron Technology, Inc.*
Steve Dai, Zhiru Zhang - *Cornell Univ.*

9C.2 Toward Scalable Source Level Accuracy Analysis for Floating-Point to Fixed-Point Conversion

Gaël Deest - *Univ. of Rennes 1*
Tomofumi Yuki - *INRIA*
Olivier Sentieys - *INRIA, Univ. of Rennes 1*
Steven Derrien - *Univ. of Rennes 1*

9C.3 Warranty-Aware Page Management for PCM-Based Embedded Systems

Sheng-Wei Cheng - *National Taiwan Univ.*
Yu-Fen Chang - *National Tsing Hua Univ.*
Yuan-Hao Chang - *Academia Sinica*
Hsin-Wen Wei - *Tamkang Univ.*
Wei-Kuan Shih - *National Tsing Hua Univ.*

9D Clock Network Design and Timing

Room: Market 1 & 2

Moderators:

Rajendra Panda - *Oracle Corp.*
Tao Huang - *Synopsys, Inc., Inc.*

Improving the accuracy of Static Timing Analysis (STA) through EDA advancements in Common Path Pessimism Removal (CPPR), and improving the generation and distribution of clocks through resonant clocking, are presented in this session. Two types of resonant clocking, rotary and coupled LC, are featured in the first two papers. An EDA solution to integrating CPPR into the STA flow for improved accuracy is presented in the third paper.

9D.1 Frequency-Centric Resonant Rotary Clock Distribution Network Design

Ying Teng, **Baris Taskin** - *Drexel Univ.*

9D.2 Opportunistic Through-Silicon-Via Inductor Utilization in Resonant Clock: Concept and Algorithms

Umamaheswara Rao Tida - *Missouri Univ. of Science and Technology*
Varun Mittapalli - *Missouri Univ. of Science and Technology*
Cheng Zhuo - *Intel Corp.*
Yiyu Shi - *Missouri Univ. of Science and Technology*

9D.3 UI-Timer: An Ultra-Fast Clock Network Pessimism Removal Algorithm

Tsung-Wei Huang, Pei-Ci Wu, Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign*

Thursday, November 6

Workshop 2:

International Workshop on Design Automation for Analog and Mixed-Signal Circuits
8:00am - 5:00pm
Room: Almaden 1

Workshop 3:

A Roadmap for EDA Research in the Dark Silicon Era
8:00am - 6:00pm
Room: Almaden 2

Workshop 4:

7th IEEE/ACM Workshop on Variability Modeling and Characterization
8:50am - 5:00pm
Room: Winchester

Workshop 5:

International Workshop on Heterogeneous Computing Platforms (HCP)
8:15am - 5:45pm
Room: Market 1 & 2

Registration: 7:00am - 3:00pm - Almaden Foyer
Parking: $10 per day with in and out privileges

W2 Workshop 2: International Workshop on Design Automation for Analog and Mixed-Signal Circuits

Room: Almaden 1

Organizers:

Helmut Graeb - *Technical Univ. of Munich*
Xin Li - *Carnegie Mellon Univ.*
Chenjie Gu - *Intel Corp.*
Goeran Jerke - *Robert Bosch GmbH*
Mark Po-Hung Lin - *National Chung Cheng Univ.*

Growing digitization of integrated circuits has contributed to making system-on-chips ever more complex. Yet, it does not prevent that a substantial portion of a chip consists of analog and mixed-signal (AMS) circuits that provide critical functionality like signal conversion. Aggressive scaling of IC technologies, as well as advancing the integration of heterogeneous physical domains on chip, substantially complicates the design of AMS components.

On the one hand, their modeling and design becomes extremely complex. On the other hand, their interplay with the rest of the system-on-chip challenges design, verification and test. The new technology trends bring up enormous challenges and opportunities for AMS design automation. This is reflected by an increase in research activity on AMS CAD worldwide. The purpose of this workshop is to report recent advances on AMS CAD and motivate new research topics and directions in this area.

The workshop puts the focus on the following topics:

1. Design verification and test
The embedding of AMS components in system-on-chips challenges the verification of overall system performance with the clash of two completely different worlds. New methods for verification and test of AMS components shall be presented and discussed.

2. Statistical design
Ever increasing variability in manufacturing requires efficient methods for design and verification of high-sigma designs. Where are we and were should be go? The workshop will discuss recent trends from application point of view.

3. Constraints and layout design
AMS layout is one of the last frontiers where design automation has not yet found its way into industrial application: industrial analog layout is still mostly “polygon pushing”. But recently, strong research effort has been spent to improve analog layout automation. We will review and discuss new layout approaches.

4. Analog benchmarks reloaded
At ISCAS`84, several researchers made an attempt to provide benchmarks for analog design. 30 years after, analog design automation still lacks reproducibility of algorithmic results by the community. We want to discuss pro and con of analog benchmarks and consider a potential initiative to create a benchmark suite for analog design problems.

Speakers:

Abhijit Chatterjee - *Georgia Institute of Technology*
Bryan Casper - *Intel Corp.*
Michael Pronath - *MunEDA GmbH*
Karthik Aadithya - *Univ. of California, Berkeley*
Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign*
Choa Yan - *Synopsys, Inc.*
Wulong Liu - *Tsinghua Univ.*
Zheng Zhang - *Massachusetts Institute of Technology*
Shigetoshi Nakatake - *Univ. of Kitakyushu*
Federico Mantovani - *Infineon Technologies AG*
Chenjie Gu - *Intel Corp.*
Felix Salfelder - *Univ. of Frankfurt*
Beiye Liu - *Univ. of Pittsburgh*

Poster Presenters:

Xiaoming Chen - *Tsinghau Univ.*
Xueqian Zhao - *Michigan Technological Univ.*
Ya Wang - *Texas A&M Univ.*
Ni Leibin - *NanyangTechnological Univ.*
Manzil Zaheer - *Carnegie Mellon Univ.*
Shupeng Sun - *Carnegie Mellon Univ.*
Fanshu Jiao - *State Univ of New York*
Po-Cheng Pan - *National Chiao Tung Univ.*
Shobha Vasudevan - *Univ. of Illinois Urbana-Champaign*
Beiye Liu - *Univ. of Pittsburgh*

Workshop 2 Schedule - Thursday, November 6, 2014

8:00 - Opening Remarks

- SESSION 1: DESIGN VERIFICATION AND TEST -

8:05 - Abhijit Chatterjee *(Georgia Institute of Technology)*
Invited Talk: Towards Self-Learning AMS/RF Circuits and Systems: Adapting to Increasing Uncertainties in Real-Time Operating Conditions

8:50 - Poster Presentations

Xiaoming Chen, Yu Wang, Huazhong Yang,
(Tsinghua University, Beijing)
NICSLU: An Adaptive Sparse Solver for Circuit Simulation

Xueqian Zhao, Lengfei Han, Zhuo Feng
(Michigan Technological University)
A Performance-Guided Graph Sparsification Approach to Scalable and Robust SPICE-Accurate Integrated Circuit Simulations

Ya Wang, Peng Li, Suming Lai *(Texas A&M University)*
A Unifying and Robust Method for Efficient Envelope-Following Simulation of PWM/PFM DC-DC Converters

Ni Leibin, Sai Manoj P D, Yang Song, Hao Yu
(Nanyang Technological University, Singapore)
A Zonotoped Reachability Verification for High-speed I/O Links

Seyed-Nematollah Ahmadyan, Shobha Vasudevan
(Univ. of Illinois Urbana-Champaign)
A New Optimization Algorithm for Compressing Post-Si Analog Functional Tests for Time-efficient and Cost-effective Testing

Manzil Zaheer, Xin Li *(Carnegie Mellon Univ.)*, Chenjie Gu, *(Intel Corp.)*
MPME-DP: Multi-Population Moment Estimation via Dirichlet Process for Efficient Validation of Analog/Mixed-Signal Circuits

Shupeng Sun, Xin Li *(Carnegie Mellon Univ.)*
Fast Statistical Analysis of Rare Circuit Failure Events via Subset Simulation in High-Dimensional Variation Space

Beiye Liu, Hai Li, Yiran Chen *(Univ. Pittsburgh)*, Xin Li *(Carnegie Mellon Univ.)*, Tingwen Huang *(Texas A&M Univ. Doha)*, Qing Wu, Mark Barnell, *(Air Force Research Lab Rome)*
Reduction and IR-drop Compensations Techniques for Reliable Neuromorphic Computing Systems

Fanshu Jiao, Sergio Montano, Christian Ferent, Alex Doboli
(State University of New York), Simona Doboli, *(Hofstra University)*
Analog Circuit Design Knowledge Mining: Discovering Topological Similarities and Uncovering Design Reasoning Strategies

Po-Cheng Pan, Hung Ming Chen *(National Chiao Tung Univ., Hsinchu)*
A Study on the Possibility of Flexible Analog Layout Migration

9:30 - Posters + Coffee

- SESSION 1 (continued) -

10:00 - Aadithya V Karthik *(Univ. of California, Berkeley)*
Invited Talk: ABCD and BEE: Tools for Analog/Mixed-Signal Verification via Boolean Modelling

10:45 - Chao Yan *(Synopsys)*, Jije Wie *(Google)*, Mark Greenstreet *(Univ. British Columbia)*
AMS Verification using COHO-REACH

Workshop 2 Schedule - Thursday, November 6, 2014

11:00 - Wulong Liu, Yu Wang, Huazhong Yang *(Tsinghua University, Beijing),* **Guoqing Chen** *(AMD Research, Beijing),* Design Methodologies and Verification of 3D Mixed-signal ICs

- SESSION 2: STATISTICAL AND CIRCUIT DESIGN -

11:15 - Bryan Casper *(Intel Corp.)* Invited Talk: Synthesis-friendly High-speed I/O Architectures

12:00 - Zheng Zhang, Luca Daniel *(Massachusetts Institute of Technology)* High-Dimensional Hierarchical Uncertainty Quantification for MEMS/IC Co-Design

12:15 - Poster + Lunch

13:15 - Michael Pronath *(MunEDA Gmbh)* Invited Talk: Analyzing the Effects of Process Variation and Mismatch on Circuit Design: Monte Carlo and Alternatives

- SESSION 3: CONSTRAINTS AND LAYOUT DESIGN -

14:00 - Martin D. F. Wong *(Univ. Illinois at Urbana-Champaign)* Invited Talk: Data structures for analog placement

14:45 - Shigetoshi Nakatake *(Univ. Kitakyushu, Japan)* Analog Structure Tree for Floorplanning

15:00 - Federico Mantovani, Andreas Mueller *(Infineon Technologies GA, Munich-Neubiberg)* Design automation of layout modules for industrial analog mixed-signal applications

15:15 - Posters + Coffee

- SESSION 4 - ANALOG BENCHMARKS RELOADED -

15:45 - Shuqi Zhang, Ngai Wong *(Univ. of Hong Kong),* **Chenjie Gu** *(Intel Corp.)* Benchmarks for Analog/Mixed-Signal Macromodeling Research

16:00 - Lars Hedrich, Felix Salfelder *(Goethe Univ. Frankfurt/Main)* Evaluation of a Benchmark Suite for Formal Verification of Analog Circuits

- Plenary Discussion -

16:15 - Analog CAD – Quo Vadis?

16:55 - Closing remarks

W3 Workshop 3: A Roadmap for EDA Research in the Dark Silicon Era

Room: Almaden 2

Organizers:

Muhammad Shafique - *Karlsruhe Institute of Technology*
Siddharth Garg - *New York Univ.*

Supply voltage scaling has slowed down in the leakage dominated nanometer era because a lower supply voltage necessitates a lower threshold voltage (for iso-performance), which in turn exponentially increases leakage power consumption. As a result, although we can integrate more transistors per unit area with technology scaling, the switching power per transistor does not scale commensurately. Coupled with the physical limits imposed by device packaging and cooling technology on the peak power and peak power density, this results in the so-called dark silicon problem, i.e., not all parts of the chip can be simultaneously powered on at nominal voltage. It is projected that at the 8 nm technology node, 50%-80% of the chip area will be dark. The dark silicon challenge is essentially one of determining how best to utilize the abundance of (potentially dark) transistors, both in terms of design time provisioning and run-time management, so as to improve quality metrics (performance, reliability, lifetime, etc.) within peak power and thermal constraints. The EDA community has potentially much to contribute here because dark silicon also opens up a vast design space of potential solutions: navigating this design space in a computationally efficient way to narrow down on the most promising solutions is, fundamentally, an EDA challenge.

This workshop is intended to provide a common platform for EDA experts to discuss their vision and perspectives on the dark silicon problem, and to define a research roadmap for the next decade. This workshop will bring together researchers and experts from industry and academia to dwell on whether fundamentally new solutions are required in the context of dark silicon, or conversely, whether existing solutions can be retro-fitted to address these problems. In either scenario, a lively, but informative technical debate is envisioned that will help to carve out a distinct niche for dark silicon research. In keeping with its intent to encourage a diversity of opinions, this workshop will attempt to include speakers in the agenda with alternate perspectives ("dark silicon is just old wine in a new bottle!").

Speakers:

Mark Horowitz - *Stanford Univ.*
Michael Schulte - *Advanced Micro Devices, Inc.*
Michael Kishinevsky - *Intel Corp.*
Douglas Carmean - *Microsoft Research*
Giovanni De Micheli - *Ecole Polytechnique Fédérale de Lausanne*
Jason Cong - *Univ. of California, Los Angeles*
David Brooks - *Harvard Univ.*
Sri Parameswaran - *Univ. of New South Wales*
Tulika Mitra - *National Univ. of Singapore*
Sanghamitra Roy - *Utah State Univ.*
Ulya Karpuzcu - *Univ. of Minnesota*
John Sampson - *Pennsylvania State Univ.*
Michael Niemier - *Univ. of Notre Dame*

Poster Presenters:

Nasim Farahini - *Royal Institute of Technology*
Ing-Chao Lin - *National Cheng Kung Univ.*
Sergio Bampi - *Federal Univ. of Rio Grande do Sul*
Yatish Turakhia - *Stanford Univ.*

Workshop 3 Schedule - Thursday, November 6, 2014

8:15 – 8:30am - Introduction to the Workshop

Organizers: **Muhammad Shafique** *(Karlsruhe Institute of Technology)*, **Siddharth Garg** *(New York Univ)*

8:30 – 9:30 - Keynote

Mark Horowitz *(Stanford Univ.)*
Title: Computing's Energy Problem
(and what we can do about it)

9:30 – 09:45 - Coffee Break + Poster Session

9:45 – 11:10 - Session I: Run-Time

Dr. Michael Kishinevsky *(Intel Corp., USA)*
Life with "dark" silicon. Power and thermal problems in future platforms

Tulika Mitra *(National Univ. of Singapore, Singapore)*
Coordinated Power Management for Heterogeneous Multi-core Architectures

Sanghamitra Roy *(Utah State Univ., USA)*
Long term sustainability of Multicore Systems in the Dark Silicon Era

15 minutes mini-Panel

11:15 – 12:00 - Industrial Keynote

Michael Schulte *(Advanced Micro Devices, Inc., USA)*

12:00 – 13:00 - Lunch

13:00 – 15:20 - Session II: On-Chip Diversity to Rescue

Jason Cong *(Univ. of California, Los Angeles, USA)*
EDA Challenges for Designing Accelerator-Rich Architectures
David Brooks *(Harvard Univ., USA)*
Sri Parameswaran *(Univ. of New South Wales, Australia)*
The Greening of Dark Silicon: A NoC Perspective
John (Jack) Sampson *(Pennsylvania State Univ., USA)*
Scaling Diversity Alongside Dark Silicon with Coprocessor-Dominated Architectures

15 minutes mini-Panel

15:20 – 15:45 Coffee Break + Poster Session

15:45 – 17:30 Session III: Pushing the Envelope

Douglas Carmean *(Microsoft Research, USA)*
Title: The Promise of New Technologies to Light the Dark Alleys of Modern Silicon
Giovanni De Micheli
(Ecole Polytechnique Fédérale de Lausanne, Switzerland)
The role of emerging technologies to avoid a dark silicon era
Michael Niemier *(Univ. of Notre Dame, USA)*
Title: The Impact of Technology on Homogeneous and Heterogenous Core Scaling
Ulya Karpuzcu *(Univ. of Minnesota, USA)*
Rethinking Computer Architecture in the Dark Silicon Era

15 minutes mini-Panel

17:30 – 18:00 - Panel

A Dark Silicon Roadmap for the EDA Community

W4 Workshop 4: 7th IEEE/ACM Workshop on Variability Modeling and Characterization

Room: Winchester

Variability has emerged as a fundamental challenge to IC design in scaled CMOS technology; and it has profound impact on nearly all aspects of circuit performance. While some of the negative effects of variability can be handled with improvements in the manufacturing process, comprehensive methods are necessary to assess and manage the negative effects of variability, which in turn requires accurate and tractable variability models. The goal of the VMC workshop is to provide a forum for theoreticians and practitioners to freely exchange opinions on current practices as well as future research needs in variability modeling and characterization.

This is the 7th year of the workshop. This year, we focus on three topics:

1). Emerging technologies

2). Approximate computing

3). Modeling & characterization

Please visit the website of the workshop for up to date information: http://www.cerc.utexas.edu/utda/vmc/

Organizer:

Hidetoshi Onodera - *Kyoto Univ.*
David Z. Pan - *Univ. of Texas at Austin*
Rasit O. Topaloglu - *IBM Systems and Technology Group*

Speakers:

Krishnendu Chakrabarty - *Duke Univ.*
Toshiro Hiramoto - *Univ. of Tokyo*
Subhasish Mitra - *Stanford Univ.*
Kaushik Roy - *Purdue Univ.*
Anand Raghunathan - *Purdue Univ.*
Chris Kim - *Univ. of Minnesota*
Rakesh Kumar - *Univ. of Illinois at Urbana-Champaign*
Rasit O. Topaloglu - *IBM Systems and Technology Group*
A.K.M. Muhfuzul Islam - *Kyoto Univ.*

Poster Presenters:

Kevin Cameron - *Cameron EDA*
Renyuan Zhang - *Japan Advanced Institute of Science and Technology*
Li Yu - *Massachusetts Institute of Technology*
Takeshi Okagaki - *Renesas Electronics Corp.*
Masaki Shimada - *Renesas Electronics Corp.*
Kan Takeuchi - *Renesas Electronics Corp.*
Daijiro Murooka - *Univ. of Kitakyushu*
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Sergio Bampi - *Federal Univ. of Rio Grande do Sul*
Jun Shiomi - *Kyoto Univ.*
Ryo Kishida - *Kyoto Institute of Technology*
Aikaterini Papadopoulou - *Univ. of California, Berkeley*

W5 Workshop 5: International Workshop on Heterogeneous Computing Platforms (HCP)

Room: Market 1 & 2

Organizers:

Gi-Joon Nam - *IBM Research*
Mustafa Ozdal - *Intel Corp.*

After the end of Dennard scaling, power has become the limiting factor for modern designs. In the last decade, the computing industry relied on multiprocessors to achieve higher performance while satisfying system power constraints. Due to difficulties in task-level parallelism, however, the expected performance gain with increasing core counts is limited. As an alternative, heterogeneous compute resources can be utilized to achieve higher performance and better energy efficiency. Heterogeneous computing is becoming the norm for different platforms, including servers and mobile devices. General purpose CPUs can be paired up with additional processing units such as vector units (SSE/AVX), GPUs, FPGAs, and custom accelerators. The rapid growth in this field however, poses a broad range of new challenges in multiple areas such as programming, synthesis and implementation of applications. Solving these open problems requires interdisciplinary collaboration involving various research communities. This workshop will provide an open forum for discussions and exchange of ideas on these topics.

Speakers:

Deshanand Singh - *Altera Corp.*
Peter Hofstee - *IBM Research*
James Reinders - *Intel Corp.*
Christoph Hagleitner - *IBM Research*
Krste Asanovic - *Univ. of California, Berkeley*
Jason Cong - *Univ. of California, Los Angeles*
Michaela Blott - *Xilinx, Inc.*
Onur Mutlu - *Carnegie Mellon Univ.*
Deming Chen - *Univ. of Illinois*
Daniel Beece - *IBM Research*
Mishali Naik - *Intel Corp.*
Ganapati Srinivasa - *Intel Corp.*

Poster Presenters:

Ahmad Lashgar - *University of Victoria*
Amirali Baniasadi - *University of Victoria*
Zhiru Zhang - *Cornell University*
Alastair McKinley - *Analytics Engines*
Scott Fischaber - *Analytics Engines*
Roger Woods - *Analytics Engines*
Ben Greene - *Analytics Engines*
Ing-Chao Lin - *National Cheng Kung University*
Christian Brugger - *University of Kaiserslautern*
Christian de Schryver - *University of Kaiserslautern*
Norbert Wehn - *University of Kaiserslautern*

Workshop 5 Schedule - Thursday, November 6, 2014

8:15 – 8:30 - Opening Remarks

Organizers: Gi-Joon Nam *(IBM)* and
Mustafa Ozdal *(Intel Corp.)*

8:30 – 10:30 - Session 1: Emerging Heterogeneous Architectures

"ASPIRE: Specializing the Software and Hardware Stacks"
Krste Asanovic, *Univ. of California, Berkeley*

"Acceleration-Rich Architectures – from Single-chip to Datacenters"
Jason Cong, *Univ. of California Los Angeles*

"Architecting and Exploiting Asymmetry in Multi-Core Architectures"
Onur Mutlu, *Carnegie Mellon Univ.*

10:30 – 11:00 - Coffee Break

11:00 – 12:00 - Session 2: High-Level Synthesis and Applications on Heterogeneous Platforms

"FCUDA: the CUDA to FPGA Compiler"
Deming Chen, *Univ. of Illinois at Urbana-Champaign*

"Towards Efficient Next-Generation Genome Sequencing"
Mishali Naik and Ganapati Srinivasa, *Intel*

12:00 – 13:00 - Lunch

13:00 – 15:00 - Session 3: Latest Heterogeneous Plaforms and Programming Models

"Bringing Shared-Memory Reconfigurable Logic to the Datacenter and the Cloud"
Peter Hofstee, *IBM Austin Research Lab*

"Programming matters: Why Intel's Many-core approach is so important"
James Reinders, *Intel Corp.*

"OpenCL on FPGAs: Custom Data Paths for Energy Efficient Computation"
Deshanand Singh, *Altera Corp.*

15:00 – 15:30 - Coffee Break

15:30 – 17:00 Session 4: Applications on Heterogeneous Platforms II

"Key-Value Store Acceleration with OpenPower"
Michaela Blott, *Xilinx, Inc.*

"Text-Analytics Acceleration on Power8 with CAPI"
Christoph Hagleitner, *IBM Research Lab Zurich*

"FPGA-Based Monte Carlo Simulation Acceleration on Power8"
Daniel Beece, *IBM T.J. Watson Research Center*

17:00 – 17:45 - Poster Session and Networking

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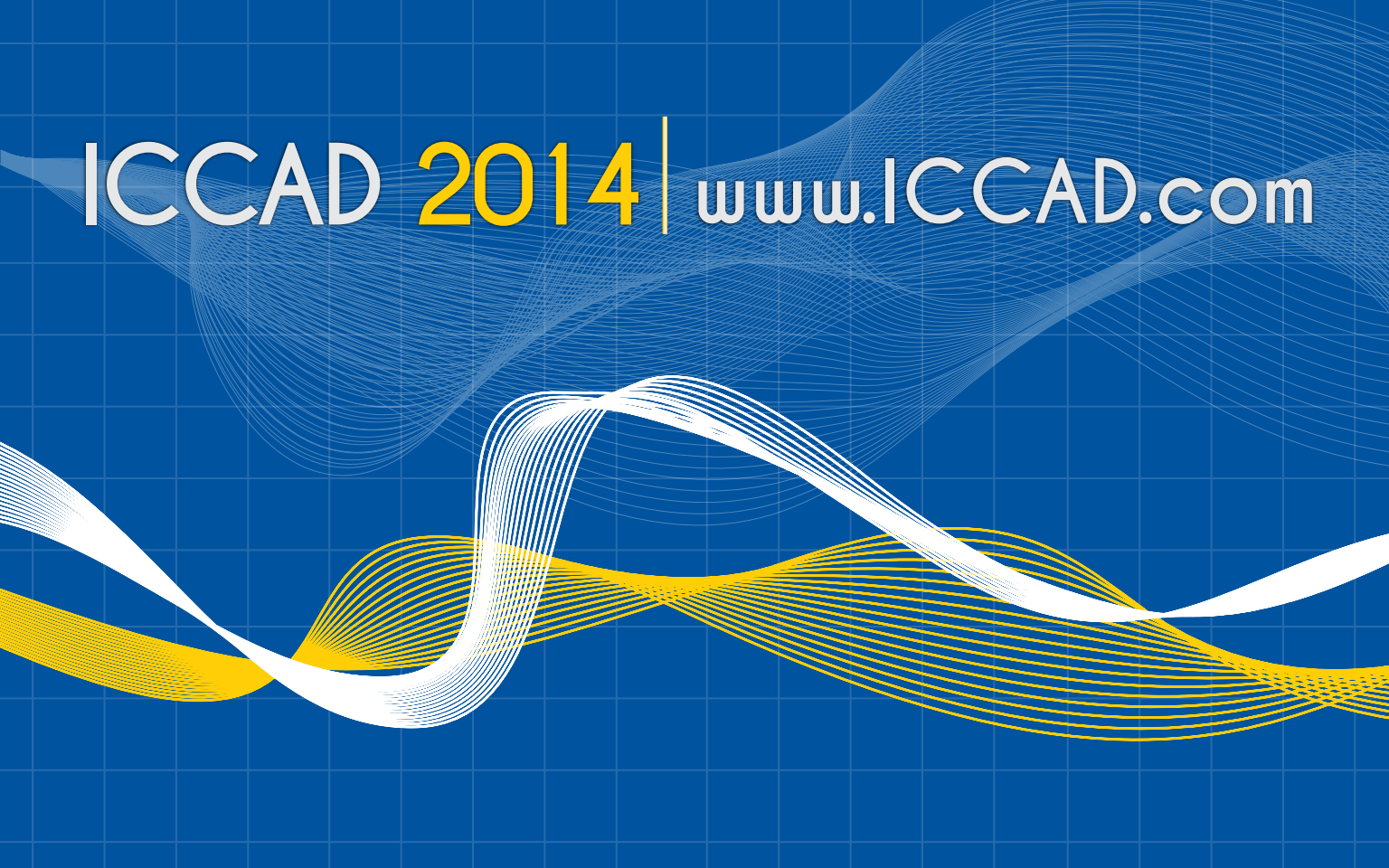
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