IEEE/ACM ICCAD

2013 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

32nd Edition

THE PREMIER CONFERENCE FOR ELECTRONIC DESIGN TECHNOLOGY

CONFERENCE PROGRAM

November 18-21, 2013

Hilton San Jose, San Jose, California

Sponsored by: IEEE, CEDA, ACM Association for Computing Machinery, SIGDA

In cooperation with: IEEE, IEEE Electron Devices Society, SSCS

www.ICCAD.com

The Premier Conference Devoted to Technical Innovations in Electronic Design Automation

Jörg Henkel
General Chair
Karlsruhe Institute of Technology (KIT)

Welcome to the 32nd Edition of ICCAD!!

ICCAD continues to be the premier conference on technical innovation on design automation with a focus on in-depth technical presentations. A key to the quality of the selected research work is a thorough double-blind review process that imposes a strict conflict-of-interest policy. As in the year before, the final selection was carried out in form of a 1-day physical TPC meeting that was held this year in June in Austin. A total of 354 papers went into the review process out of which 92 were finally accepted. This represents an acceptance ratio of 26% and an increase in submissions by around 5% compared to last year. Especially the front-end/system-level design as well as the nano/bio/new directions paper submissions represent a source of steady growth.

ICCAD has three William J. McCalla Paper Awards: A front-end best paper award, a back-end best paper award and a ten-year retrospective most influential paper award. Each award is selected throughout several steps by a separate committee of highly recognized international experts. For example, the front-end and back-end best paper selection starts with proposals from the track chairs of the technical tracks. All these papers are then passed to the respective best paper committee that thoroughly reads and discusses these papers and finally selects a small number out of them as official best paper candidates (marked in the program) out of which one is finally selected as the best paper award in that category.

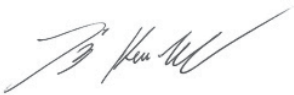
Besides the regular technical presentations, the technical program consists of special session and embedded tutorial presentations that focus on the newest trends and hottest topics in the field. A separate committee of experts has selected the proposed sessions out of a growing number of submissions in this track. ICCAD is complemented by three Thursday workshops.

Last but not least, ICCAD is proud to have three keynote presentations: The Monday Keynote is presented by Thomas Sterling from Indiana University on “The Future of Computing through Brain-Inspired Architectures.” The Tuesday Luncheon Keynote is by Lars Liebmann from IBM on “The Escalating Design Impact of Resolution-Challenged Lithography” whereas the Wednesday keynote is presented by Louis Scheffer from the Howard Hughes Medical Institute on “Networks of NMOS and Neurons.” They represent a mix of core ICCAD expertise and prospective future directions ICCAD may focus on.

Finally, I want to thank all ICCAD presenters/session organizers/session chairs, the ICCAD TPC, the ICCAD best paper/tutorial/special session selection committees, the ICCAD Executive Committee, the Program Chair, Vice Program Chair, Special Sessions/Tutorial Chair, Workshop Chair, MP Associates, the sponsors and all other who contributed, to make this edition of ICCAD another successful event.

I hope that you enjoy the diverse program of this year’s ICCAD!

Here’s looking to a great ICCAD in 2013, and the next 30 years of progress and success in our field!



Jörg Henkel, *ICCAD 2013 General Chair*

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IEEE/ACM ICCAD 2013 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

Speakers / Presenters

SPEAKERS' BREAKFAST

Room: **Santa Clara 1 & 2**
Please attend the day of your presentation!

Monday, November 18	7:30 - 8:30am
Tuesday, November 19	7:30 - 8:30am
Wednesday, November 20	7:30 - 8:30am

Need Practice?

A/V Practice Rooms are available to all speakers and presenters

Rooms: **Pacific, University & Executive Rooms**

Monday, November 18	7:00am - 6:00pm
Tuesday, November 19	7:00am - 6:00pm
Wednesday, November 20	7:00am - 4:00pm

General Information

CONFERENCE REGISTRATION HOURS

Room: **Almaden Foyer**

Monday, November 18	7:00am – 6:00pm
Tuesday, November 19	7:00am – 6:00pm
Wednesday, November 20	7:00am – 6:00pm
Thursday, November 21	7:00am – 4:00pm

Parking

$10 per day with in and out privileges

Conference Management: MP Associates, Inc.

MP associates, inc.

Our mission is to facilitate networking, education and marketing with efficiency and precision in order to maximize customer experiences, and client profitability and recognition. We accomplish this by having a committed staff of trade show production organizers with the training, technology tools, processes and experience to offer the best service in the industry. www.mpassociates.com

Best Paper Candidates/Award Committees

IEEE/ACM William J. McCalla Best Paper Candidates:

Monday

2B.1 Improved SAT-based ATPG: More Constraints, Better Compaction
Stephan Eggersglüß, Robert Wille, **Rolf Drechsler** - *Univ. of Bremen*

3B.2 Layout Decomposition with Pairwise Coloring for Multiple Patterning Lithography
Ye Zhang, Wai-Shing Luk, Changhao Yan, Xuan Zeng - *Fudan Univ.*
Hai Zhou - *Northwestern Univ.*

3B.4 Block Copolymer Directed Self-Assembly (DSA) Aware Contact Layer Optimization for 10 nm 1D Standard Cell Library
Yuelin Du, Daifeng Guo, Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign*
He Yi, H.-S. Philip Wong - *Stanford Univ.*
Hongbo Zhang, Qiang Ma - *Synopsys, Inc.*

Tuesday

5B.2 Methodology for Standard Cell Compliance and Detailed Placement for Triple Patterning Lithography
Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, David Z. Pan - *Univ. of Texas at Austin*

6A.4 Unleashing the Potential of MLC STT-RAM Caches
Xiuyuan Bi, Mengjie Mao, Hai Li - *Univ. of Pittsburgh*
Danghui Wang - *Northwestern Polytechnical Univ.*

7B.1 Redundancy-Aware Electromigration Checking for Mesh Power Grids
Sandeep Chatterjee, Mohammad Fawaz, Farid N. Najm - *Univ. of Toronto*

Wednesday

9A.2 A Polynomial Time Algorithm for Solving the Word-length Optimization Problem
Karthick Nagaraj Parashar, Olivier Sentieys - *INRIA Rennes - Bretagne Atlantique*
Daniel Menard - *Institut National des Sciences*

IEEE/ACM William J. McCalla ICCAD Best Paper Award Selection Committee:

Luca Benini, *Eidgenössische Technische Hochschule Zürich*

Nikil Dutt, *Univ. of California, Irvine*

Alan Hu, *Univ. of British Columbia*

Jiang Hu, *Texas A&M Univ.*

Andrew Kahng, *Univ. of California, San Diego*

Sani Nassif, *IBM Corp.*

Ten-Year Retrospective Most Influential Paper Award Selection Committee:

Helmut Graeb, *Technical Univ. of Munich*

Niraj Jha, *Princeton Univ.*

Hidetoshi Onodera, *Kyoto Univ.*

Sri Parameswaran, *Univ. of New South Wales*

CADathlon at ICCAD

Sunday, November 17, 8:00am - 5:00pm
Almaden 1 & 2

In the spirit of the long-running ACM programming contest, the CADathlon challenges students in their CAD knowledge, and their problem solving, programming, and teamwork skills. It serves as an innovative initiative to assist in the development of top students in the EDA field. The contest will provide a platform for SIGDA, academia, and industry to focus attention on the best and brightest of next generation CAD professionals.

The students will be given a number of problems that range in difficulty and topics. Information about the CAD areas, relevant papers, and potentially a software framework that will run on Linux will be released one week before the competition. Students will be allowed to work in teams of two. At the contest, students will be given the problem statements and an example test data, but they will not have the judges' test data. Solutions will be judged on correctness and efficiency. The team that passes the most testcases is declared the winner. A handsome prize awaits the winning team. The judges are experts in EDA from both academia and industry.

During the competition students will be presented with six problems in the following areas:

- Circuit Design & Analysis
- Physical Design
- Logic & High-Level Synthesis
- System Design & Analysis
- Functional Verification
- Bio-EDA

The competition is open to all graduate students specializing in CAD currently enrolled full-time in a Ph.D. granting institution in any country. Partial or full travel grants will be provided for qualifying students.

For more information, please contact Jarrod Roy at jarrod.a.roy@gmail.com

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sigda special interest group on design automation

Monday, November 18

8:30 - 9:00AM - Almaden 1&2
Opening Session & Awards: Jörg Henkel - General Chair, *Karlsruhe Institute of Technology (KIT)*

9:00 - 10:00AM - Keynote Address: The Future of Computing through Brain-Inspired Architectures
Thomas Sterling, *Center for Research in Extreme Scale Technologies*

TIME	ALMADEN 1	ALMADEN 2	WINCHESTER	MARKET 1 & 2
10:30am - 12:00pm	Session 1A: Emerging Memory Technologies	Session 1B: Novel Techniques for Manfacturability and Layout Migration	Session 1C: Making Timing Variations Irrelevant	Designer Track 1D: Advances in Modeling and Optimization: From System Level to Mixed Signal Designs
12:00 - 1:45pm	**Lunch:** Hyatt Hotel - Grand Hall			
2:00 - 4:00pm	Embedded Tutorial 2A: Performance Evaluation of Multicore Systems: From Traffic Analysis to Latency Predictions	Session 2B: Improving Test Quality, Manufacturability & Reliability	Session 2C: CAD Approaches for Emerging Applications	Special Session 2D: From Application to Emerging Devices: Analog is Between a Rock and a Hard Place
4:30 - 6:30pm	Special Session 3A: Keeping Kilo-Core Chips Cool: New Directions and Emerging Solutions	Session 3B: Triple Patterning, Triple the Trouble?	Special Session 3C: Emerging Design Automation: The Movement to Apply CAD Techniques to Global Challenges	Session 3D: Emerging Directions in Hardware Synthesis

Additional Meeting: ACM Student Research Competition Poster Session: 1:00 - 3:00pm - Santa Clara 1 & 2

Networking Reception: 6:30 - 7:00pm: Almaden Foyer

Registration: 7:00am - 6:00pm - Almaden Foyer
Parking: $10 per day with in and out privileges
Speakers Breakfast: 7:30 - 8:30am - Santa Clara 1 & 2
AV Practice Rooms: 7:00am - 6:00pm - Pacific, Executive Boardroom, and University

Opening Session & Award Presentations

Room: Almaden 1 & 2

Opening Remarks -

Jörg Henkel - General Chair - *Karlsruhe Institute of Technology (KIT)*

Award Presentations

IEEE/ACM William J. McCalla ICCAD Best Paper Award

This award is given in memory of William J. McCalla for his contribution to ICCAD and his CAD technical work throughout his career.

Front End

2B.1 Improved SAT-based ATPG: More Constraints, Better Compaction
Stephan Eggersglüß, Robert Wille, Rolf Drechsler - *Univ. of Bremen / DFKI*

Back End

5B.2 Methodology for Standard Cell Compliance and Detailed Placement for Triple Patterning Lithography
Bei Yu, Xiaoqing Xu, Jhih-Rong Gao and David Z. Pan - *Univ. of Texas at Austin*

ICCAD Ten Year Retrospective Most Influential Paper Award

This award is being given to the paper judged to be the most influential on research and industrial practice in computer-aided design of integrated circuits over the ten years since its original appearance at ICCAD.

2003 Paper Titled: Statistical Timing Analysis Considering Spatial Correlations Using A Single PERT-Like Traversal
Authors: Hongliang Chang, Sachin S. Sapatnekar - *Univ. of Minnesota*
Publication: ICCAD 2003 Proceedings: pp. 621-625

IEEE CEDA Early Career Award

David Atienza, *Assistant Professor of Electrical Engineering and Director of the Embedded Systems Laboratory at EPFL*

For sustained and outstanding contributions to design methods and tools for multi-processor systems-on-chip (MPSoC), particularly for work on thermal-aware design, low-power architectures and on-chip interconnects synthesis.

IEEE CEDA Early Career Award

Zhuo Li, *IBM T. J. Watson Research Center*

For essential and outstanding contributions to algorithms, methodologies, and software for interconnect optimization, physical synthesis, parasitic extraction, testing and simulation.

IEEE CEDA Outstanding Service Contribution

Alan Hu, *Univ. of British Columbia*

For significant service to the EDA community as the 2012 ICCAD General Chair

2013 SIGDA Pioneering Achievement Award

Donald E. Thomas, *Dept. of Electrical and Computer Engineering, Carnegie Mellon Univ.*

For his pioneering work in making the Verilog Hardware Description Language more accessible for the design automation community and allowing for faster and easier pathways to simulation, high-level synthesis, and co-design of hardware-software systems.

ACM/SIGDA CADathlon

Introduction of the 2013 winners.

Keynote:

The Future of Computing Through Brain-Inspired Architectures

Presenter: Thomas Sterling - *Center for Research in Extreme Scale Technologies*

Room: Almaden 1 & 2

The human brain is perhaps the most complicated creation of nature with 89 billion neurons and a quadrillion connections in a volume of less than 1500 cubic centimeters operating at a power consumption of a mere 20 watts. Each neuron carries out a complicated algorithm of summation of potentially thousands of inputs, comparison with a time varying threshold, and dissemination of a signal to hundreds or thousands of outputs, and this potentially every millisecond. While it is difficult to compare this performance with conventional supercomputers, it is clear that it would take a system larger than any existing to duplicate this specific functionality. Both the EU and the US have recently undertaken major projects in the study of the human brain. The notion of "brain-inspired" has many interpretations but for more than two decades researchers have explored the possibilities of using structures to achieve unprecedented performance, efficiencies, and solutions to problems previously interpreted as requiring "intelligence". This presentation will explore the background of brain inspired computing including classical neural networks and AI as well as the most recent major initiatives. It will then examine two levels of computer architecture that differ from conventional practices and embody important aspects of structure and operation implicit in brain function at high and low abstract levels. A conclusion is that the practical application of machine intelligence may be feasible but only if true knowledge understanding is achieved.

Thomas Sterling is Professor of Informatics and Computing at Indiana University. He serves as the Executive Associate Director of CREST and as its Chief Scientist. Since receiving his Ph.D from MIT as a Hertz Fellow in 1984, Dr. Sterling has conducted research in parallel computing systems in industry, academia, and government centers. He is most widely known for his pioneering work in commodity cluster computing as leader of the Beowulf Project for which he and colleagues were awarded the Gordon Bell Prize. Professor Sterling currently leads a team of researchers at IU to derive the advanced ParalleX execution model and develop a proof-of-concept reference implementation to enable a new generation of extreme scale computing systems and applications. He is the co-author of six books and holds six patents.

All speakers are denoted in bold | * - denotes best paper candidate

1A Emerging Memory Technologies
Room: Almaden 1

Moderators:

Shih-Lien Lu - *Intel Corp.*
Dmitri Stukov - *Univ. of California, Santa Barbara*

Emerging non-volatile memories are promising alternatives to Flash and DRAM which are facing scaling limitations at nanoscale. In this session there are three papers providing novel solutions to address some of the major challenges in the design of these emerging memory technologies. The first paper addresses asymmetric failure probabilities in STT-MRAMs. The second paper provides asymmetric differential cell architecture for reliability and performance in STT-MRAM. The last paper explores design tradeoffs for resistive random access memories.

1A.1 CD-ECC: Content-Dependent Error Correction Codes for Combating Asymmetric Nonvolatile Memory Operation Errors
Wujie Wen, Mengjie Mao, Yiran Chen - *Univ. of Pittsburgh*
Xiaochun Zhu, Seung Kang - *Qualcomm, Inc.*
Danghui Wang - *Northwestern Polytechnical Univ.*

1A.2 ADAMS: Asymmetric Differential STT-RAM Cell Structure For Reliable and High-performance Applications
Yaojun Zhang, Ismail Bayram, Hai Li, Yiran Chen - *Univ. of Pittsburgh*
Yu Wang - *Tsinghua Univ.*

1A.3 Design of Cross-Point Metal-Oxide ReRAM Emphasizing Reliability and Cost
Dimin Niu, Cong Xu, Yuan Xie - *Pennsylvania State Univ.*
Naveen Muralimanohar, Norman Jouppi - *Hewlett-Packard Labs.*

1B Novel Techniques for Manufacturability and Layout Migration
Room: Almaden 2

Moderators:

Rasit Topaloglu - *IBM Systems and Technology Group*
Charles Chiang - *Synopsys, Inc.*

This session consists of three papers on novel techniques for manufacturability and layout migration. The first paper presents efficient aerial image simulatoin on multi-core SIMD CPU. The second paper presents a polynomial-time SADP solution targeting minimization of overlay in standard cells. The final paper presents a minimally invasive technique for analog layout migration.

1B.1 Efficient Aerial Image Simulation on Multi-Core SIMD CPU
Pei-Ci Wu, Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign*
Tan Yan, Hongbo Zhang - *Synopsys, Inc.*

1B.2 Optimally Minimizing Overlay Violation in Self-aligned Double Patterning Decomposition for Row-based Standard Cell Layout in Polynomial Time
Zigang Xiao, Yuelin Du, Haitong Tian, Martin Wong - *Univ. of Illinois at Urbana-Champaign*

1B.3 Efficient Analog Layout Prototyping by Layout Reuse with Routing Preservation
Ching-Yu Chin, Po-Cheng Pan, Hung-Ming Chen, Jou-Chun Lin - *National Chiao Tung Univ.*
Tung-Chieh Chen - *Synopsys, Inc.*

1C Making Timing Variations Irrelevant

Room: Winchester

Moderator:

Suriyaprakash Natarajan - *Intel Corp.*
Hongliang Chang - *Cadence Design Systems, Inc.*

In this session, you will learn about several innovative techniques to deal with timing variations in digital circuits. The first paper proposes a reconfigurable adder that is flexible in dealing with applications with different accuracy requirements. This is followed by a paper that describes a concept for the design of speculative circuits, mixing time-borrowing with error detection/correction in order to dynamically improve performance and/or reduce energy consumption in logic circuits. The final paper optimizes circuits such that aging is more evenly distributed, resulting in increased circuit lifetime.

1C.1 On Reconfiguration-Oriented Approximate Adder Design and Its Application
Rong Ye, Ting Wang, Feng Yuan, Qiang Xu - *Chinese Univ. of Hong Kong*
Rakesh Kumar - *Univ. of Illinois at Urbana-Champaign*

1C.2 ForTER: A Forward Error Correction Scheme for Timing Error Resilience
Jie Zhang, Feng Yuan, Rong Ye, **Qiang Xu** - *Chinese Univ. of Hong Kong*

1C.3 Aging-Aware Logic Synthesis
Mojtaba Ebrahimi, Fabian Oboril, Saman Kiamehr, Mehdi B. Tahoori - *Karlsruhe Institute of Technology*

1D Designer Track: Advances in Modeling and Optimization: From System Level to Mixed Signal Designs

Room: Market 1 & 2

Moderator:

Siddharth Garg - *Univ. of Waterloo*

Organizer:

Diana Marculescu - *Carnegie Mellon Univ.*

Increased complexity of emerging designs require new tools and methodologies for coping with challenges introduced by the sheer number of devices and added functionality. This session covers advances methodologies and tools designers are employing for large scale designs ranging from system simulation and hardware acceleration, to custom hardware and mixed-signal designs.

1D.1 Modeling Hardware for Software Optimization and Verification - System Design from the Transaction Level Simulation to Hardware Acceleration
Frank Schirrmeister - *Cadence Design Systems, Inc.*

1D.2 Model-Based Hardware Design
Girish Venkataramani, Kiran Kintali, Sudeepa Prakash, Stephan van Beek - *MathWorks, Inc.*

1D.3 BAG: A Designer-Oriented Integrated Framework for the Development of AMS Circuit Generators
John Crossley, Alberto Puggelli, Hanh-Phuc Le, Bonjern Yang, Rachel Nancollas, Kwangmo Jung, Lingkai Kong, Nathan Narevsky, Yue Lu, Nicholas Sutardja, Eun Ji An, Alberto Sangiovanni-Vincentelli, Elad Alon - *Univ. of California, Berkeley*

AM

Additional Meeting: **ACM Student Research Competition Poster Session**

Room: Santa Clara 1 & 2

Organizers:

Srinivas Katkoori - *University of South Florida*
Miroslav Velev - *Aries Design Automation*

Sponsored by Microsoft Research, the ACM Student Research Competition (SRC) is an internationally recognized venue enabling undergraduate and graduate students who are ACM members to:

- Experience the research world—for many undergraduates this is a first!
- Share research results and exchange ideas with other students, judges, and conference attendees;
- Rub shoulders with academic and industry luminaries;
- Understand the practical applications of their research;
- Perfect their communication skills;
- Receive prizes and gain recognition from ACM and the greater computing community.

ACM SRC has three rounds: (1) abstract review; (2) poster session (this session); and (3) technical presentation.

In the first round, 2-page research abstracts are evaluated by EDA experts from academia and industry to select participants for the second round (this session). For the ACM SRC at ICCAD 2013 competition, 43 abstracts were received out of which 22 participants were invited to present their research at ICCAD. The posters are evaluated by EDA experts to select 5 participants in graduate and undergraduate categories to advance to the final round (technical presentation round). Students are expected to discuss their work with evaluators who visit their presentation areas. Each evaluator will rate the student's visual presentation based on the criteria of uniqueness of the approach, the significance of the contribution, visual presentation, and format of presentation.

More details can be found at: **www.sigda.org/src**

Sponsored By:

2A Embedded Tutorial: **Performance Evaluation of Multicore Systems: From Traffic Analysis to Latency Predictions**

Room: Almaden 1

Moderator:

Paul Bogdan - *Univ. of Southern California*

Organizer:

Zhiliang Qian - *Hong Kong Univ. of Science and Technology*

With technology scaling down, more and more components can be integrated on a single chip. As a result, the modern computing system has led to the advent of Multi-processor System-on-Chip (MPSoC) and Chip Multi-processor(CMP) design. Network-on-Chips (NoCs) have been proposed as a modular and scalable solution to handle the complex on-chip communications. What distinguishes NoC based multicore systems design from traditional embedded System-on-Chip (SoC) design is that, the complexity of such systems, as well as the tight requirements in terms of power, performance, cost and time-to-market place a tremendous pressure on the design exploration and optimization. The specifications of multicore system drive the choice of NoC design parameters, such as the routing algorithm, flow control scheme etc,. Therefore, it is of utmost importance to rely on accurate NoC traffic models and provide a robust performance evaluation with respect to numerous configurations to obtain an optimal design. The simulation based evaluation method besides being extremely slow, provides little insight on how the design parameters will affect the final performance so as to guide the optimization process in the synthesis loop. Consequently, fast and accurate performance evaluation methods for multicore systems are strongly desired. Furthermore, these methods should consider and tackle the non-stationary and fractal behavior which are usually involved in NoC-based systems. Such complex requirements call for a multi-disciplinary approach towards the NoC performance analysis.

In this tutorial, we argue that a precise performance analysis of NoC based multicore system should cover both the traffic analysis and the router latency behavior modeling. Therefore, we introduce the NoC performance evaluation from the following perspectives: we begin with the review of network workloads and the analysis methods to explore the traffic characteristics. We especially emphasize the analysis of NoC traffic non-stationary (i.e., time dependent statistics) and fractal (i.e., long-range-dependent (LRD)) characteristics and their implications on multi-core system design. Then, we elaborate on the analytical methods for latency and throughput modeling. We review how to utilize the queuing models for estimating the wormhole and virtual channel NoC delays. We will also discuss on the modifications needed to tackle the traffic burstiness (or non-independent arrival or service time distribution). Finally, we review a machine learning based approach to combine the advantages of analytical methods and simulations for a more accurate performance evaluation.

2A.1 Performance Evaluation of Multicore Systems: From Traffic Analysis to Latency Predictions

Zhiliang Qian, Chi-Ying Tsui - *Hong Kong Univ. of Science and Technology*

Paul Bogdan - *Univ. of Southern California*

All speakers are denoted in bold | * - denotes best paper candidate

2B Improving Test Quality, Manufacturability & Reliability

Room: Almaden 2

Moderators:

Mahmut Yilmaz - *Nvidia Corp.*
Hung-Ming Chen - *National Chiao Tung Univ.*

This session presents novel SAT-based techniques to generate compact tests and effective delay test patterns, innovative methods to glean DFM rules from failed silicon to improve yield, and efficient techniques for field error-rate estimation.

***2B.1 Improved SAT-based ATPG: More Constraints, Better Compaction**
Stephan Eggersglüß, Robert Wille, **Rolf Drechsler** - *Univ. of Bremen*

2B.2 Automatic Test Pattern Generation for Delay Defects Using Timed Characteristic Functions
Shin-Yann Ho, Shuo-Ren Lin, Ko-Lung Yuan, Chien-Yen Kuo, Kuan-Yu Liao, Jie-Hong Roland Jiang, Chien-Mo Li - *National Taiwan Univ.*

2B.3 DREAMS: DFM Rule EvAluation using Manufactured Silicon
Shawn Blanton, Fa Wang, Cheng Xue, Pranab Nag, Xue Yang, Xin Li - *Carnegie Mellon Univ.*

2B.4 Stochastic Error Rate Estimation for Adaptive Speed Control with Field Delay Testing
Shoichi Iizuka, Masafumi Mizuno, Dan Kuroda, Masanori Hashimoto, Takao Onoye - *Osaka Univ.*

2C CAD Approaches for Emerging Applications

Room: Winchester

Moderators:

Alex Jones - *Univ. of Pittsburgh*
Naehyuck Chang - *Seoul National Univ.*

This session introduces CAD techniques for emerging applications on automotive systems, data centers, machine learning, and optical networks-on-chip. The first paper presents an ILP-based approach to optimize the end-to-end latency while meeting the security requirements. The second paper introduces dynamic server power capping that enables consumer side load regulation of the power grid. The third paper introduces a carry-skip adder that tradeoffs power consumption and accuracy, which can significantly reduce the power consumption of machine learning applications. The final paper presents tools for physical design of optical NoC topologies.

2C.1 Security-Aware Mapping for CAN-Based Real-Time Distributed Automotive Systems
Chung-Wei Lin, Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley*
Qi Zhu, Calvin Phung - *Univ. of California, Riverside*

2C.2 Dynamic Server Power Capping for Enabling Data Center Participation in Power Markets
Hao Chen, Can Hankendi, Michael Caramanis, Ayse Coskun - *Boston Univ.*

2C.3 An Energy Efficient Approximate Adder with Carry Skip for Error Resilient Neuromorphic VLSI Systems
Yongtae Kim, Yong Zhang, Peng Li - *Texas A&M Univ.*

2C.4 PROTON: An Automatic Place-and-Route Tool for Optical Networks-on-Chip
Anja Boos, Ulf Schlichtmann - *Technical Univ. of Munich*
Luca Ramini, Davide Bertozzi - *Univ. di Ferrara*

MONDAY, NOVEMBER 18 - 2:00 - 4:00pm

2D Special Session: From Application to Emerging Devices: Analog is Between a Rock and a Hard Place

Room: Market 1 & 2

Moderator:
Janet Roveda - *Univ. of Arizona*

Organizer:
Janet Roveda - *Univ. of Arizona*

The real world is analog. Nearly 70% of today's integrated circuit designs are considered mixed signal according to Mentor Graphics' recent survey. It is obvious that the success or failure of analog mixed-signal designs determines the future of integrated circuits. In this presentation, we invite three speakers to provide the state of art analog design need from three different angles: Variation aware analog design, Integration solution for mixed signal design, Analog verification, and data driven mixed signal designs. In the first talk, Dr. Trent McConaghy of Solido Design Automation will discuss variation-aware design from 40nm to 14nm, not only for "pure" analog circuits but other custom circuits where analog behavior must be considered, including memories, standard cells, and custom digital circuits. In the second talk, Dr. Richard Shi will talk about analog verification. While digital verification has a number of options, for years, analog design verification relies on transistor-level SPICE circuit simulation. Dr. David White from Cadence will provide an integrated vision of mixed signal design. Accord to Cadence, today's analog functionality has to interface thousands or millions of gates including DSPs, memories, and processors. The analog portion of the designs, including antennas, sensors, cables, RF interfaces, etc., yet small but is critical in both function and performance to the overall design.

2D.1 Analog Behavior in Custom IC Variation-Aware Design
Trent McConaghy - *Solid State Technology*

2D.2 Mixed-Signal Verification by Signal Abstraction
Richard Shi - *Orora Design Technologies, Inc.*

2D.3 A New Methodology to Address the Growing Productivity Gap in Analog Design
David White - *Cadence Design Systems, Inc.*

All speakers are denoted in bold | * - denotes best paper candidate

MONDAY, NOVEMBER 18 - 4:30 - 6:30pm

3A Special Session: Keeping Kilo-Core Chips Cool: New Directions and Emerging Solutions

Room: Almaden 1

Moderator:
Muhammad Shafique - *Karlsruhe Institute of Technology*

Organizers:
Muhammad Shafique - *Karlsruhe Institute of Technology*
Siddharth Garg - *Univ. of Waterloo*

As Moore's law continues unabated, it is predicted that future generation multi-processor systems-on-chip (MPSoC) will feature hundreds, and potentially even thousands, cores. However, since the power and thermal budgets are not expected to keep pace with this abundance of transistors and cores, the need for effective, efficient and responsive power and thermal management algorithms is greater than ever before and will, arguably, require an entirely new set of foundational and theoretical tools. The goal of this special session is to introduce the audience to emerging, promising techniques, both theoretical and practical, that are likely to come to the forefront for the power and thermal management of massively parallel MPSoC platforms.

3A.1 Agent-Based Distributed Power Management for Kilo-Core Processors
Muhammad Shafique, Jörg Henkel - *Karlsruhe Institute of Technology*

3A.2 Managing Mobile Platform Power
Umit Ogras - *Arizona State Univ.*
Raid Ayoub, Michael Kishinevsky - *Intel Corp.*
David Kadjo - *Texas A&M Univ.*

3A.3 Control Theoretic Techniques for Multi-Core Power Management
Siddarth Garg - *Univ. of Waterloo*

All speakers are denoted in bold | * - denotes best paper candidate

3B Triple Patterning, Triple the Trouble?

Room: Almaden 2

Moderators:

J. Andres Torres - *Mentor Graphics Corp.*
Jamil Kawa - *Synopsys, Inc.*

This session presents the recent progress in algorithmic developments for enabling advanced patterning techniques. The first paper presents a high performance triple patterning decomposer with balanced density. The second paper focuses on a similar challenge and proposes a pair-wise coloring technique. The next paper tailors triple patterning decomposition of standard-cell-based designs using a SAT-based solution. The final paper discusses the contact-layer optimization for a lithographic process using directed self-assembly.

3B.1 A High-Performance Triple Patterning Layout Decomposer with Balanced Density

Bei Yu, David Pan - *Univ. of Texas at Austin*
Yen-Hung Lin - *National Chiao Tung Univ.*
Gerard Luk-Pat, Kevin Lucas - *Synopsys, Inc.*
Duo Ding - *Oracle Corp.*

***3B.2 Layout Decomposition with Pairwise Coloring for Multiple Patterning Lithography**

Ye Zhang, Wai-Shing Luk, Changhao Yan, Xuan Zeng - *Fudan Univ.*
Hai Zhou - *Northwestern Univ.*

3B.3 Constrained Pattern Assignment for Standard Cell Based Triple Patterning Lithography

Haitong Tian, Yeulin Du, Zigang Xiao, Martin Wong - *Univ. of Illinois at Urbana-Champaign*
Hongbo Zhang - *Synopsys, Inc.*

***3B.4 Block Copolymer Directed Self-Assembly (DSA) Aware Contact Layer Optimization for 10 nm 1D Standard Cell Library**

Yuelin Du, Daifeng Guo, Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign*
He Yi, H.-S. Philip Wong - *Stanford Univ.*
Hongbo Zhang, Qiang Ma - *Synopsys, Inc.*

3C Special Session: Emerging Design Automation: The Movement to Apply CAD Techniques to Global Challenges

Moderator: Room: Winchester

Yiran Chen - *Univ. of Pittsburgh*

Organizer:

Yiran Chen - *Univ. of Pittsburgh*

The Electronic Design Automation (EDA) industry is now facing severe challenges as the technology scaling pace of sem-iconductor fabrication dramatically slows. In addition to electronic/VLSI chip designs, many EDA researchers and professionals are relaxing the electronics application and exploring new opportunities for utilizing design automation methods. Many markets can leverage the knowledge accumulated in EDA industry for tens of years as well as their well-trained expertise in modeling and optimizing large scale problems. In this special session, four speakers will share their experiences on solving the problems that are not conventional EDA, but all require general CAD knowledge. These topics span energy storage, Surveillance, semiconductor sustainability and intelligent traffic controls. We hope the four talks will inspire the creativity of EDA professionals and researchers to consider new applications of their unique expertise while providing motivation of the EDA community for considering new markets as new growth potential for the industry.

3C.1 Computer-Aided Design of Electrical Energy Systems

Younghyun Kim, Sangyoung Park, **Naehyuck Chang** - *Seoul National Univ.*
Donghwa Shin, Massimo Petricca, Massimo Poncino - *Politecnico di Torino*

3C.2 A Neuromorphic Architecture for Anomaly Detection in Autonomous Large-Area Traffic Monitoring

Qiuwen Chen, **Qinru Qiu** - *Syracuse Univ.*
Hai Li - *Univ. of Pittsburgh*
Qing Wu - *Air Force Research Lab*

3C.3 Considering Fabrication in Sustainable Computing

Alex Jones, Yiran Chen, William Collinge, Haifeng Xu, Laura Schaefer, Melissa Bilec - *Univ. of Pittsburgh*
Amy Landis - *Arizona State Univ.*

3C.4 Transit Bus Scheduling with Limited Energy

Jing-Quan Li - *Univ. of California, Berkeley*

3D Emerging Directions in Hardware Synthesis

Room: Market 1 & 2

Moderators:

Stephen Neuendorffer - *Xilinx, Inc.*
Jay Bhadra - *Freescale Semiconductor, Inc.*

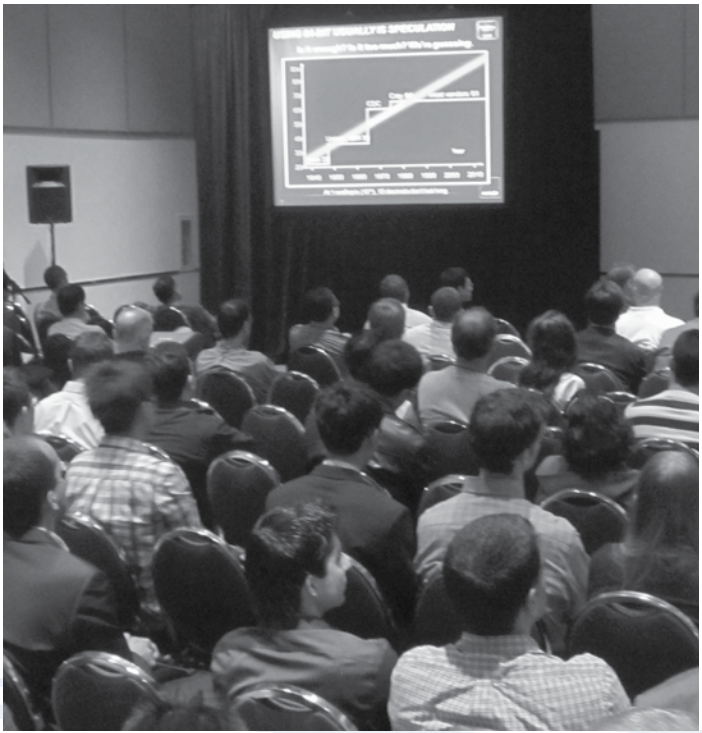
This session presents novel ideas on high-level synthesis (HLS), asynchronous and threshold-logic synthesis, and FPGA acceleration. The first paper incorporates loop pipelining into the system of difference constraints (SDC) approach for scheduling in HLS. The second paper deals with the synthesis of asynchronous circuits, offering an approach for optimized slack matching in circuits with conditional execution. The third paper proposes a path sensitization criteria to analyze the timing of threshold-logic circuits. The last paper proposes a hardware architecture to accelerate BCP (Boolean Constraint Propagation) for speeding up SAT solvers.

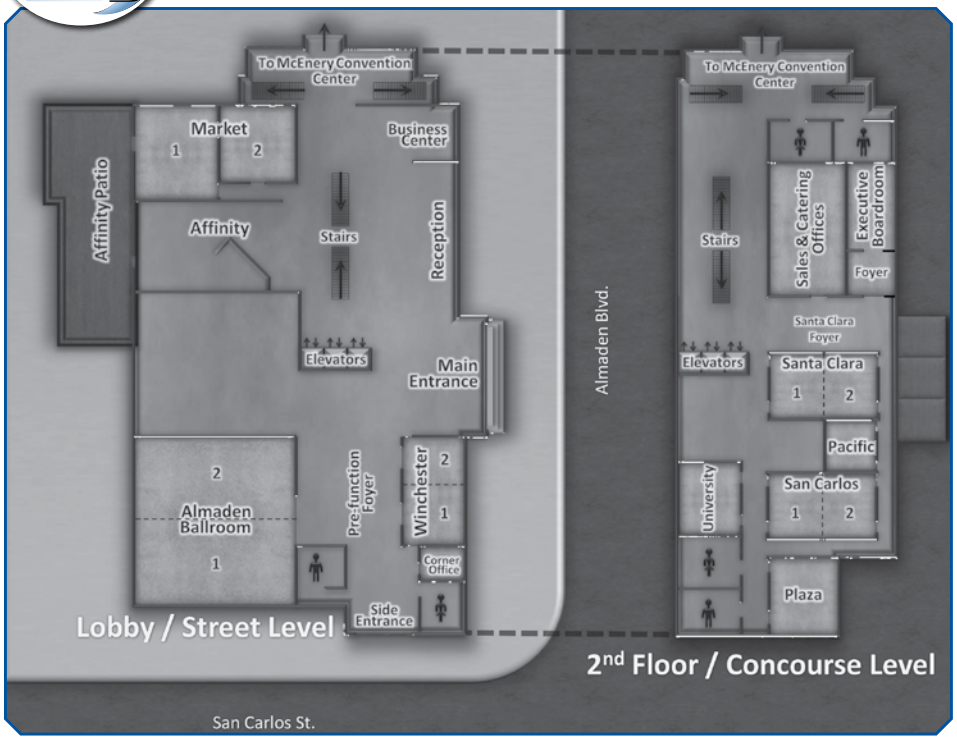
3D.1 SDC-Based Modulo Scheduling for Pipeline Synthesis
Zhiru Zhang - *Cornell Univ.*
Bin Liu - *Micron Technology, Inc.*

3D.2 Slack Matching Mode-Based Asynchronous Circuits for Average-case Performance
Mehrdad Najibi, Peter Beerel - *Univ. of Southern California*

3D.3 Sensitization Criterion for Threshold Logic Circuits and its Application
Chen-Kuan Tsai, Chun-Yao Wang, **Ching-Yi Huang** - *National Tsing Hua Univ.*
Yung-Chih Chen - *Yuan Ze Univ.*

3D.4 FPGA Acceleration of Enhanced Boolean Constraint Propagation for SAT Solvers
Jason Thong, Nicola Nicolici - *McMaster Univ.*





HILTON SAN JOSE

300 Almaden Blvd.
San Jose, CA 95110
408-287-2100

Tuesday, November 19

TIME	ALMADEN 1	ALMADEN 2	WINCHESTER	MARKET 1 & 2
8:30 - 10:00am	Session 4A: Thermal Management	Special Session 4B: 2013 CAD Contest	Session 4C: Modelling of Through Silicon Vias Parasitics and Shallow Trench Isolation Stress Effects	Session 4D: System-Level and Post-Silicon Validation
10:30am - 12:00pm	Session 5A: Power Considerations in System Design	Session 5B: Placement	Session 5C: Lifetime Analysis of TSV-Based 3D ICs	Session 5D: Test and Security for Analog and Mixed-Signal Circuits
12:00 - 1:45PM - Hyatt Hotel, Grand Hall Sponsored: CEDA **Invited Luncheon Keynote:** The Escalating Design Impact of Resolution-Challenged Lithography - **Lars Liebmann**, *IBM Corp.*				
2:00 - 4:00pm	Session 6A: To Remember or Not: Embedded Memories	Session 6B: Power, Timing and Noise Analysis and Optimization	Special Session 6C: Intelligent Compilation for Emulation and Acceleration	Session 6D: Analog and RF
4:30 - 6:30pm	Session 7A: Efficient and Secure Embedded Processors	Session 7B: Novel EM-IR for Power Grids	Special Session 7C: FPGA-Based Application Acceleration: Case Study with GZIP Compression/ Decompression Streaming Engine	Embedded Tutorial 7D: FinFET: A Multifaceted Perspective for CAD Engineers
Additional Meeting: ACM Student Research Competition Technical Presentations: 2:30 - 4:30pm - Santa Clara 1 & 2				
Networking Reception: 6:30 - 7:00pm - Almaden Foyer				
Additional Meeting: ACM/SIGDA Member Meeting: 7:00 - 8:30pm - Santa Clara 1 & 2				

Registration: 7:00am - 6:00pm - Almaden Foyer

Parking: $10 per day with in and out privileges

Speakers Breakfast: 7:30 - 8:30am - Santa Clara 1 & 2

AV Practice Rooms: 7:00am - 6:00pm - Pacific, Executive Boardroom, and University

TUESDAY, NOVEMBER 19 - 8:30 - 10:00am

All speakers are denoted in bold | * - denotes best paper candidate

4A Thermal Management
Room: Almaden 1

Moderators:

Sarma Vrudhula - *Arizona State Univ.*
Yiran Chen - *Univ. of Pittsburgh*

The papers in this session address different aspects of thermal modeling and management. The first paper extends dynamic thermal management to consider the coupling between components in mobile devices, such as processor and battery. The second paper addresses the need to verify increasingly complex and distributed dynamic thermal management schemes. The last paper proposes a thermal model for integrated systems that use two-phase liquid cooling.

4A.1 Dynamic Thermal Management in Mobile Devices Considering the Thermal Coupling Between Battery and Application Processor
Qing Xie, Yanzhi Wang, Massoud Pedram - *Univ. of Southern California*
Jaemin Kim, Naehyuck Chang - *Seoul National Univ.*
Donghwa Shin - *Politecnico di Torino*

4A.2 Formal Verification of Distributed Dynamic Thermal Management
Muhammad Ismail, Osman Hasan - *National Univ. of Science and Technology*
Thomas Ebi, **Muhammad Shafique**, Jörg Henkel - *Karlsruhe Institute of Technology*

4A.3 STEAM: A Fast Compact Thermal Model for Two-Phase Cooling of Integrated Circuits
Arvind Sridhar, David Atienza, John Thome - *Ecole Polytechnique Fédérale de Lausanne*
Yassir Madhour, Thomas Brunschwiler - *IBM Research - Zurich*

4B Special Session: **2013 CAD Contest**
Room: Almaden 2

Moderators:

Zhuo Li - *IBM T.J. Watson Research Center*
Iris Hui-Ru Jiang - *National Chiao Tung Univ.*

Organizers:

Yih-Lang Li - *National Chiao Tung Univ.*
Yao-Wen Chang - *National Taiwan Univ.*

Contests and their benchmarks have become an important driving force to push our EDA domain forward in different areas lately. The CAD Contest at ICCAD originates from the Taiwan CAD Contest and has been internationalized under the joint sponsorship of IEEE CEDA and Taiwan MOE since 2012. Continuing its great success in 2012, the 2013 CAD contest attracts 87 teams from 9 regions, achieving 55% growth. Three contest problems on technology mapping, detailed placement, and mask optimization are called for competition this year. This session presents the three contest problems, releases their benchmarks, and announces the contest results. This session also provides a forum for top final teams to disclose their key ideas and algorithms through video presentations.

4B.1 The Overview of 2013 CAD Contest at ICCAD
Iris Hui-Ru Jiang - *National Chiao Tung Univ.*
Zhuo Li - *IBM T.J. Watson Research Center*
Hwei-Tseng Wang - *Cadence Taiwan, Inc.*
Natarajan Viswanathan - *IBM Systems and Technology Group*

4B.2 ICCAD-2013 CAD Contest in Technology Mapping for Macro Blocks and Benchmark Suite
Feng Lu, Kei-Yong Khoo - *Cadence Design Systems, Inc.*
Hwei-Tseng Wang, Chih-Jen Hsu, Wei-Hsun Lin - *Cadence Taiwan, Inc.*

4B.3 ICCAD-2013 CAD Contest in Placement Finishing and Benchmark Suite
Myung-Chul Kim, Natarajan Viswanathan - *IBM Systems and Technology Group*
Zhuo Li, Charles Alpert - *IBM T.J. Watson Research Center*

4B.4 ICCAD-2013 CAD Contest in Mask Optimization and Benchmark Suite
Shayak Banerjee - *IBM Research - East Fishkill*
Sani R. Nassif, Damir Jamsek - *IBM Research - Austin*
Zhuo Li - *IBM T.J. Watson Research Center*

4C Modelling of Through Silicon Vias Parasitics and Shallow Trench Isolation Stress Effects

Room: Winchester

Moderators:

Yehia Massoud - *Worcester Polytechnic Institute*
Roberto Suaya - *Mentor Graphics Corp.*

This session describes the development of several models for physical phenomena in ICs and 3D ICs. Parasitic phenomena previously ignored are receiving more attention. Specifically, the first two papers model lateral resistance and capacitive coupling in TSV arrays. The third paper presents models to characterize the effects of shallow trench isolation stress on transistor mobility and hence on digital cell delays and leakage power.

4C.1 Compact Lateral Thermal Resistance Modeling and Characterization for TSV and TSV Array
Zao Liu, Sahana Swarup, Sheldon X.-D. Tan - *Univ. of California, Riverside*

4C.2 On Accurate Full-Chip Extraction and Optimization of TSV-to-TSV Coupling Elements in 3D ICs
Yarui Peng, Taigon Song, Sung Kyu Lim - *Georgia Institute of Technology*
Dusan Petranovic - *Mentor Graphics Corp.*

4C.3 The Impact of Shallow Trench Isolation Effects on Circuit Performance
Sravan Marella, Sachin Sapatnekar - *Univ. of Minnesota*

4D System-Level and Post-Silicon Validation

Room: Market 1 & 2

Moderators:

Masahiro Fujita - *Univ. of Tokyo*
Ric Huang - *National Taiwan Univ.*

The session consists for three papers addressing high-level, microarchitectural and post-silicon validation techniques. The first paper presents pattern mining techniques to localize causes of latency and throughput violations. The second paper uses virtual prototypes and concolic executions to derive tests for post-silicon validation. The final paper presents an approach to adapt assertion-based software verification of micro-architectures to hardware acceleration platforms.

4D.1 Diagnosing Root Causes of System Level Performance Violations
Lingyi Liu, Xuanyu Zhong, Shobha Vasudevan - *Univ. of Illinois at Urbana-Champaign*
Xiaotao Chen - *Huawei Technologies Co., Ltd.*

4D.2 Automatic Concolic Test Generation with Virtual Prototypes for Post-silicon Validation
Kai Cong, Fei Xie, Li Lei - *Portland State Univ.*

4D.3 Hybrid Checking for Microarchitectural Validation of Microprocessor Designs on Acceleration Platforms
Debapriya Chatterjee, **Biruk Mammo**, Doowon Lee, Valeria Bertacco - *Univ. of Michigan*
Raviv Gal, Ronny Morad, Amir Nahir, Avi Ziv - *IBM Research - Haifa*

All speakers are denoted in bold | * - denotes best paper candidate

5A Power Considerations in System Design
Room: Almaden 1

Moderators:

Sarma Vrudhula - *Arizona State Univ.*
Muhammad Shafique - *Karlsruhe Institute of Technology*

There are diverse tools available for circuit and system designers to achieve low power consumption and pursue power-performance trade-offs. The makeup of this session is a true reflection of this landscape. The first paper in this session proposes re-thinking the memory hierarchy to serve processor cores implemented with the near threshold technology. The second paper proposes a technique for constructing power gating domains for circuits described with a rule-based design language. Finally, the third paper will present a method for increasing opportunities for frequency boosting while maintaining safe voltage droop margins.

5A.1 Improving Platform Energy-Chip Area Trade-off in Near-Threshold Computing Environment
Hao Wang, Nam Sung Kim - *Univ. of Wisconsin*
Abhishek A Sinkar - *Oracle Corp.*

5A.2 Leveraging Rule-based Designs for Automatic Power Domain Partitioning
Abhinav Agarwal, Arvind - *Massachusetts Institute of Technology*

5A.3 Performance Boosting Under Reliability and Power Constraints
Youngtaek Kim, Lizy John - *Univ. of Texas at Austin*
Indrani Paul, Srilatha Manne, Michael Schulte - *Advanced Micro Devices, Inc.*

5B Placement
Room: Almaden 2

Moderators:

Dave Chinnery - *Mentor Graphics Corp.*
Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign*

The authors of the first paper propose a latch-placement algorithm targeting datapath-oriented designs. Latch clustering, sizing, and ordering are followed by (a) global latch-cluster placement by linear programming and (b) local latch placement based on network flows. The authors of the second paper propose a framework for triple-patterning-lithography (TPL)-friendly design based on specialized standard-cell compliance techniques, solution coloring, and detailed placement. Cell placement and color assignment are solved simultaneously, without the need for additional layout decomposition. In the third paper, a study of rough, look-ahead legalization in large-scale quadratic placement is presented. Expansion-region enumeration and recursive cell-distribution bisection are used to obtain excellent quality and run time.

5B.1 LatchPlanner: Latch Placement Algorithm for Datapath-oriented High-Performance VLSI Designs
Minsik Cho, Hua Xiang, Haoxing Ren, Matthew Ziegler, Ruchir Puri - *IBM T.J. Watson Research Center*

***5B.2 Methodology for Standard Cell Compliance and Detailed Placement for Triple Patterning Lithography**
Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, David Pan - *Univ. of Texas at Austin*

5B.3 POLAR: Placement Based on Novel Rough Legalization and Refinement
Tao Lin, Chris Chu - *Iowa State Univ.*
Ivailo Nedelchev, Joseph Shinnerl, Ismail Bustany - *Mentor Graphics Corp.*

5C Lifetime Analysis of TSV-Based 3D ICs

Room: Winchester

Moderators:

Qiang Xu - *Chinese Univ. of Hong Kong*
Guojie Luo - *Peking Univ.*

This session brings out novel ideas in addressing electromigration and fatigue issues in through-silicon vias in 3D ICs. The first paper translates the physcis of electromigration to build a characterized TSV library that can be used in power grid analysis. A method for analyzing and mitigating cracks in TSVs is proposed in the next paper. The session closes out with a study of the interactions between TSVs and intralayer vias used for power distribution.

5C.1 Transient Modeling of TSV-Wire Electromigration and Lifetime Analysis of Power Distribution Network for 3D ICs
Xin Zhao - *IBM Corp.*
Yang Wan, Sung Kyu Lim - *Georgia Institute of Technology*
Michael Scheuermann - *IBM T.J. Watson Research Center*

5C.2 Novel Crack Sensor Design for TSV-based 3D Integrated Circuits: Design and Deployment Perspectives
Chun Zhang, Yiyu Shi - *Missouri Univ. of Science and Technology*
Moongon Jung, Sung Kyu Lim - *Georgia Institute of Technology*

5C.3 Electromigration Study for Multi-scale Power/Ground Vias in TSV-based 3D ICs
Jiwoo Pak, David Pan - *Univ. of Texas at Austin*
Sung Kyu Lim - *Georgia Institute of Technology*

5D Test and Security for Analog and Mixed-Signal Circuits

Room: Market 1 & 2

Moderators:

Amit Majumder - *Xilinx, Inc.*
Abhilash Goyal - *Oracle Corp.*

This session highlights advances in parametric analog fault modeling based on Monte Carlo simulation. It also includes a novel defect-oriented design-for-test technique for the DAC array in source-driver ICs, and the first silicon results on hardware Trojan insertion and detection for wireless ICs.

5D.1 Scalable and Efficient Analog Parametric Fault Identification
Mustafa Yelten, Suriyaprakash Natarajan, Bin Xue, Prashant Goteti - *Intel Corp.*

5D.2 An IDDQ-Based Source Driver IC Design-for-Test Technique
Shih-Hsuan Lin, Jiun-Lang Huang, Chia-Lung Kao - *National Taiwan Univ.*
Chuan-Che Lee - *Himax Technologies, Inc.*
Xuan-Lun Huang - *Industrial Technology Research Institute*

5D.3 Hardware Trojans in Wireless Cryptographic ICs: Silicon Demonstration and Detection Method Evaluation
Yu Liu, Yiorgos Makris - *Univ. of Texas at Dallas*
Yier Jin - *Univ. of Central Florida*

Invited Luncheon Keynote: Sponsored by: CEDA

The Escalating Design Impact of Resolution-Challenged Lithography

Organizer: Joel Phillips - *Cadence Design Systems, Inc.*

Hyatt Hotel - Grand Hall

Lars Liebmann - *IBM Corp.* For the first three decades of semiconductor scaling, the exponential increase in transistor density was largely driven by lithography resolution. Manufacturability and design efficiency were achieved through periodic increases in numerical aperture and reduction in exposure wavelength at a pace that kept the effective patterning complexity fairly constant node-to-node. This all changed almost exactly 30 years after Robert Dennard published his seminal paper describing MOSFET scaling rules in 1974. When the industry hit what most referred to as the 130nm technology node, existing 193nm wavelength lithography tools were rapidly running out of resolution with no real relief in sight until the massively disruptive introduction of extreme ultraviolet (EUV) lithography.

What followed was more than a decade of technology nodes that ever more blatantly violated the fundamental laws of lithography resolution. The semiconductor industry was being kept alive by 'Computational Scaling', a series of increasingly complex resolution enhancement techniques (RET) with growing impact on design. This era of 'sub-resolution scaling' reached unprecedented levels of lithography-driven design impact with the introduction of double patterning in the 14nm technology node and continues to escalate as we extend 193nm optical lithography further past its physical limits.

This talk will briefly review the path leading up to the use of double patterning, elaborate on the challenges introduced by double patterning, and provide and overview of the solutions implemented to overcome these challenges. Unfortunately, the battle for resolution does not end there. The continued uncertainty surrounding the availability of EUV lithography for volume manufacturing forces the industry to eek out at least one more technology node with the existing lithography toolset. While the 14nm technology node pioneered the use of double patterning, the 10nm node 'kicks it up a notch' on the complexity scale.

As will be shown, moving from double to triple patterning and introducing self-aligned double patterning through sidewall image transfer requires fundamental innovation in design rules, design methodologies, and design automation tooling. The ultimate goal of this presentation is to communicate the sense of urgency with which we need to implement these innovative design solutions to maintain semiconductor scaling feasibility in this resolution challenged environment.

TUESDAY, NOVEMBER 19 - 2:00 - 4:00pm

6A To Remember or Not: Embedded Memories
Room: Almaden 1

Moderator:
Paul Bogdan - *Univ. of Southern California*
Philip Brisk - *Univ. of California, Riverside*

The authors of the first paper propose applicatin specific hybrid memories for HEVC standards. The second paper examines cachememoriy reconfigaration during runtime. The final two papers examine methods to improve lifetime in non-volatile memories.

6A.1 AMBER: Adaptive Energy Management for On-Chip Hybrid Video Memories
Muhammad Usman Karim Khan, Muhammad Shafique, Jörg Henkel - *Karlsruhe Institute of Technology*

6A.2 Thread-Criticality Aware Dynamic Cache Reconfiguration in Multi-core System
Po-Yang Hsu, Tingting Hwang - *National Tsing Hua Univ.*

6A.3 A Disturb-Alleviation Scheme for 3D Flash Memory
Yu-Ming Chang, Hsiang-Pang Li, Yung Chun Li - *Macronix International Co., Ltd.*
Yuan-Hao Chang - *Academia Sinica*
Tei-Wei Kuo - *National Taiwan Univ.*

***6A.4 Unleashing the Potential of MLC STT-RAM Caches**
Xiuyuan Bi, Mengjie Mao, Hai Li - *Univ. of Pittsburgh*
Danghui Wang - *Northwestern Polytechnical Univ.*

6B Power, Timing and Noise Analysis and Optimization
Room: Almaden 2

Moderators:
Jia Wang - *Illinois Institute of Technology*
Mondira Pant - *Intel Corp.*

This session features four papers that deal with the analysis and optimization of power, timing, and noise. The first paper proposes a method to detect voltage drops by optimal placement of noise sensors on the chip.. The second and third papers address gate sizing for either timing or power. The fourth paper introduces power macromodels to help estimating the power consumption of designs comprising many IP blocks.

6B.1 Eagle-Eye: A Near-Optimal Statistical Framework for Noise Sensor Placement
Tao Wang, Chun Zhang, Yiyu Shi - *Missouri Univ. of Science and Technology*
Jinjun Xiong - *IBM Research*

6B.2 Joint Sizing and Adaptive Independent Gate Control for FinFET Circuits Operating in Multiple Voltage Regimes Using the Logical Effort Method
Xue Lin, Yanzhi Wang, Massoud Pedram - *Univ. of Southern California*

6B.3 High-Performance Gate Sizing with a Signoff Timer
Andrew Kahng, Seokhyeong Kang, **Hyein Lee** - *Univ. of California at San Diego*
Igor Markov, Pankit Thapar - *Univ. of Michigan*

6B.4 Efficient PVT Independent Abstraction of Large IP Blocks for Hierarchical Power Analysis
Nagu Dhanwada, David Hathaway, Victor Zyuban, Peng Peng, Karl Moody, William Dungan, Arun Joseph, Rahul Rao, Christopher Gonzalez - *IBM Corp.*

All speakers are denoted in bold | * - denotes best paper candidate

6C Special Session: Intelligent Compilation for Emulation and Acceleration

Room: Winchester

Moderator:
Valeria Bertacco - *Univ. of Michigan*

Organizer:
Michael D. Moffitt - *IBM Corp.*

Due to the rapidly increasing demand for high simulation throughput and performance, hardware emulation and acceleration continue to dominate state-of-the-art methodologies for functional verification. These systems typically employ FPGAs or custom ASICs to enable orders-of-magnitude speedups as compared to conventional software simulators, and are capable of supporting massive model sizes with millions (and sometimes billions) of gates. Although modern systems for logic simulation are finely tuned to optimize concurrency and communication, the ability to effectively and efficiently map netlists to the architecture of each specific platform is ultimately up to the compiler. This special session provides an industrial perspective on how successful compilation is achieved through parallel processing, design partitioning, and resource-aware scheduling.

6C.1 Place and Route for Massively Parallel Hardware-Accelerated Functional Verification
Michael D. Moffitt, Gernot E. Günther, Kevin A. Pasnik - *IBM Corp.*

6C.2 Techniques and Challenges of Implementing Large Scale Logic Design Models in Massively Parallel Fine-Grained Multiprocessor Systems
Platon Beletsky, **Mike Bershteyn**, Alexandre Birguer, Chunkuen Ho, Viktor Salitrennik - *Cadence Design Systems, Inc.*

6C.3 Parallel Computation for System Level Emulation Compilation
Charley Selvidge - *Mentor Graphics Corp.*

6C.4 Timing-Driven Partitioning/Placement for High-Performance Emulation Models
Vivek Prasad - *Synopsys, Inc.*

6D Analog and RF

Room: Market 1 & 2

Moderators:
Eric Keiter - *Sandia National Laboratories*
Raj Raghuram - *Berkeley Design Automation*

This session addresses important issues in the statistical analysis, verification, effective simulation and noise modelling of analog and RF systems. The first paper presents a simple yet efficient technique for estimating rare failures in high-dimensional spaces. The second paper tackles the problem of verifying correct oscillator functionality. The third paper introduces a new sparsification technique for addressing the long-standing problem of harmonic balance preconditioning. The final paper presents a technique for bottom-up modelling of non-stationary noise in devices using particle concepts from chemical kinetics.

6D.1 Fast Statistical Analysis of Rare Circuit Failure Events via Scaled-Sigma Sampling for High-Dimensional Variation Space
Shupeng Sun, Xin Li - *Carnegie Mellon Univ.*
Hongzhou Liu, Kangsheng Luo, Ben Gu - *Cadence Design Systems, Inc.*

6D.2 Verifying Start-up Failures in Coupled Ring Oscillators in Presence of Variability Using Predictive Global Optimization
Taehwan Kim, Do-Gyoon Song, Sangho Youn, Jaeha Kim - *Seoul National Univ.*
Jaejin Park, Hojin Park - *Samsung Electronics Co., Ltd,*

6D.3 An Efficient Graph Sparsification Approach to Scalable Harmonic Balance (HB) Analysis of Strongly Nonlinear RF Circuits
Lengfei Han, Xueqian Zhao, Zhuo Feng - *Michigan Technological Univ.*

6D.4 Modeling and Analysis of (Nonstationary) Low Frequency Noise in Nano Devices: A Synergistic Approach based on Stochastic Chemical Kinetics
Ahmet Gokcen Mahmutoglu, Alper Demir - *Koc Univ.*
Jaijeet Roychowdhury - *Univ. of California, Berkeley*

AM Additional Meeting: **ACM Student Research Competition Technical Presentations**
Room: Santa Clara 1 & 2

Organizers:

Srinivas Katkoori - *University of South Florida*
Miroslav Velev - *Aries Design Automation*

The ACM Student Research Competition allows both graduate and undergraduate students to discuss their research with student peers, as well as academic and industry researchers, in an informal setting, while enabling them to attend ICCAD.

This session is the final round of ACM SRC at ICCAD 2013. Each student will present for 10 minutes, followed by a 5-minute question and answer period. This session will be attended by the evaluators and any interested conference attendees. The top three winners in each category will be chosen based on these presentations.

The undergraduate and graduate finalists are eligible to compete in the ACM SRC Grand Finals to be held in June 2014.

More details can be found at: **www.sigda.org/src**

Sponsored By:

Microsoft Research

acm

sigda special interest group on design automation

TUESDAY, NOVEMBER 19 - 4:30 - 6:30pm

All speakers are denoted in bold | * - denotes best paper candidate

7A Efficient and Secure Embedded Processors
Room: Almaden 1

Moderators:

Qi Zhu - *Univ. of California, Riverside*
Hiren Patel - *Univ. of Waterloo*

The authors of the first paper propose a novel memory controller-aware mapping for software pipelined applications. The second paper presents a compiler for bypassing caches in GPUs for improved performance. The third paper presents a runtime adaptable instruction-set extensible architecture. The final paper proposes a novel method to detect hardware Trojans using temperature tracking.

7A.1 MOMA: Mapping of Memory-intensive Software-pipelined Applications for Systems with Multiple Memory Controllers
Janmartin Jahn, Santiago Pagani, Jian-Jia Chen, Jörg Henkel - *Karlsruhe Institute of Technology*

7A.2 An Efficient Compiler Framework for Cache Bypassing on GPUs
Xiaolong Xie, **Yun Liang**, Guangyu Sun - *Peking Univ.*
Deming Chen - *Univ. of Illinois at Urbana-Champaign*

7A.3 A Just-in-Time Customizable Processor
Liang Chen, Tulika Mitra - *National Univ. of Singapore*
Joseph Tarango, Philip Brisk - *Univ. of California, Riverside*

7A.4 Temperature Tracking: An Innovative Run-Time Approach for Hardware Trojan Detection
Domenic Forte - *Univ. of Connecticut*
Chongxi Bao, Ankur Srivastava - *Univ. of Maryland*

7B Novel EM-IR for Power Grids
Room: Almaden 2

Moderators:

Rajendran Panda - *Oracle Corp.*
Iris Hui-Ru Jiang - *National Chiao Tung Univ.*

This session will showcase powerful new techniques for power grid noise simulation and for estimating electromigration reliability. The first paper introduces a way to reduce pessimism in estimating EM failure by considering the redundancy in the power grid. The second paper applies the mesh-based EM failure model of the first paper to do vectorless EM estimation. The third paper applies model order reduction to enable efficient dynamic power grid simulations in parallel. The last paper leverages the massive parallelization opportunity with GPUs to speed-up power grid simulation.

***7B.1 Redundancy-Aware Electromigration Checking for Mesh Power Grids**
Sandeep Chatterjee, Mohammad Fawaz, Farid Najm - *Univ. of Toronto*

7B.2 Scalable Power Grid Transient Analysis via MOR-Assisted Time Domain Simulations
Jia Wang, Xuanxing Xiong - *Illinois Institute of Technology*

7B.3 A Vectorless Framework for Power Grid Electromigration Checking
Mohammad Fawaz, Sandeep Chatterjee, Farid Najm - *Univ. of Toronto*

7B.4 Parallel Power Grid Analysis Using Preconditioned GMRES Solver on CPU-GPU Platforms
Xuexin Liu, Sheldon X.-D. Tan - *Univ. of California, Riverside*
Hai Wang - *Univ. of Science and Technology of China*

7C Special Session: FPGA-Based Application Acceleration: Case Study with GZIP Compression/ Decompression Streaming Engine

Room: Winchester

Moderator:
Derek Chiou - *Univ. of Texas at Austin*

Organizer:
Gi-Joon Nam - *IBM Research - Austin*

With ever-increasing demands for performance and challenging technology constraints, the higher performance computing research has been exploring the venue of heterogeneous system architecture that combines multiple types of processor cores sharing memory. In recent research, FPGA or GPU accelerator-based hybrid architecture is considered as one of the most feasible and promising ways to improve the overall system throughput for various types of applications. In this special session, the authors give the tutorial presentations on the detailed implementation of GZIP compression/decompression streaming engine via FPGA accelerator attached to the host microprocessor. Several interesting topics will be covered ranging the whole stacks of system level design from overall architecture to middle-ware design to FPGA synthesis CAD techniques. Finally the performance of compression/decompression engine attached to the industrial server architecture will be presented.

Speakers:
Andrew Martin, Damir Jamsek, Kanak Agarwal - *IBM Research - Austin*

7D Embedded Tutorial: FinFET: A Multifaceted Perspective for CAD Engineers

Room: Market 1 & 2

Organizer:
Rasit O. Topaloglu - *IBM Corp.*

With CMOS technology pushing the boundaries of 10nm technology, FinFET (3D) devices are proving to be the next generation device technology. FinFETs have appeared in 22nm production first, and are now being used at 14nm. It seems to be the case that 10nm and beyond may also require this device type in one form or another and potentially with new materials. Hence, a thorough understanding of this new device type and the underlying impact on integrated circuit design is necessary. This session covers modeling, TCAD, and design aspects of integrated circuits with FinFETs. The session consists of four parts. FinFETs are manufactured using multiple fins of silicon. The new devices require new device models. The first talk covers device modeling aspects. It focuses on the need to model the channel charge control and how to efficiently model it without deviating significantly from known modeling techniques. Fast and accurate simulations that utilize available models are furthermore necessary. In order to extend the CMOS device reach beyond the 10nm barrier, TCAD is a key enabler to quickly validate device architecture. The second talk focuses on the TCAD aspects and what needs to change with respect to what was available for planar devices so that atomistic interactions can be accounted for. Transitioning to a new device type may require significant infrastructure changes. However, it is necessary to minimize these changes with respect to previous nodes. The third talk outlines the design impact of moving to FinFETs. The talk discusses design rules, design patterns, and variability aspects and how the CAD tools can or should adopt the new changes. Finally, all these need to be utilized in designing larger circuits and intellectual property (IP). The final talk combines these aspects and presents on design of IP that utilizes FinFET technology.

Presenters:
Chenming Hu - *Univ. of California, Berkeley*
Gerhard Klimeck - *Purdue Univ.*
Rasit O. Topaloglu - *IBM Corp.*
Vikas Chandra - *ARM, Ltd.*

7D.1 Design with FinFETs: Design Rules, Patterns, and Variability
Rasit Topaloglu - *IBM Corp.*

ADDITIONAL MEETING: ACM/SIGDA Member Meeting

Room: Santa Clara 1 & 2

Presenter: Donald E. Thomas - SIGDA Pioneering Achievement Award Recipient

The annual ACM/SIGDA Member Meeting will be held on Tuesday evening from 7-8:30pm. The meeting is open to everyone in the EDA community and we especially encourage ACM SIGDA members (or those considering becoming members) to attend. Finger food and beverages will be provided. The meeting will begin with a brief overview of our group, including its organization, activities, volunteering opportunities, member benefits, etc. We will then announce the winners of the Student Research Competition taking place at this year's ICCAD. Finally, we will proceed to an informal talk by this year's SIGDA Pioneering Achievement award recipient, Professor Donald E. Thomas. With this award, he is being recognized for his pioneering work in making the Verilog Hardware Description Language more accessible for the design automation community and allowing for faster and easier pathways to simulation, high-level synthesis, and co-design of hardware-software systems. We hope to see you there!

Sponsored by:

Wednesday, November 20

9:00 - 10:00AM - Room: Almaden 1 & 2 - Keynote Address: Networks of NMOS and Neurons
Louis K. Scheffer, *Janelia Farm, Howard Hughes Medical Institute*

TIME	ALMADEN 1	ALMADEN 2	WINCHESTER	MARKET 1 & 2
10:30am - 12:00pm	Embedded Tutorial 8A: Beyond Charge-Based Computing	Designer Track 8B: Verification of Large Scale Designs	Session 8C: Tree Optimization in Physical Synthesis	Session 8D: New Frontiers in EDA for Neural and Microfluidic Circuits
12:00 - 1:45pm	**LUNCH:** Second Floor by Santa Clara Room			
2:00 - 4:00pm	Session 9A: Customized and Heterogeneous Architectures	Session 9B: Formal and Symbolic Verification	Session 9C: Clock Synthesis, ECO, and PCB Routing	Special Session 9D: Just Like How We Designed VLSI Circuit and System: Design Automation is Also Essential to System Biology
4:30 - 6:30pm	Session 10A: Emerging System Level Design	Session 10B: Advances in Logic Synthesis	Special Session 10C: Stochastic Circuit Simulation	Special Session 10D: Trustworthy Hardware
Networking Reception: 6:30 - 7:00pm - Almaden Foyer				

Registration: 7:00am - 6:00pm - Almaden Foyer
Speakers Breakfast: 7:30 - 8:30am - Santa Clara 1 & 2
Parking: $10 per day with in and out privileges
AV Practice Rooms: 7:00am - 4:00pm - Pacific, Executive Boardroom, and University

KEYNOTE:

Networks of NMOS and Neurons

Presenter: Louis K. Scheffer - *Janelia Farm, Howard Hughes Medical Institute*

Room: Almaden 1 & 2

Biology and electronics have yet to build truly integrated systems, despite the obvious promise. The interactions of existing systems are almost all one way, from electronics to the brain as in cochlear implants and from the brain to electronics in the case of prosthetics.

Furthermore, the interface models used are entirely empirical and adaptation is left to the unknown mechanisms of the brain. This situation is sure to change with better interfaces, better biology, and in particular better understanding of the brain. The time is ripe for such advances - interest is high, the technical tools needed to understand the brain are advancing at a good clip, and the political and funding environment is favorable. This talk will review this area, looking at the formidable challenges but huge opportunities that await.

Lou Scheffer is a fellow at the Janelia Farm Research Campus of the Howard Hughes Medical Institute. His research there is on the structure and function of the nervous system, using the optical lobes of the fruit fly as a model organism. Before that, he spent about 30 years in EDA, mostly with Cadence Design Systems, and before that was a chip designer. His main outside interest is in SETI, the search for extraterrestrial intelligence. He graduated from Caltech and Stanford, and is the author of the usual books, papers, and patents.

8A Embedded Tutorial: **Beyond Charge-Based Computing**

Room: Almaden 1

Moderator:

Arijit Raychowdhury - *Georgia Institute of Technology*

The trend towards ultra low power logic and low leakage embedded memories for Systems-On-Chip, has prompted research to consider the possibility of replacing charge as the state variable for computation and storage. Recent experiments on spin devices like magnetic tunnel junctions (MTJ's), domain wall magnets (DWM) and spin valves have led to the possibility of using "spin" as state variable for computation, achieving very high density on-chip memories and ultra low voltage logic. Spin-transfer-torque (STT)-RAM which stores data by the spin orientation of a soft ferromagnetic material and shows current induced switching, is being actively investigated for its use as embedded memory. In the first half of this talk, we will examine the physics of operation of STT and describe physical, numerical and compact models for device-circuit and architectural analysis. We will put particular emphasis on recent advances in the 1T-1R bit-cell, for dense embedded memory applications.

The second half of the talk will emphasize on design paradigms for non-charge based logic design. While the possibility of having on-chip spin transfer torque memories is close to reality, several questions still exist regarding the energy benefits of spin as the state variable for logic computation. Latest experiments on lateral spin valves (LSV) have shown switching of nano-magnets using spin-polarized current injection through a metallic channel such as Cu. Such lateral spin valves having multiple input magnets connected to an output magnet using metal channels can be used to mimic "neurons". The spin-based neurons can be integrated with CMOS and other devices like Phase change memories to realize ultra low-power data processing hardware based on neural networks, and are suitable for different classes of applications like, cognitive computing, programmable Boolean logic and analog and digital signal processing. We will also consider recent advances in other non-charge based computing paradigm such as magnetic quantum cellular automata.

8A.1 Spin Torque Devices in Embedded Memory: Model Studies and Design Space Exploration
Arijit Raychowdhury - *Georgia Institute of Technology*

8A.2 Exploring Boolean and Non-Boolean Computing with Spin Torque Devices
Kaushik Roy, Mrigank Sharad, Deliang Fan, Karthuk Yogendra - *Purdue Univ.*

8B Designer Track: **Verification of Large Scale Designs**

Room: Almaden 2

Moderator:

Jie-Hong (Roland) Jiang - *National Taiwan Univ.*

Organizer:

Diana Marculescu - *Carnegie Mellon Univ.*

With sheer complexity come challenges in verifying whether designs comply with specifications. This session covers advances in verification methodologies and tools for large scale designs that are in use by leaders in large scale design verification.

8B.1 Why the Design Productivity Gap Never Happened
Harry Foster - *Mentor Graphics Corp.*

8B.2 The Challenges of Validating Large Intel CPU and SOC Designs
Blair Milburn - *Intel Corp.*

8B.3 Verification Building Blocks: An IBM Perspective
Hari Mony, Viresh Paruthi, Jason Baumgartner, Wolfgang Roesner - *IBM Systems and Technology Group*

All speakers are denoted in bold | * - denotes best paper candidate

8C Tree Optimization in Physical Synthesis

Room: Winchester

Moderators:

Joseph Shinnerl - *Mentor Graphics Corp.*
Atsushi Takahashi - *Tokyo Institute of Technology*

This session presents new tree optimization techniques for physical synthesis. The authors of the first paper restructure symmetric-function fanin tree to improve routability and timing. The second paper performs clock-tree aware flip-flops merging to reduce power. In the third paper, local clock tree capacitance is reduced in order to optimize clock power.

8C.1 Depth Controlled Symmetric Function Fanin Tree Restructure
Hua Xiang, Louise Trevillyan, Ruchir Puri - *IBM T.J. Watson Research Center*
Lakshmi Reddy - *IBM Systems and Technology Group*

8C.2 In-Placement Clock-Tree Aware Multi-Bit Flip-Flop Generation for Power Optimization
Chih-Cheng Hsu, Yu-Chuan Chen, Mark Po-Hung Lin - *National Chung Cheng Univ.*

8C.3 Clock Power Minimization Using Structured Latch Templates and Decision Tree Induction
Samuel Ward, David Pan - *Univ. of Texas at Austin*
Natarajan Viswanathan - *IBM Systems and Technology Group*
Nancy Zhou, Cliff C.N. Sze, Zhuo Li, Charles Alpert - *IBM Research - Austin*
Zhuo Li - *IBM T. J. Watson Research Center*

8D New Frontiers in EDA for Neural and Microfluidic Circuits

Room: Market 1 & 2

Moderators:

Evangeline Young - *Chinese Univ. of Hong Kong*
Hsiao-Chun Huang - *National Taiwan Univ.*

This session includes three interesting papers that explore design automation and simulation techniques for neural and microfluidic circuits. The first paper describes an FPGA-based simulation platform for neural microcircuits that provides automatic optimization and fast design exploration. The next two papers address the problem of minimizing reagent consumption in microfluidic lab-on-chip experiments. In particular, the second paper in this session proposes a new algorithm for preparing solutions in digital microfluidic biochips that considers multiple reactants with varying costs. The session ends with a paper describing an integrated design method for optimizing amplification and testing stages of bio-experiments using DNA strands.

8D.1 FPGA Simulation Engine for Customized Construction of Neural Microcircuits
Hugh Blair, Jason Cong, **Di Wu** - *Univ. of California, Los Angeles*

8D.2 Sample Preparation for Many-Reactant Bioassay on DMFBs Using Common Dilution Operation Sharing
Chia-Hung Liu, Hao-Han Chang, Tung-Che Liang, Juinn-Dar Huang - *National Chiao Tung Univ.*

8D.3 Optimization of Polymerase Chain Reaction on a Cyberphysical Digital Microfluidic Biochip
Yan Luo, Krishnendu Chakrabarty - *Duke Univ.*
Bhargab Bhattacharya - *Indian Statistical Institute*
Tsung-Yi Ho - *National Cheng Kung Univ.*

9A Customized and Heterogeneous Architectures
Room: Almaden 1

Moderators:

Yosinori Watanabe - *Cadence Design Systems, Inc.*
Younghyun Kim - *Seoul National Univ.*

This session presents approaches for critical problems of today's system designs. The first paper describes how to generate an NoC architecture for speciialized accelerator-memory communication. The second paper addresses the problem of word-length optimization, where an effective herusitic to address the NP-hard probem is presented. The third paper presents an approach for reliability of multi-core systems on soft-errors based on task-specific resilience characteristics. The fourth paper considers workload traces to optimize power-performance trade-offs on multi-core systems.

9A.1 Optimization of Interconnects Between Accelerators and Shared Memories in Dark Silicon
Jason Cong, **Bingjun Xiao** - *Univ. of California, Los Angeles*

***9A.2 A Polynomial Time Algorithm for Solving the Word-Length Optimization Problem**
Karthick Nagaraj Parashar, Olivier Sentieys - *INRIA Rennes - Bretagne Atlantique*
Daniel Menard - *Institut National des Sciences*

9A.3 DHASER: Dynamic Heterogeneous Adaptation for Soft-Error Resiliency in ASIP-based Multi-core Systems
Tuo Li, Jude Angelo Ambrose, Sri Parameswaran - *Univ. of New South Wales*
Muhammad Shafique, Semeen Rehman, Jörg Henkel - *Karlsruhe Institute of Technology*

9A.4 Trace Alignment Algorithms for Offline Workload Analysis of Heterogeneous Architectures
Mustafa Ozdal, Aamer Jaleel, Paolo Narvaez, Steven Burns, Ganapati Srinivasa - *Intel Corp.*

9B Formal and Symbolic Verification
Room: Almaden 2

Moderator:

Miroslav Velev - *Aries Design Automation, LLC*
Yirng-An Chen - *Marvell Semiconductor Inc.*

The session consists for four papers addressing formal verification technique. The first paper proposes the concept of statistical model inference for analog circuits. The second paper proposes a FPGA platform for accelerating statistical model checking. The third paper describes a polynomial algebra method to unify proof logging in an SMT-solver environment. The final paper presents a new method to reduce the scheduling alternatives for formal analysis of SystemC designs.

9B.1 From Statistical Model Checking to Statistical Model Inference: Characterizing the Effect of Process Variations in Analog Circuits
Yan Zhang, Sriram Sankaranarayanan, Fabio Somenzi - *Univ. of Colorado*
Xin Chen, Erika Abraham - *RWTH Aachen Univ.*

9B.2 Hardware Implementation of BLTL Property Checkers for Acceleration of Statistical Model Checking
Kosuke Oshima, Takeshi Matsumoto, Masahiro Fujita - *Univ. of Tokyo*

9B.3 Proof Logging for Computer Algebra based SMT Solving
Oliver Marx, Markus Wedler, Dominik Stoffel, Wolfgang Kunz - *Univ. of Kaiserslautern*
Alexander Dreyer - *Fraunhofer ITWM*

9B.4 Conquering the Scheduling Alternative Explosion Problem of SystemC Symbolic Simulation
National Taiwan Univ.

All speakers are denoted in bold | * - denotes best paper candidate

9C Clock Synthesis, ECO, and PCB Routing

Room: Winchester

Moderators:

Lars Hagen - *Cadence Design Systems, Inc.*
Thorlindur Thorolfsson - *Synopsys, Inc.*

The first two papers propose tenchieques and methodologies for clock network synthesis and optimization for modern 3D and low-power designs. The third paper considers scan-chain ordering for ECO optimization. The last paper focuses on improving the signal integraty in PCB routing.

9C.1 Comprehensive Technique for Designing and Synthesizing TSV Fault-Tolerant 3D Clock Trees
Heechun Park, Taewhan Kim - *Seoul National Univ.*

9C.2 Low-Power Timing Closure Methodology for Ultra-Low Voltage Designs
Wen-Pin Tu, Shih-Hsu Huang - *Chung Yuan Christian Univ.*
Chung-Han Chou, Shih-Chieh Chang - *National Tsing Hua Univ.*
Yow-Tyng Nieh, Chien-Yung Chou - *Industrial Technology Research Institute*

9C.3 Incremental Multiple-Scan Chain Ordering for ECO Flip-Flop Insertion
Andrew Kahng, **Ilgweon Kang**, Siddhartha Nath - *Univ. of California at San Diego*

9C.4 Post-Route Alleviation of Dense Meander Segments in High-Performance Printed Circuit Boards
Tsun-Ming Tseng, **Bing Li,** Ulf Schlichtmann - *Technical Univ. of Munich*
Tsung-Yi Ho - *National Cheng Kung Univ.*

9D Special Session: Just Like How We Designed VLSI Circuit and System: Design Automation is Also Essential to System Biology

Room: Market 1 & 2

Moderator:

Janet Roveda - *Univ. of Arizona*

Organizer:

Janet Roveda - *Univ. of Arizona*

Computer based models and CAD tools are essential to integrate together jigsaw pieces of information from different technologies for system biology. However, in addition to scalability issue, we also face diversity and uncertainty problems. In the first talk, Dr. Wenzhe Ma will present their recent work in identifying adaptations through enumerating a large set of small abstracted networks. In the second talk, Prof. Marc Riedel will present a methodology for implementing digital logic with molecular reactions based on a bistable mechanism for representing bits. In the third talk, Dr. Nathan J. Hillson will discuss how the capacity to iterate through the biological design-build-test engineering cycle more quickly than the competition is mission critical for academics and biotechnology companies to be the first to publish or bring product to market. From Electronics 101 we learn how noise is exploited in electrical circuits, for instance in oscillator, noise acts as the initial signal to get oscillation started in the amplifier-filter loop. In the last talk, Prof. Huang will introduce what noise can do in cellular processes: it can be beneficial from evolutionary or differentiation perspective, or it can lead to undesirable outcomes in cancer therapeutics.

9D.1 Computational Study of Network Topologies that Can Achieve Biochemical Adaptation
Wenzhe Ma - *Harvard Univ.*

9D.2 Digital Logic with Molecular Reactions
Hua Jiang, **Marc Riedel**, Keshab Parhi - *Univ. of Minnesota*

9D.3 Biological Design and Build Automation Platforms at JBEI and TeselaGen
Nathan Hillson - *Lawrence Berkeley National Lab*

9D.4 Noise in Genetic Circuits: Hindrance or Chance?
Cheng-Ju Pan, **Hsiao-Chun Huang** - *National Taiwan Univ.*

10A Emerging System Level Design

Room: Almaden 1

Moderators:

Felice Balarin - *Cadence Design Systems, Inc.*
Cheng Zhuo - *Intel Corp.*

This session focuses on system design issues for emerging technologies. The first paper defines sequential logic to transform the probabilities of probabilistic streams for stochastic processing. The second paper proposes using BDDs to automatically generate instruction decoders for non-orthogonal instruction sets. The third paper demonstrates how to reduce the latency and power consumption of 3D stacked memories and quantifies. The fourth paper is an integrated approach to efficiently mapping computation to a dynamically reconfigurable fabric.

10A.1 Sequential Logic to Transform Probabilities
Naman Saraf, **Kia Bazargan** - *Univ. of Minnesota, Twin Cities*

10A.2 Automated Generation of Efficient Instruction Decoders for Instruction Set Simulators
Nicolas Fournel, Luc Michel, Frédéric Pétrot - *TIMA Laboratory, CNRS/Grenoble INP/UJF*

10A.3 Dynamic Bandwidth Scaling for Embedded DSPs with 3D-Stacked DRAM and Wide I/Os
Daniel Chang, Nam Sung Kim - *Univ. of Wisconsin*
Younghoon Son, Jung Ho Ahn - *Seoul National Univ.*
Hoyoung Kim, Minwook Ahn - *Samsung Electronics Co., Ltd,*
Michael Schulte - *Advanced Micro Devices, Inc.*

10A.4 ISOMER: Integrated Selection, Partitioning and Placement Methodology for Reconfigurable Architectures
Rana Muhammad Bilal, **Rehan Hafiz,** Saad Shoaib - *National Univ. of Science and Technology*
Muhammad Shafique, Jörg Henkel - *Karlsruhe Institute of Technology*
Asim Munawar - *IBM Research*

10B Advances in Logic Synthesis

Room: Almaden 2

Moderators:

Alan Mishchenko - *Univ. of California, Berkeley*
Chun-Yao Wang - *National Tsing Hua Univ.*

This session comprises four papers addressing practical problems in logic synthesis. The first paper presents an efficient approach to finding generalized Booleas symmetries. The second paper poses the encoding problem with the objective of maximizing partial and full symmetries. The third paper addresses the problem of approximate logic synthesis and explores an approach for buliding a minimum-cost Boolean network whose behavior deviates minimally from the specifications. The fourth paper presents techniques for partial synthesis where some parts of the target circuit are fixed but some parts are missing and must be synthesized.

10B.1 Generalized Boolean Symmetries Through Nested Partition Refinement
Hadi Katebi, Karem Sakallah, Igor Markov - *Univ. of Michigan*

10B.2 Encoding Multi-Valued Functions for Symmetry
Ko-Lung Yuan, Chien-Yen Kuo, **Jie-Hong Roland Jiang** - *National Taiwan Univ.*
Meng-Yen Li - *Industrial Technology Research Institute*

10B.3 Approximate Logic Synthesis Under General Error Magnitude and Frequency Constraints
Jin Miao, Andreas Gerstlauer, Michael Orshansky - *Univ. of Texas at Austin*

10B.4 Partial Synthesis Through Sampling with and Without Specification
Masahiro Fujita, **Satoshi Jo**, Shohei Ono, Takeshi Matsumoto - *Univ. of Tokyo*

All speakers are denoted in bold | * - denotes best paper candidate

All speakers are denoted in bold | * - denotes best paper candidate

10C Special Session: **Stochastic Circuit Simulation**
Room: Winchester

Moderator:
Ibrahim (Abe) M. Elfadel - *Masdar Institute of Science and Technology*

Organizer:
Ibrahim (Abe) M. Elfadel - *Masdar Institute of Science and Technology*

This Special Session brings together experts on Stochastic Circuit Simulation to present the most recent developments in the efficient assessment of the impact of "randomness" on the behavior of non-linear circuits. The first presentation deals with randomness due to parametric variations and takes a holistic view of the AMS design cycle to propose a novel statistical framework for minimizing the aggregate simulation/measurement effort needed for pre-silicon validation and post-silicon optimization. The second presentation also deals with parametric variations but takes a SPICE perspective and discusses algorithmic methods for improving the efficiency of circuit uncertainty quantification using generalized polynomial chaos. Finally, the third presentation deals with randomness due to intrinsic noise and fluctuations and looks toward the biological world of proteins, cells, and neurons for fundamental examples as well as for inspiration and guidance on how to deal with the intrinsic randomness problems that arise in the electronic world.

10C.1 Bayesian Model Fusion: A Statistical Framework for Efficient Pre-Silicon Validation and Post-Silicon Tuning of Complex Analog and Mixed-Signal Circuits
Xin Li, Fa Wang, Shupeng Sun - *Carnegie Mellon Univ.*
Chenjie Gu - *Intel Corp.*

10C.2 Uncertainty Quantification for Integrated Circuits: Stochastic Spectral Methods
Zheng Zhang, Luca Daniel - *Massachusetts Institute of Technology*
Ibrahim (Abe) M. Elfadel - *Masdar Institute of Science and Technology*

10C.3 Simulation of Temporal Stochastic Phenomena in Electronic and Biological Systems: A Comparative Review, Examples and Synergies
Alper Demir, Burak Erman - *Koç Univ.*

10D Special Session: **Trustworthy Hardware**
Room: Market 1 & 2

Organizers:
Ramesh Karri - *Polytechnic Institute of New York Univ.*
Farinaz Koushanfar - *Rice Univ.*

The emergence of a globalized, horizontal semiconductor business model raises several concerns involving the security and trust of the information systems on which modern society is increasingly reliant for mission-critical functionality. Hardware security and trust issues span a broad range including threats related to the malicious insertion of Trojan circuits, to intellectual property (IP) and IC piracy, to untrusted third party IPs, IC reverse engineering, and counterfeiting. The first presentation of this session will survey the hardware threats and metrics landscape. The second presentation will present proof carrying code methodology for third party IP protection. The last presentation will present one application of an emerging nanotechnology to security.

10D.1 Hardware Security: Threat Models and Security Metrics
Masoud Rostami, **Farinaz Koushanfar** - *Rice Univ.*
Jeyavijayan Rajendran, Ramesh Karri - *Polytechnic Institute of New York Univ.*

10D.2 A Proof Carrying Based Framework for Trusted Microprocessor IP
Yier Jin - *Univ. of Central Florida*
Yiorgos Makris - *Univ. of Texas at Dallas*

10D.3 A Write-Time Based Memristive PUF for Hardware Security Applications
Garrett S. Rose, Nathan McDonald, Lok-Kwong Yan, Bryant Wysocki - *Air Force Research Lab*

Thursday, November 21

TIME	ALMADEN 1	ALMADEN 2	WINCHESTER
8:00am - 5:00pm	**Workshop 1:** International Workshop on Design Automation for Analog and Mixed-Signal Circuits	**Workshop 2:** IEEE/ACM Workshop on Variability Modeling and Characterization (VMC) 2013	
8:50am - 5:00pm			**Workshop 3:** Eighth International Workshop on Constraints in Formal Verification (CFV), 2013

Registration: 7:00am - 4:00pm - Almaden Foyer **Parking:** $10 per day with in and out privileges

W1 Workshop 1: International Workshop on Design Automation for Analog and Mixed-Signal Circuits

Room: Almaden 1

Organizers:

Xin Li - *Carnegie Mellon Univ.*
Chenjie Gu - *Intel Corp.*
Chandramouli Kashyap - *Intel Corp.*
Jaeha Kim - *Seoul National Univ.*
Trent McConaghy - *Solido Design Automation, Inc.*
Omeed Momeni - *Univ. of California, Davis*

With the aggressive scaling of advanced IC technologies, today's analog and mixed-signal (AMS) circuits have become extremely complex. As circuit designers have adopted a number of non-traditional methodologies (e.g., multi-mode operation, adaptive self-healing, etc.) to address the design challenges associated with technology scaling (e.g., reduced voltage headroom, increased process variation, etc.), the corresponding digital-analog interactions have become increasingly difficult to design and verify. These recent trends of AMS circuits have brought up enormous new challenges and opportunities for AMS CAD. The purpose of this workshop is to report recent advances on AMS CAD and, more importantly, motivate new research topics and directions in this area.

Speakers:

Tim Cheng - *Univ. of California, Santa Barbara*
Frankie Liu - *Oracle Corp.*
Jaijeet Roychowdhury - *Univ. of California, Berkeley*
Martin Vlach - *Mentor Graphics Corp.*
Helmut Graeb - *Technical Univ. of Munich*
Francisco Fernandez - *Univ. of Sevilla*
John Maddux - *Intel Corp.*
Victor Moroz - *Synopsys, Inc.*
Gilles Lamant - *Cadence Design Systems, Inc.*

W2 Workshop 2: IEEE/ACM Workshop on Variability Modeling and Characterization (VMC) 2013

Room: Almaden 2

Organizers:

Hidetoshi Onodera - *Kyoto Univ.*
David Pan - *Univ. of Texas at Austin*
Rasit Topaloglu - *IBM Corp.*

It is widely recognized that process variation is emerging as a fundamental challenge to IC design in scaled CMOS technology; and it will have profound impact on nearly all aspects of circuit performance. While some of the negative effects of variability can be handled with improvements in the manufacturing process, the industry is starting to accept the fact that some of the effects are better mitigated during the design process. Handling variability in the design process will require accurate and appropriate models of variability and its dependence on designable parameters (i.e. layout), and its spatial and temporal distributions. It also requires carefully designed test structures and proper statistical data analysis methods to extract meaningful models from large volumes of silicon measurements. The resulting compact modeling of systematic, random, spatial, and temporal variations is essential to abstract the physical level variations into a format the designers (and more importantly, the tools they use) can utilize. This workshop provides a forum to discuss current practice as well as near future research needs in test structure design, variability characterization, compact variability modeling, and statistical simulation.

Speakers:

Lars Liebmann - *IBM Corp.*
Steve Ramey - *Intel Corp.*
Ahmed Ramadan - *Mentor Graphics Corp.*
Mitiko Miura-Mattausch - *Hiroshima City Univ.*
Keith Jenkins - *IBM Corp.*
Takakshi Sato - *Kyoto Univ.*
Andres Torres - *Mentor Graphics Corp.*

W3 Workshop 3: Eighth International Workshop on Constraints in Formal Verification (CFV), 2013

Room: Winchester

Organizer:

Miroslav Velev - *Aries Design Automation, LLC*

Formal verification is of crucial significance in the development of hardware and software systems. In the last few years, tremendous progress was made in both the speed and capacity of constraint technology. Most notably, SAT solvers have become orders of magnitude faster and capable of handling problems that are orders of magnitude bigger, thus enabling the formal verification of more complex computer systems. As a result, the formal verification of hardware and software has become a promising area for research and industrial applications. The main goals of the Constraints in Formal Verification workshop are to bring together researchers from the CSP/SAT and the formal verification communities, to describe new applications of constraint technology to formal verification, to disseminate new challenging problem instances, and to propose new dedicated algorithms for hard formal verification problems.

This workshop will be of interest to researchers from both academia and industry, working on constraints or on formal verification and interested in the application of constraints to formal verification.

Speakers:

Thomas Ball - *Microsoft Corp.*
Kristin Rozier - *NASA*
Maciej Ciesielski - *Univ. of Massachusetts*
Masahiro Fujita - *Univ. of Tokyo*
Alex Groce - *Oregon State Univ.*
Sumit Jha - *Univ. of Central Florida*
Susmit Jha - *Intel Corp.*
Shobha Vasudevan - *Univ. of Illinois at Urbana-Champaign*
Andreas Veneris - *Univ. of Toronto*
Fei Xie - *Portland State Univ.*

8:50 – 9:00 OPENING REMARKS

9:00 – 10:15 SESSION 1

9:00 – 10:15 **Invited Talk: Efficient Modular SAT Solving for PropertyDirected Reachability**
Thomas Ball, *Microsoft*

10:15 – 10:30 **Coffee Break**

10:30 – 12:00 SESSION 2

10:30 – 11:00 **Towards Certifiable Loop Pipelining Transformations in Behavioral Synthesis**
Disha Puri, Sandip Ray, and Fei Xie *(Portland State Univ.)*

11:00 – 11:30 **Assertion Based Equivalence Between System Level and RTL**
Lingyi Liu, and Shobha Vasudevan *(UIUC)*

11:30 – 12:00 **Formal Verification of Reconfigurable Architectures**
Miroslav Velev, and Ping Gao, *Aries Design Automation*

12:00 – 13:00 **Lunch Break**

13:00 – 15:15 SESSION 3

13:00 – 14:15 **Invited Talk: LTL Satisfiability Checking**
Kristin Rozier, *NASA*

14:15 – 14:45 **Finding Model-Checkable Needles in Large Source Code Haystacks: Modular Bug Finding via Static Analysis and Dynamic Invariant Discovery**
Mohammad Amin Alipour, Alex Groce, Chaoqiang Zhang, Anahita Sanadaji, and Gokul Caushik *(Oregon State Univ.)*

14:45 – 15:00 **Coffee Break**

15:00 – 17:00 SESSION 4

15:00 – 15:30 **Learning Dependency Constraints from System Traces**
Susmit Jha *(Intel)*, Sumit Jha and Emily Sassano *(Univ. of Central Florida)*

15:30 – 16:00 **Automatic Identification of Assertions with Small Number of Test Vectors and Its Applications**
Masahiro Fujita, Satoshi Jo, Takeshi Matsumoto *(Univ. of Tokyo)*

16:00 – 16:30 **Debugging Missing Assumptions in a Formal Verification Environment**
Brian Keng, Andreas Veneris and Djordje Maksimovic *(Univ. of Toronto)*

16:30 – 17:00 **Minimization of Skolem/Herbrand Certificates of Quantified Boolean Formulas**
Valeriy Balabanov, Shuo-Ren Lin, and Jie-Hong R. Jiang *(National Taiwan Univ.)*

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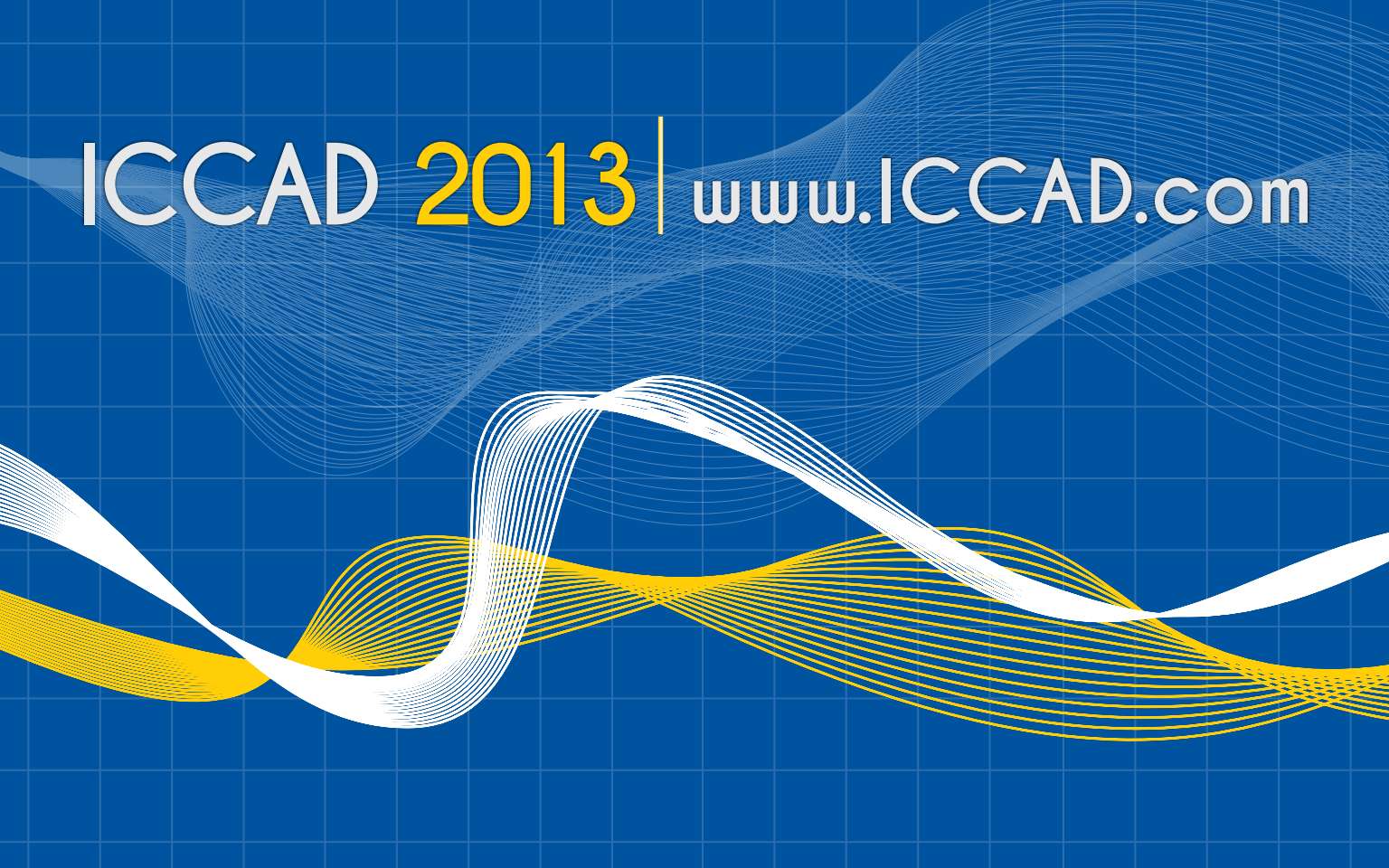
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