ICCAD 30 1982 2012 Celebrating 30 years

IEEE/ACM ICCAD 2012 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

November 5-8, 2012, Hilton San Jose, San Jose, California

FINAL PROGRAM

THE PREMIER CONFERENCE FOR ELECTRONIC DESIGN TECHNOLOGY

Sponsored by: IEEE CEDA IEEE Council on Electronic Design Automation, acm Association for Computing Machinery, sigda

In cooperation with: IEEE, Electron Devices Society, SSCS

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Alan J. Hu
General Chair
Dept. of Computer Science, Univ. of British Columbia

Welcome to ICCAD 2012!

This is a special year for ICCAD; marking the 30th anniversary of the conference. Throughout these 30 years, ICCAD has been, and continues to be, the premier conference devoted entirely to technical innovation in design automation.

The core of ICCAD has always been the technical program of fully refereed research papers. As always, reviewing was double-blind, with strict conflict-of-interest policies to protect the integrity of the process. This year, we reinstated the physical Technical Program Committee meeting, as well as maintaining the full online review-and-deliberation system of the past several years. I believe that this has given us the best of both worlds: the in-depth consideration of an electronic TPC meeting with the face-to-face bandwidth, timeliness, and subtlety of a physical meeting. Out of 338 submissions worldwide, the Technical Program Committee selected a mere 82 papers, for a 24% acceptance rate.

Complementing the refereed program is an entire track of invited sessions: embedded tutorials, special sessions on emerging topics, and designer perspective sessions that highlight needs and gaps in EDA tools. Whatever your interests, we hope you'll find something valuable, useful, and thought-provoking on every day, during every session.

Following the three days of the main conference will be a day of affiliated workshops, providing focused coverage of topics of emerging and current interest. This year, we have expanded the workshop program to five concurrent, full-day workshops -- on design automation for analog and mixed-signal circuits, on domain-specific multicore, on variability modeling and characterization, on multi-synchronous and asynchronous circuits/systems, and on hardware/software techniques for resilience. The rich variety of workshops is becoming a vibrant addition to ICCAD.

Speaking of vibrant, this year, we are trying out a new hotel. ICCAD has always been a wonderful place to reconnect with old friends, colleagues, and contacts, as well as to make new ones. We hope the new space, with many restaurants and activities within easy walking distance, provides all of you with an even better ICCAD experience.

Finally, a 30th anniversary should be a time to reflect on the past, as well as look forward to the future. This year, we have expanded the program to include three keynote presenters, each noted for extraordinary vision and the scope of their contributions.

Kicking off the conference on Monday is John Gustafson, Senior Fellow and Chief Product Architect at AMD. John is a pioneer in parallelism and high-performance computing (e.g., the eponymous Gustafson's Law), and as the characteristics of high-performance computers of yore become commonplace, his insights are indispensable for everyone.

Tuesday, the lunch keynote is by Alberto Sangiovanni-Vincetelli, Edgar L. and Harold H. Buttner Chair of EECS at UC Berkeley. Alberto has long been a pioneer and guiding light in the EDA field, for example co-founding both Cadence and Synopsys, while simultaneously winning a slew of research awards, and also supervising the PhDs of many other luminaries in our field. Alberto's talk will give us a long view of our field.

On Wednesday, we go for breadth, with a keynote by Sebastian Thrun, Research Professor of Computer Science at Stanford, Google Fellow, and co-founder of Udacity. Sebastian built his career in robotics and artificial intelligence, for example, winning the 2005 DARPA Grand Challenge with an autonomous robotic car, and leading the Google Driverless Car project. His keynote talk, however, will be on massive, open, on-line education, where he is also a pioneer. This is a topic that is timely, but with potentially revolutionary ramifications.

We hope you are as excited about these talks as we are!

Here's looking to a great ICCAD in 2012, and the next 30 years of progress and success in our field!

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IEEE/ACM ICCAD 2012 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

Speakers / Presenters

SPEAKERS' BREAKFAST

Room: **Santa Clara 1 & 2**

Please attend the day of your presentation!

Monday, November 5	7:30 - 8:30am
Tuesday, November 6	7:30 - 8:30am
Wednesday, November 7	7:30 - 8:30am

Need Practice

A/V Practice rooms are available to all speakers and presenters

Rooms: **Pacific, Executive Boardroom, and University**

Monday, November 5	7:00am - 6:00pm
Tuesday, November 6	7:00am - 6:00pm
Wednesday, November 7	7:00am - 4:00pm

General Information

CONFERENCE REGISTRATION HOURS

Room: **Almaden Foyer**

Monday, November 5	7:00am – 6:00pm
Tuesday, November 6	7:00am – 6:00pm
Wednesday, November 7	7:00am – 6:00pm
Thursday, November 8	7:30am – 4:00pm

Parking

$10 per day with in and out privileges

Conference Management: MP Associates, Inc.

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Best Paper Candidates/Award Committees

IEEE/ACM William J. McCalla ICCAD Best Paper Candidates:

Monday

1C.1 Layout Small-Angle Rotation and Shift for EUV Defect Mitigation
Hongbo Zhang, *Synopsys Inc.*
Yuelin Du, Martin D.F. Wong, *Univ. of Illinois at Urbana Champaign*
Yunfei Deng, Pawitter Mangat, *GLOBALFOUNDRIES*

2A.4 Probabilistic Design Methodology to Improve Run-time Stability and Performance of STT-RAM Caches
Xiuyuan Bi, Zhenyu Sun, Hai Li, *Polytechnic Institute of New York Univ.*
Wenqing Wu, *Qualcomm, Inc.*

Tuesday

4A.1 Stability Assurance and Design Optimization of Large Power Delivery Networks with Multiple On-Chip Voltage Regulators
Suming Lai, Boyuan Yan, and Peng Li, *Texas A&M Univ.*

6B.1 Fast Transform-Based Preconditioners for Large-Scale Power Grid Analysis on Massively Parallel Architectures
Konstantis Daloukas, Nestor Evmorfopoulos, George Drasidis, Michalis Tsiampas, Panagiota Tsompanopoulou, George I. Stamoulis
Univ. of Thessaly

6C.2 A Fast Time-Domain EM-TCAD Coupled Simulation Framework via Matrix Exponential
Quan Chen, *Univ. of Hong Kong*
Wim Schoenmaker, *Magwel*
Shih-Hung Weng, Chung-Kuan Cheng, *Univ. of California at San Diego*
Guan-Hua Chen, Li-Jun Jiang, and Ngai Wong,
Univ. of Hong Kong

IEEE/ACM William J. McCalla ICCAD Best Paper Award Selection Committee:

Nikil Dutt, *Univ. of California at Irvine*

Tei-Wei Kuo, *National Taiwan Univ.*

Sani Nassif, *IBM Research - Austin*

Sachin Sapatnekar, *Univ. of Minnesota*

Hai Zhou, *Northwestern Univ.*

Ten-Year Retrospective Most Influential Paper Award Selection Committee:

Yao-Wen Chang, *National Taiwan Univ.*

Jason Cong, *Univ. of California, Los Angeles*

Helmut Graeb, *Technische Univ. Muenchen*

Hidetoshi Onodera, *Kyoto Univ.*

CADathlon at ICCAD

SUNDAY, November 4, 8:00am - 5:00pm | Almaden Ballroom

In the spirit of the long-running ACM programming contest, the CADathlon challenges students in their CAD knowledge, and their problem solving, programming, and teamwork skills. It serves as an innovative initiative to assist in the development of top students in the EDA field. The contest will provide a platform for SIGDA, academia, and industry to focus attention on the best and brightest of next generation CAD professionals.

The students will be given a number of problems that range in difficulty and topics. Information about the CAD areas, relevant papers, and potentially a software framework that will run on Linux will be released one week before the competition. Students will be allowed to work in teams of two. At the contest, students will be given the problem statements and an example test data, but they will not have the judges' test data. Solutions will be judged on correctness and efficiency. The team that passes the most testcases is declared the winner. A handsome prize awaits the winning team. The judges are experts in EDA from both academia and industry.

During the competition students will be presented with six problems in the following areas:

- Circuit Design & Analysis
- Physical Design
- Logic & High-Level Synthesis
- System Design & Analysis
- Functional Verification
- Bio-EDA

The competition is open to all graduate students specializing in CAD currently enrolled full-time in a Ph.D. granting institution in any country. Partial or full travel grants will be provided for qualifying students.

For more information, please contact Jarrod Roy at jarrod.a.roy@gmail.com

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IEEE/ACM ICCAD 2012 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

MONDAY, NOVEMBER 5

OPENING SESSION & AWARDS, KEYNOTE ADDRESS - ROOM: ALMADEN 1 & 2

OPENING SESSION & AWARDS
Alan Hu - General Chair, *Dept. of Computer Science,Univ. of British Columbia*
8:30 - 9:00am

KEYNOTE ADDRESS:
Dr. John Gustafson, *Advanced Micro Devices, Inc.*
9:00 - 10:00am

10:30am - 12:00pm

SESSION 1A: Sensing and Harvesting for Energy-Efficient System Design
Room: **Almaden 1**

SESSION 1B: Test Cost and Security
Room: **Almaden 2**

SESSION 1C: DFM for EUV and Multiple Patterning Lithography
Room: **Winchester**

SESSION 1D: EMBEDDED TUTORIAL: Algorithms for Analysis and Optimization of Future Cyber Physical Systems
Room: **Market 1 & 2**

2:00 - 4:00pm

SESSION 2A: Hardware and Software Techniques for for Memory Hierarchy Optimization
Room: **Almaden 1**

SESSION 2B: Simulation-Based Verification
Room: **Almaden 2**

SESSION 2C: Advanced Topics in Routing
Room: **Winchester**

SESSION 2D: SPECIAL SESSION: Computing in the Random Noise: The Bad, the Good, and the Amazing Grace
Room: **Market 1 & 2**

4:30 - 6:00pm

SESSION 3A: Timing and Behavioral Modeling
Room: **Almaden 1**

SESSION 3B: Formal Approaches to Verification
Room: **Almaden 2**

SESSION 3C: Leakage and Technology-Aware Gate Sizing
Room: **Winchester**

SESSION 3D: EMBEDDED TUTORIAL: Dealing with Manufacturing and Reliability in Extremely Scaled CMOS and Beyond
Room: **Market 1 & 2**

LUNCH: 12:00 - 1:45pm: Hyatt Hotel - Grand Hall

Colleague Networking Reception **6:00-6:30pm, Almaden Foyer**

ACM SIGDA Member Meeting:
Time: 8:00pm Room: Santa Clara 1 & 2

PANEL: The Empire Strikes Back or Attack of the Clones? The Once and Future CAD: Time: 6:30pm Room: Almaden 1 & 2

Registration: 7:00am - 6:00pm - Almaden Foyer
Parking: $10 per day with in and out privileges
Speakers Breakfast: 7:30 - 8:30am - Santa Clara 1 & 2
AV practice rooms: 7:00am - 6:00pm - Pacific, Executive Boardroom, and University

Opening Session & Award Presentations

Room: Almaden 1 & 2

Opening Remarks

Alan Hu - General Chair - *Dept. of Computer Science, Univ. of British Columbia*

Award Presentations

IEEE/ACM William J. McCalla ICCAD Best Paper Award

This award is given in memory of William J. McCalla for his contribution to ICCAD and his CAD technical work throughout his career.

4A.1 Stability Assurance and Design Optimization of Large Power Delivery Networks with Multiple On-Chip Voltage Regulators

Suming Lai, Boyuan Yan, and Peng Li, *Texas A&M Univ.*

ICCAD Ten Year Retrospective Most Influential Paper Award

This award is being given to the paper judged to be the most influential on research and industrial practice in computer-aided design of integrated circuits over the ten years since its original appearance at ICCAD.

2002 Paper Titled: Combined Dynamic Voltage Scaling and Adaptive Body Biasing for Lower Power Microprocessors under Dynamic Workloads

Authors: Steven M. Martin, Krisztian Flautner, Trevor Mudge, David Blaauw

Publication: pp. 721-725, ICCAD 2002

IEEE CEDA Early Career Award

For seminal contributions to system-level design, including latency-insensitive design, on-chip communications synthesis, and compositional design-space exploration.

Luca Carloni, *Columbia Univ.*

IEEE CEDA Outstanding Service Contribution

For significant services as ICCAD General Chair 2011.

Joel R. Phillips, *Cadence Design Systems, Inc.*

2012 SIGDA Pioneering Achievement Award

The SIGDA Pioneering Achievement Award recognizes a researcher whose early work has played a pivotal role in the design of electronic systems.

Louise Trevillyan, *IBM T. J. Watson Research Center*

The CADathlon at ICCAD.

Introduction of the 2012 winners.

MONDAY, NOVEMBER 5 - 9:00 - 10:00am

KEYNOTE: The Limits of Parallelism for Simulation

Room: Almaden 1 & 2

Presenter: Dr. John Gustafson - *Advanced Micro Devices, Inc.*

Workstations can now host tens of CPUs and thousands of GPU processing elements, but is this wealth of parallelism limited to just a small fraction of the computing workload of simulation and design? Some have posited that certain tasks are inherently serial and will not benefit from the manycore revolution or from heterogeneous computing using powerful GPUs.

The solution may lie in using dimensions of parallelism that are not obvious and have not been exploited in the past. There are many ways to scale problems besides increasing the size of the data set, and that increase our computing capability within the time we are willing to wait for an answer. A simple but powerful speedup model that includes all overhead costs shows how we can predict the limits of parallelism, and in many cases it predicts that it is possible to apply billions of processors to simulation problems that have traditionally been viewed as "embarrassingly serial."

Dr. John Gustafson is Senior Fellow at AMD, where he serves as Chief Product Architect for Graphics. He is a 35-year veteran of the computing industry, and comes to AMD from Intel, where he directed the company's eXtreme Technologies Lab. Prior to that, he served as CEO at Massively Parallel Technologies, and CTO at ClearSpeed Technology, a high-performance computing company. John has also held key management and research positions at numerous companies including Sun Microsystems, Ames Laboratory, and Sandia Laboratories. John holds an M.S. and Ph.D. in applied mathematics from Iowa State University, and a B.S. in the same from Caltech. He holds numerous patents and has authored an extensive array of technical publications.

All speakers are denoted in bold | * - denotes best paper candidate

1A Sensing and Harvesting for Energy-Efficient System Design
Room: Almaden 1

Moderator:

Hidetoshi Onodera - *Kyoto Univ.*

The papers in this session explore two important facets of energy-efficient system design - harvesting energy from solar power, and the use of inward-facing sensors that monitor process variations and temperature. The first paper addresses an increasingly common energy source - solar energy, and proposes a reconfigurable architecture and algorithms for online fault detection and recovery. The second paper presents a tunable process variation sensor, and the third paper proposes calibration techniques for accurate thermal sensing.

1A.1 Online Fault Detection and Tolerance for Photovoltaic Energy Harvesting Systems

Xue Lin, Yanzhi Wang, Di Zhu, Massoud Pedram - *Univ. of Southern California*

Naehyuck Chang - *Seoul National Univ.*

1A.2 Tunable Sensors for Process-Aware Voltage Scaling

Tuck-Boon Chan, Andrew B. Kahng - *Univ. of California at San Diego*

1A.3 Collaborative Calibration of On-Chip Thermal Sensors Using Performance Counters

Shiting (Justin) Lu, Russell Tessier, Wayne Burleson - *Univ. of Massachusetts, Amherst*

1B Test Cost and Security
Room: Almaden 2

Moderator:

Prashant Goteti - *Intel Corp.*

This session addresses important issues in test cost and hardware security. It addresses these issues through novel modeling, new ATPG, and intelligent use of hardware monitoring techniques.

1B.1 Spatial Correlation Modeling For Probe Test Cost Reduction in RF Devices

Nathan Kupp - *Yale Univ.*

Ke Huang, Yiorgos Makris - *Univ. of Texas at Dallas*

John M. Carulli - *Texas Instruments, Inc.*

1B.2 Small-Delay-Fault ATPG with Waveform Accuracy

Matthias Sauer, Alexander Czutro, Bernd Becker - *Univ. of Freiburg*

Ilia Polian - *Univ. of Passau*

1B.3 Experimental Analysis of a Ring Oscillator Network for Hardware Trojan Detection in a 90nm ASIC

Xuehui Zhang, Andrew Ferraiuolo, Mohammad Tehranipoor - *Univ. of Connecticut*

1C DFM for EUV and Multiple Patterning Lithography
Room: Winchester

Moderator:

Duo Ding - *Oracle Corp.*

Emerging lithography for nanoscale patterning in 14nm and beyond calls for new techniques in design and process integration. This session consists of three interesting papers dealing with design for manufacturability (DFM) in extreme ultra-violet (EUV) and multiple-patterning lithography. The first paper proposes a novel small-angle rotation and shift technique to mitigate EUV defects. The second paper applies probablistic wiring estimation and machine learning to explore design rules for double/multiple patterning. The third paper presents a row-based polynominal time algorithm for triple patterning layout decomposition.

1C.1* Layout Small-Angle Rotation and Shift for EUV Defect Mitigation
Hongbo Zhang - *Synopsys, Inc.*
Yuelin Du, Martin D. F. Wong - *Univ. of Illinois at Urbana-Champaign*
Yunfei Deng, Pawitter Mangat - *GLOBALFOUNDRIES*

1C.2 A Methodology for the Early Exploration of Design Rules for Multiple-Patterning Technologies
Rani S. Ghaida, Tanaya Sahu, Puneet Gupta - *Univ. of California, Los Angeles*
Parag Kulkarni - *Qualcomm, Inc.*

1C.3 A Polynomial Time Triple Patterning Algorithm for Cell Based Row-Structure Layout
Haitong Tian, Zigang Xiao, Martin D. F. Wong - *Univ. of Illinois at Urbana-Champaign*
Hongbo Zhang, Qiang Ma - *Synopsys, Inc.*

1D Embedded Tutorial: Algorithms for Analysis and Optimization of Future Cyber Physical Systems
Room: Market 1 & 2

Organizer:

Radu Marculescu - *Carnegie Mellon Univ.*

We live in a world where computation, communication, and controls are increasingly interwoven to produce functionally rich and energy efficient Cyber-Physical Systems (CPS). What distinguishes CPS from traditional embedded control systems is that the plants, such as the human body, are typically ill-defined, interactive and non-deterministic in nature. Furthermore, these systems often involve life-critical and safety-critical applications where the operation and performance must be formally and functionally verified as a closed-loop system - from abstract models all the way down to the generated code. Consequently, the basic algorithms for CPS design and runtime operation should include time and feedback-based control as intrinsic components of the programming model.

In this tutorial, we plan to introduce the CPS from three perspectives of nano, meso and macro systems across the domains of implantable medical devices, energy-efficient building scheduling and control automation, and large-scale transportation systems involving millions of vehicles. With this multi-scale approach we plan to use a thread of running examples to support the fundamental challenges CPS bring in robust and adaptive algorithms, closed-loop verification and testing approaches, runtime monitoring and platform development. We aim to balance the breadth of the applicability of CPS with a focus on the above three application domains.

Presenters:

Radu Marculescu - *Carnegie Mellon Univ.*
Rahul Mangharam - *Univ. of Pennsylvania*

All speakers are denoted in bold | * - denotes best paper candidate

2A Hardware and Software Techniques for Memory Hierarchy Optimization
Room: Almaden 1

Moderator:

Sri Parameswaran - *Univ. of New South Wales*

The papers in this session propose hardware and software techniques for improving performance and energy of the memory hierarchy subsystem. The first paper presents a combination of loop and data locality transformations targeting the last level cache. The second paper proposes synthesizing an asymmetric DRAM structure in response to varying application requirements. The third paper proposes and evaluates a hybrid GPU memory targeting high bandwidth and low power. The final paper adapts the write pulse period to reduce failure rates.

2A.1 Improving Last Level Cache Locality by Integrating Loop and Data Transformations

Wei Ding, Mahmut Kandemir - *Pennsylvania State Univ.*

2A.2 Asymmetric DRAM Synthesis for Heterogeneous Chip Multiprocessors in 3-D-Stacked Architecture

Minje Jun, Myoung-Jin Kim, Eui-Young Chung - *Yonsei Univ.*

2A.3 Optimizing Bandwidth and Power of Graphics Memory with Hybrid Memory Technologies and Adaptive Data Migration

Jishen Zhao - *Pennsylvania State Univ.*

Yuan Xie - *Pennsylvania State Univ., Advanced Micro Devices, Inc.*

2A.4* Probabilistic Design Methodology to Improve Run-Time Stability and Performance of STT-RAM Caches

Xiuyuan Bi, Zhenyu Sun, Hai Li - *Polytechnic Institute of New York Univ.*

Wenqing Wu - *Qualcomm, Inc.*

2B Simulation-Based Verification
Room: Almaden 2

Moderator:

Bryan Brady - *IBM Corp.*

This session brings together advances along different axes in simulation and emulation based verification. In the first paper, efficient protocol detectors are inserted on chip to pin point design errors in complex SoCs. The next two papers improve the quality of test vectors using coverage based novel-test detection, and by range based pruning of constrained random simulation, resulting in 20x faster speed. The last paper presents a system for co-simulation with emulation and on-demand sub-circuit simulation.

2B.1 Bridging Pre- and Post-Silicon Debugging with BiPeD

Andrew DeOrio, Jialin Li, Valeria Bertacco - *Univ. of Michigan*

2B.2 Novel Test Detection to Improve Simulation Efficiency - A Commercial Experiment

Wen Chen, Nik Sumikawa, Li-C Wang - *Univ. of California, Santa Barbara*

Jayanta Bhadra, Xiushan Feng, Magdy S. Abadir - *Freescale Semiconductor, Inc.*

2B.3 A Robust General Constrained Random Pattern Generator for Constraints with Variable Ordering

Bo-Han Wu, Chung-Yang (Ric) Huang - *National Taiwan Univ.*

2B.4 Fast and Scalable Hybrid Functional Verification and Debug with Dynamically Reconfigurable Co-Simulation

Somnath Banerjee, Tushar Gupta - *Mentor Graphics Pvt. Ltd., India*

2C Advanced Topics in Routing
Room: Winchester

Moderators:

Aiqun Cao - *Synopsys, Inc.*
Inki Hong - *Cadence Design Systems, Inc.*

The routing problems addressed in this session span the spectrum of EDA interests: At the chip level, two of the papers deal with the realistic and relevant problem of routing over blocks while placing buffers between them. At the analog level, one paper addresses the problem of precisely matching critical routes. And at the technology level, one paper addresses the problem of next generation triple layer lithography.

2C.1 TRIAD: A Triple Patterning Lithography Aware Detailed Router
Yen-Hung Lin, Yih-Lang Li - *National Chiao Tung Univ.*
Bei Yu, David Z. Pan - *Univ. of Texas at Austin*

2C.2 Maze Routing Algorithms with Exact Matching Constraints for Analog and Mixed Signal Designs
Renato Fernandes Hentschke, Muhammet Mustafa Ozdal - *Intel Corp.*

2C.3 Reclaiming Over-the-IP-Block Routing Resources with Buffering-Aware Rectilinear Steiner Minimum Tree Construction
Yilin Zhang, David Z. Pan - *Univ. of Texas at Austin*
Ashutosh Chakraborty, Salim Chowdhury - *Oracle Corp.*

2C.4 Construction of Rectilinear Steiner Minimum Trees with Slew Constraints over Obstacles
Tao Huang, Evangeline F. Y. Young - *The Chinese Univ. of Hong Kong*

2D Special Session: Computing in the Random Noise: The Bad, the Good, and the Amazing Grace
Room: Market 1 & 2

Moderator:

Amit Singhee - *IBM T.J. Watson Research Center*

Organizer:

Yiyu Shi - *Missouri Univ. of Science and Technology*

In the past decade, circuit designers have been fighting with electrical and thermal noise for signal and power integrity (SI, PI). However, with the aggressive technology scaling in the deep sub-micron paradigm, noise margin keeps decreasing and larger area/performance penalty has to be paid to sustain SI and PI. This enforces us to rethink our practice: instead of suppressing the noise, can we change our design philosophy and make use of the noise to enhance the designs? This special session consists of four invited talks giving introductions and discussions on a variety of noise-based design methodologies from different aspects.

2D.1 Noise Based Logic: Why Noise?
Laszlo B. Kish - *Texas A&M Univ.*
He Wen - *Texas A&M Univ., Hunan Univ.*

2D.2 An Efficient Implementation of Numerical Integration Using Logical Computation on Stochastic Bit Streams
Weikang Qian, Chen Wang - *Shanghai Jiao Tong Univ.*
Peng Li, Kia Bazargan, David Lilja, Marc Riedel - *Univ. of Minnesota*

2D.3 Utilizing Random Noise in Cryptography: Where is the Tofu?
Yiyu Shi, Hui Geng, Jun Wu, Minsu Choi, Jianming Liu - *Missouri Univ. of Science and Technology*

2D.4 Learning from Biological Neurons to Compute with Electronic Noise
Hsin Chen, Chih-Chen Lu, Yi-Da Wu - *National Tsing Hua Univ.*
Tang-Jung Chiu - *Taiwan Semiconductor Manufacturing Co., Ltd.*

All speakers are denoted in bold | * - denotes best paper candidate

3A Timing and Behavioral Modeling
Room: Almaden 1

Moderators:

Chenjie Gu - *Intel Corp.*

Igor Keller - *Cadence Design Systems, Inc.*

In this session, we have an excellent set of papers presenting both theoretical and practical advances in timing analysis and behavioral modeling. The first paper presents interesting proofs for criticality computation in SSTA and a practical approach for speeding it up. The authors of the second paper present an optimal sampling methodology for mismatch characterization of standard cells for SSTA. The last paper presents the application of machine learning to the problem of classifying performance of circuits such as PLLs and SRAM.

3A.1 On the Computation of Criticality in Statistical Timing Analysis

S. Ramprasath, V. Vasudevan - *Indian Institute of Technology, Madras*

3A.2 A Dynamic Method for Efficient Random Mismatch Characterization of Standard Cells

Amith Singhee, Jinjun Xiong - *IBM T.J. Watson Research Center*

Wangyang Zhang, Peter Habitz, Amol Joshi, Chandu Visweswariah, James Sundquist - *IBM Systems and Technology Group*

3A.3 Classifying Circuit Performance Using Active-Learning Guided Support Vector Machines

Honghuang Lin, Peng Li - *Texas A&M Univ.*

3B Formal Approaches to Verification
Room: Almaden 2

Moderator:

Pankaj Chauhan - *Calypto Design Systems, Inc.*

This session presents a collection of papers that demonstrate wide applicability of formal methods. The first paper describes formal analysis to exploit signal correlations to improve circuit imulation. The second paper presents flow-directed discretization of the analog circuit state-space for verification. The last paper lifts assertion mining from bit-level to word-level for RTL verification.

3B.1 Scalable Sampling Methodology for Logic Simulation: Reduced-Ordered Monte Carlo

Armin Alaghi, Chien-Chih Yu, John P. Hayes - *Univ. of Michigan*

3B.2 Trajectory-Directed Discrete State Space Modeling for Formal Verification of Nonlinear Analog Circuits

Sebastian Steinhorst - *TUM CREATE Ltd.*

Lars Hedrich - *Univ. of Frankfurt*

3B.3 Word Level Feature Discovery to Enhance Quality of Assertion Mining

Shobha Vasudevan, Lingyi Liu, Chen-Hsuan Lin - *Univ. of Illinois at Urbana-Champaign*

3C Leakage and Technology-Aware Gate Sizing
Room: Winchester

Moderators:

Cheng Zhuo - *Intel Corp.*

Jianchao Lu - *Synopsys, Inc.*

This session examines the long-standing problem of gate sizing during physical design. The first paper examines the needs of future technology libraries and how this affects design optimality. The second two papers were entries in the 2012 ISPD Gate Sizing Contest and present multi-threaded gate-sizing algorithms that are evaluated using an industrial methodology.

3C.1 Impact of Range and Precision in Technology on Cell-Based Design

John Lee, Puneet Gupta - *Univ. of California, Los Angeles*

3C.2 An Efficient Algorithm for Library-Based Cell-Type Selection in High-Performance Low-Power Designs

Li Li, Peng Kang, Hai Zhou - *Northwestern Univ.*

Yinghai Lu - *Synopsys, Inc.*

3C.3 Sensitivity-Guided Metaheuristics for Accurate Discrete Gate Sizing

Seokhyeong Kang, Andrew B. Kahng - *Univ. of California at San Diego*

Jin Hu, Myung-Chul Kim, Igor L. Markov - *Univ. of Michigan*

3D Embedded Tutorial: Dealing with Manufacturing and Reliability in Extremely Scaled CMOS and Beyond
Room: Market 1 & 2

Moderators:

David Z. Pan - *Univ. of Texas at Austin*

Sachin Sapatnekar - *Univ. of Minnesota*

Organizers:

David Z. Pan - *Univ. of Texas at Austin*

Sachin Sapatnekar - *Univ. of Minnesota*

As the CMOS feature enters the era of extreme scaling (14nm, 11nm and beyond), many manufacturability and reliability issues are exacerbated. On one hand, the patterning through the 193nm lithography is pushed to the extreme, through double/triple or more general multiple patterning, while non-conventional lithography technologies such as EUV, e-beam direct-write (EBDW), and directed self-assembly (DSA) still have grand challenges to be solved for their adoption into IC volume production. On the other hand, the list of reliability concerns keeps growing along with the feature size miniaturization, including bias temperature instability (BTI), gate oxide breakdown, hot carrier injection, electromigration, and thermomechanical stress. This tutorial will provide a broad yet in-depth overview of how to deal with the aforementioned manufacturability and reliability issues. Both analysis/modeling issues and optimization techniques will be presented. The topics include but not limited to: (1) double/multiple patterning lithography analysis, layout decomposition, and physical design; (2) CAD challenges and potential solutions for emerging lithography; (3) analysis and modeling of major reliability issues, their impact on logic and memory, and interactions between variations and aging; (4) pre-silicon and post-silicon optimizations for reliability enhancement.

3D.1 Dealing with IC Manufacturability in Extreme Scaling

David Z. Pan, Bei Yu, Jhih-Rong Gao, Duo Ding, Yongchan Ban, Jae-seok Yang, Kun Yuan, Minsik Cho - *Univ. of Texas at Austin*

3D.2 Circuit Reliability: From Physics to Architectures

Sachin S. Sapatnekar, Jianxin Fang, Saket Gupta, Sanjay V. Kumar, Sravan K. Marella, Vivek Mishra, Pingqiang Zhou - *Univ. of Minnesota*

All speakers are denoted in bold | * - denotes best paper candidate

PANEL

The Empire Strikes Back or Attack of the Clones? The Once and Future CAD

Time: 6:30 - 7:45pm
Room: Almaden 1 & 2

Moderator:

William Joyner - *Semiconductor Research Corporation*

Organizers:

Diana Marculescu - *Carnegie Mellon Univ.*
Yao-Wen Chang - *National Taiwan Univ.*

Thirty years is a long time for any conference to exist, and it is a tribute to ICCAD and to the field that this work is still going strong. But where is it going, and for how long? Areas which have been declared dead have become vital again, and new challenges arise with decreases in feature size, increases in system complexity, and new applications. Are we seeing more, smaller, incremental improvements being advanced by a clone army, or are there major imperial breakthroughs that yet await? Is the proliferation of smaller conferences a good thing, or does it threaten the established venues? Will smaller start-ups flourish, or will the "Big N" dominate? The panelists will both reminisce about the ICCAD and CAD experiences of the past and prognosticate about the future.

Panelists:

Valeria Bertacco - *Univ. of Michigan*
Luca Carloni - *Columbia Univ.*
Andreas Kuehlmann - *Coverity, Inc.*
Hidetoshi Onodera - *Kyoto Univ.*
Louis Scheffer - *Howard Hughes Medical Institute*
Donatella Sciuto - *Politecnico di Milano*

ACM/SIGDA Member Meeting

The Resource for EDA Professionals

Time: 8:00 - 9:30pm
Room: Santa Clara 1 & 2

The annual ACM/SIGDA Member Meeting is open to all members of the EDA community. *(Limited Seating)*

Presentation of Pioneer Award
Hear a few words from Louise Trevillyan as she speaks about her experiences in EDA.

Everyone is invited to join the meeting for a light dinner, refreshments, and an entertaining and interesting presentation.

Plus...
Meet the newly elected SIGDA Executive Committee.

By the way, why don't you join SIGDA?

IEEE/ACM ICCAD 2012 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

TUESDAY, NOVEMBER 6

8:30 - 10:00am

SESSION 4A: System-Level Modeling and Optimization of Power Ground Networks
Room: **Almaden 1**

SESSION 4B: DESIGNER TRACK:
Challenges in 3-D IC Technologies and Integration
Room: **Almaden 2**

SESSION 4C:
SPECIAL SESSION:
Placement for the Next Decade
Room: **Winchester**

SESSION 4D:
SPECIAL SESSION:
Automation of Biological System Modeling and Analysis
Room: **Market 1 & 2**

10:30am - 12:00pm

SESSION 5A: Power-Aware Architecture and System Design
Room: **Almaden 1**

SESSION 5B: Reliability and Thermal Issues in 3-D ICs
Room: **Almaden 2**

SESSION 5C: CAD Contest
Room: **Winchester**

SESSION 5D:
SPECIAL SESSION:
Power Characterization and Optimization in Smartphones
Room: **Market 1 & 2**

2:00 - 4:00pm

SESSION 6A: Computational Approaches for Biological Systems
Room: **Almaden 1**

SESSION 6B: Fast Parallel Power Ground Network Simulation Methods
Room: **Almaden 2**

SESSION 6C: Efficient Verification and Yield Estimation for Analog Circuits
Room: **Winchester**

SESSION 6D:
SPECIAL SESSION:
Toward Co-Design in High-Performance Computing Systems
Room: **Market 1 & 2**

4:30 - 6:00pm

7A SESSION: System-Level Modeling and Optimization
Room: **Almaden 1**

7B SESSION: High-Level Design Methods
Room: **Almaden 2**

SESSION 7C:
SPECIAL SESSION: The Next Wave: Top Challenges in Electromagnetic-Based Design Automation
Room: **Winchester**

SESSION 7D:
EMBEDDED TUTORIAL:
Printable Electronics
Room: **Market 1 & 2**

INVITED LUNCHEON TALK: ICCAD at Thirty Years: Where We Have Been, Where We Are Going
Alberto Sangiovanni-Vincentelli, *University of Califoria, Berkeley.* **Time: 12:00 - 1:45pm, Hyatt Hotel - Grand Hall**

Colleague Networking Reception **6:00-6:30pm, Almaden Foyer**

Registration: 7:00am - 6:00pm - Almaden Foyer
Parking: $10 per day with in and out privileges
Speakers Breakfast: 7:30 - 8:30am - Santa Clara 1 & 2
AV practice rooms: 7:00am - 6:00pm - Pacific, Executive Boardroom, and University

All speakers are denoted in bold | * - denotes best paper candidate

4A System-Level Modeling and Optimization of Power Ground Networks
Room: Almaden 1

Moderators:

Yiyu Shi - *Missouri Univ. of Science and Technology*

Don MacMillen - *Nimbic, Inc.*

This session presents system level simulation, modeling and optimization techniques towards the design of advanced power ground networks. The first paper discusses a method to characterize the stability of power distribution systems with multiple voltage regulators. The next paper presents a system-level power ground modeling methodology with model-to-hardware correlation. The last paper develops models for DC-DC converters as a function of size and layout and proposes an optimization technique for best efficiency.

4A.1* Stability Assurance and Design Optimization of Large Power Delivery Networks with Multiple On-Chip Voltage Regulators

Suming Lai, Boyuan Yan, Peng Li - *Texas A&M Univ.*

4A.2 A Silicon-Validated Methodology for Power Delivery Modeling and Simulation

Cheng Zhuo, Gustavo Wilke, Ritochit Chakraborty, Alaeddin Aydiner, Sourav Chakravarty, Wei-Kai Shih - *Intel Corp.*

4A.3 Optimization of On-Chip Switched-Capacitor DC-DC Converters for High-Performance Applications

Pingqiang Zhou, Won Ho Choi, Bongjin Kim, Chris H. Kim, Sachin S. Sapatnekar - *Univ. of Minnesota*

4B Designer Track: Challenges in 3-D IC Technologies and Integration
Room: Almaden 2

Moderator:

David Z. Pan - *Univ. of Texas at Austin*

Organizer:

Yao-Wen Chang - *National Taiwan Univ.*

Three-dimensional (3-D) IC integration has been proven to be able to offer significant advantages for heterogeneous integration, higher performance, better form factors, etc. This session invites experts from three key companies to address recent technology trends and new challenges in 3-D IC design, including promising 3-D integration techniques, architecture considerations, packaging technologies, simulation/modeling requirements, physical implementation issues, power delivery and thermal management, advanced test methodologies, and so on.

4B.1 Scaling the "Memory Wall"

Shih-Lien Lu, Tanay Karnik, Ganapati Srinivasa, Kai-Yuan Chao, Doug Carmean, Jim Held - *Intel Corp.*

4B.2 Test Challenges in Designing Complex 3-D Chips: What is on the Horizon for the EDA Industry?

Sandeep Kumar Goel - *Taiwan Semiconductor Manufacturing Co., Ltd.*

4B.3 3-D Integrated Circuits: Designing in a New Dimension

Robert Patti - *Tezzaron Semiconductor*

4C Special Session: Placement for the Next Decade
Room: Winchester

Moderator:

Patrick Groeneveld - *Synopsys, Inc.*

Organizer:

Charles Alpert - *IBM Corp.*

Design automation algorithms for standard cell placement have been around for several decades; and placement has historically been considered a core problem in EDA. Perhaps due to its relatively straightforward formulation and longevity, there is a fairly widespread perception that placement is no longer a particularly interesting area of research, i.e., it is not a "hot topic." However, nothing could be further from the truth: placement is at the heart of design quality in terms of timing closure, routability, area, power and, most importantly, time-to-market. The speakers in this session will describe new opportunities for research in placement for the next ten years and make the case that more investment in this fundamental technology would significantly benefit the design community.

4C.1 Progress and Challenges in VLSI Placement Research

Igor L. Markov, Jin Hu, Myung-Chul Kim - *Univ. of Michigan*

4C.2 The Upcoming Golden Age of Placement Research

Shankar Krishnamoorthy - *Mentor Graphics Corp.*

4C.3 Placement: Hot or Not?

Charles J. Alpert, Zhuo Li, Gi-Joon Nam, C.N. Sze, Natarajan Viswanathan, Samuel Ward - *IBM Corp.*

4D Special Session: Automation of Biological System Modeling and Analysis
Room: Market 1 & 2

Moderator:

Subarna Sinha - *Stanford Univ.*

Organizer:

Natasa Miskov-Zivanov - *Univ. of Pittsburgh*

Biological systems are astoundingly complex and it is often hard to comprehend all their details. Despite their complexity, there has been an unceasing attempt to understand and control them. It has been shown that the evolution has driven towards recurrent molecular "designs" and circuit motifs, thus establishing principles of organization, architecture, and (evolutionary) design in biological circuits. However, there are many details and deep principles yet to be discovered. At the same time, in electronic circuit design, circuits are designed by selecting and combining well understood electronic components for the purpose of implementing the desired functionality. Electronic design automation (EDA) allows for the efficiency of this process by abstracting away details and using higher level building blocks to describe computational systems. These systems are modular, hierarchically organized, and their behavior is controllable and predictable. This session is a step towards answering the following questions: (i) Why not study complex biological systems, design and control them in the same manner as electronic circuits? (ii) Is the complexity of systems that engineers are designing comparable to the complexity of biological systems? The session will address challenges in studying biological systems, and will present existing methods for automation of model development and analysis for these systems.

4D.1 Modeling and Design Automation of Biological Circuits and Systems

James R. Faeder, Natasa Miskov-Zivanov - *Univ. of Pittsburgh*

Herbert M. Sauro - *Univ. of Washington*

Chris J. Myers - *Univ. of Utah*

All speakers are denoted in bold | * - denotes best paper candidate

5A Power-Aware Architecture and System Design
Room: Almaden 1

Moderator:

Youngsoo Shin - *KAIST*

The papers in this session address various aspects of power-aware architecture. The first paper presents a variant of the popular tool CACTI that models off-chip memory interfaces. The second paper proposes a hardware/software approach to power-gate the registers in the register files of general-purpose processors. The last paper proposes a technique to efficiently implement state retention for power-gated logic circuits.

5A.1 CACTI-IO: CACTI with Off-Chip Power-Area-Timing Models

Vaishnav Srinivas, Andrew B. Kahng - *Univ. of California at San Diego*

Norman P. Jouppi, Naveen Muralimanohar - *Hewlett-Packard Co.*

5A.2 AFReP: Application-Guided Function-Level Registerfile Power-Gating for Embedded Processors

Hamed Tabkhi, Gunar Schirner - *Northeastern Univ.*

5A.3 Efficient Multiple-Bit Retention Register Assignment for Power Gated Design: Concept and Algorithms

Yu-Guang Chen, Kuan-Yu Lai, Shih-Chieh Chang - *National Tsing-Hua Univ.*

Yiyu Shi, Geng Hui - *Missouri Univ. of Science and Technology*

5B Reliability and Thermal Issues in 3-D ICs
Room: Almaden 2

Moderator:

Miroslav Velev - *Aries Design Automation, LLC*

This session consists of papers addressing reliabiliy and thermal issues in emerging 3-D integrated circuits. The first paper proposes a holistic analysis of timing variations that caused by thermal and TSV-stress. The second paper models the electromigration effects with stress-aware modeling and proposes a routing algorithm to migitate such effects. The last paper proposes a fast transient thermal simulation of 3-D ICs.

5B.1 A Holistic Analysis of Circuit Timing Variations in 3-D-ICs with Thermal and TSV-Induced Stress Considerations

Sravan K. Marella, Sanjay V. Kumar, Sachin S. Sapatnekar - *Univ. of Minnesota*

5B.2 Electromigration-Aware Routing for 3-D ICs with Stress-Aware EM Modeling

Jiwoo Pak, David Z. Pan - *Univ. of Texas at Austin*

Sung Kyu Lim - *Georgia Institute of Technology*

5B.3 3-D Transient Thermal Solver using Non-Conformal Domain Decomposition Approach

Jianyong Xie, Madhavan Swaminathan - *Georgia Institute of Technology*

5C CAD Contest
Room: Winchester

Moderators:

Zhuo Li - *IBM Research - Austin*
Iris Hui-Ru Jiang - *National Chiao Tung Univ.*

Organizers:

Yih-Lang Li - *National Chiao Tung Univ.*
Iris Hui-Ru Jiang - *National Chiao Tung Univ.*
Yao-Wen Chang - *National Taiwan Univ.*

Contests and their benchmarks have become an important driving force to push our EDA domain forward in different areas lately. Continuing its great success during the past 12 years, the annual CAD Contest in Taiwan, originally sponsored by the Ministry of Education (MOE), is now with the technical sponsorship from IEEE CEDA and open worldwide to have more significant contributions to our global EDA community. Three contest problems on functional ECO, placement, and litho hotspot identification are announced this year. This session presents the three contest problems, releases their benchmarks, and announces the contest results. This session also provides a forum for top final teams to disclose their key ideas and algorithms through video presentations.

5C.1 Opening: Introduction to CAD Contest at ICCAD 2012
Zhuo Li - *IBM Corp.*
Yih-Lang Li, Iris Hui-Ru Jiang - *National Chiao Tung Univ.*

5C.2 ICCAD-2012 CAD Contest in Finding the Minimal Logic Difference for Functional ECO and Benchmark Suite
Hwei-Tseng Wang, WoeiTzy Wells Jong, Chengta Hsieh, Kei-Yong Khoo - *Cadence Design Systems, Inc.*

5C.3 ICCAD-2012 CAD Contest in Design Hierarchy Aware Routability-Driven Placement and Benchmark Suite
Natarajan Viswanathan, Charles J. Alpert, Cliff Sze, Zhuo Li, Yaoguang Wei - *IBM Corp.*

5C.4 ICCAD-2012 CAD Contest in Fuzzy Pattern Matching for Physical Verification and Benchmark Suite
J. Andres Torres - *Mentor Graphics Corp.*

5D Special Session: Power Characterization and Optimization in Smartphones
Room: Market 1 & 2

Moderator:

Massoud Pedram - *Univ. of Southern California*

Organizer:

Massoud Pedram - *Univ. of Southern California*

This session focuses on power modeling, estimation, optimization and management in battery-powered and thermally constrained mobile systems, e.g., smart phones. Presenters will cover topics ranging from per-process energy consumption accounting to remaining battery life estimation to system-level power management.

5D.1 System Energy Consumption is a Multi-Player Game
Lin Zhong, Mian Dong - *Rice Univ.*
Tian Lan - *George Washington Univ.*

5D.2 Power Estimation and Modeling Challenges for Mobile Devices
Mohamed Allam - *Qualcomm, Inc.*

5D.3 Thermal Management on Smart-Phones: A Case Study
John Redmond, Ajat Hukkoo, Hwisung Jung - *Broadcom Corp.*

All speakers are denoted in bold | * - denotes best paper candidate

ICCAD at Thirty Years: Where We Have Been, Where We Are Going

Hyatt Place - Grand Hall

Organizer:

Joel Phillips - *Cadence Design Systems, Inc.*

In celebration of ICCAD's 30th anniversary year, the Distinguished Lecture Series of the IEEE Council on Electronic Design Automation is pleased to feature Professor Alberto Sangiovanni-Vincentelli of the Univ. of California, Berkeley, speaking on the past and future evolution of computed-aided integrated circuit design.

Alberto Sangiovanni-Vincentelli holds the Buttner Chair of EECS, Univ. of California, Berkeley. He co-founded Cadence and Synopsys, the two largest EDA public companies. He is a member of the Board of Directors of Cadence, Sonics, ExpertSystems, KPIT Cummins and Accent, of the Science and Technology Advisory Board of GM, of the Technology Advisory Council of UTC, and of the Executive Committee of the Italian Institute of Technology. He is on the advisory board of Walden International Xseed and Innogest Venture Capital Funds and on the investment committee of Banca Intesa Fondo Atlante and of Finlombarda Next Venture Capital Fund. He is a member of the Scientific Council of the Italian National Science Foundation and President of the Group of 7 Research Supervisors of the Italian Government. He received the Kaufman Award for "pioneering contributions to EDA" and the IEEE/RSE Maxwell Medal "for groundbreaking contributions that have had an exceptional impact on the development of electronics and electrical engineering or related fields". He is an author of over 880 papers, 17 books and 3 patents. He is a Fellow of the IEEE and a Member of the National Academy of Engineering.

Sponsored by:

IEEE CEDA IEEE Council on Electronic Design Automation

TUESDAY, NOVEMBER 6 - 2:00 - 4:00pm

6A Computational Approaches for Biological Systems
Room: Almaden 1

Moderators:

Phillip Brisk - *Univ. of California, Riverside*
Saurabh Srivastava - *Univ. of California, Berkeley*

This session presents recent advances in designing and analyzing biological systems. Microfluidic approaches investigate how devices can be designed to be voltage aware, recover from errors quickly and effiicently, and how to minimize the reactants used in the system. A biochemical reaction based formalism is examined to transform control flows into robust molecular reactions.

6A.1 Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWOD Chips
Sheng-Han Yeh, Jia-Wen Chang, Tsung-Wei Huang, Tsung-Yi Ho - *National Cheng Kung Univ.*

6A.2 Compiling Program Control Flows into Biochemical Reactions
Ruei-Yang Huang, De-An Huang, Jie-Hong R. Jiang, Chi-Yun Cheng - *National Taiwan Univ.*

6A.3 Dictionary-Based Error Recovery in Cyberphysical Digital-Microfluidic Biochips
Yan Luo, Krishnendu Chakrabarty - *Duke Univ.*
Tsung-Yi Ho - *National Cheng Kung Univ.*

6A.4 Reactant Minimization during Sample Preparation on Digital Microfluidic Biochips using Skewed Mixing Trees
Chia-Hung Liu, Juinn-Dar Huang, Ting-Wei Chiang - *National Chiao Tung Univ.*

6B Fast Parallel Power Ground Network Simulation Methods
Room: Almaden 2

Moderators:

Wil Schilders - *Technische Univ. Eindhoven*
Amitava Bhaduri - *Intel Corp.*

This session presents advances in fast power ground network simulation techniques, especially tailored to massively parallel computing architectures. The first paper discusses an iterative solution for power grid analysis, with a preconditioner that is based upon a fast transform and is amenable to parallelization. The next paper presents a structured random walk method for constructing the power grid preconditioner. The third paper discusses a parallel implementation of the additive Schwartz method and solves a problem size of over 190 million nodes. The last paper presents a novel matrix exponential method for transient circuit simulation, especially applicable to power grids.

6B.1* Fast Transform-Based Preconditioners for Large-Scale Power Grid Analysis on Massively Parallel Architectures
Konstantis Daloukas, Nestor Evmorfopoulos, George Drasidis, Michalis Tsiampas, Panagiota Tsompanopoulou, George I. Stamoulis - *Univ. of Thessaly*

6B.2 Deterministic Random Walk Preconditioning for Power Grid Analysis
Jia Wang - *Illinois Institute of Technology*

6B.3 Efficient Parallel Power Grid Analysis via Additive Schwarz Method
Ting Yu, Zigang Xiao, Martin D. F. Wong - *Univ. of Illinois at Urbana-Champaign*

6B.4 Circuit Simulation via Matrix Exponential Method for Stiffness Handling and Parallel Processing
Shih-Hung Weng, Chung-Kuan Cheng - *Univ. of California at San Diego*
Quan Chen, Ngai Wong - *The Univ. of Hong Kong*

All speakers are denoted in bold | * - denotes best paper candidate

6C Efficient Verification and Yield Estimation for Analog Circuits
Room: Winchester

Moderators:

Ibrahim Elfadel - *Masdar Institute of Science and Technology*
Eric Keiter - *Sandia National Laboratories*

Advanced process technologies bring renewed challenges to design in general and analog design in particular due to increasing circuit size, complexity and process variations. The papers in this session propose novel techniques for improving computational efficiency in circuit simulation, verification and yield estimation for analog and mixed signal circuits. They are based on novel stochastic formulations, new ways to combine circuits with device-level analysis, improved iterative techniques via graph-based preconditioning, and the use of SMT-based solvers for formal verification.

6C.1 An Efficient Control Variates Method for Yield Estimation of Analog Circuits Based on a Local Model
Pierre-Francois Desrumaux, Yoan Dupret, Jens Tingleff, Sean Minehane, Mark Redford - *Cambridge Silicon Radio*
Laurent Latorre, Pascal Nouet - *Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier*

6C.2* A Fast Time-Domain EM-TCAD Coupled Simulation Framework via Matrix Exponential
Quan Chen, Li-Jun Jiang, Guan-Hua Chen, Ngai Wong - *The Univ. of Hong Kong*
Wim Schoenmaker - *Magwel*
Shih-Hung Weng, Chung-Kuan Cheng - *Univ. of California at San Diego*

6C.3 GPSCP: A General-Purpose Support-Circuit Preconditioning Approach to Large-Scale SPICE- Accurate Nonlinear Circuit Simulations
Xueqian Zhao, Zhuo Feng - *Michigan Technological Univ.*

6C.4 Verifying Dynamic Properties of Nonlinear Mixed-Signal Circuits via Efficient SMT-Based Techniques
Peng Li, Leyi Yin, Yue Deng - *Texas A&M Univ.*

6D Special Session: Toward Co-Design in High-Performance Computing Systems
Room: Market 1 & 2

Moderator:

X. Sharon Hu - *Univ. of Notre Dame*

Organizers:

X. Sharon Hu - *Univ. of Notre Dame*
Richard Barrett - *Sandia National Laboratories*

High performance computing (HPC) is facing daunting challenges going from peta-scale to exa-scale. It is well accepted that HPC system development requires fundamental changes. The "co-design" principle may offer a common basis for application and system developers as well as computer architects to work synergistically toward achieving exa-scale computing. Considerable effort is being invested by the HPC community to investigate systematic codesign approaches. For example, application proxies, called "miniapps", are being developed to aid the exploration of the architectural design space. Simulation tool suites are being constructed to allow performance/power analysis of different architectures running different algorithm implementations. Methods are being studied to reconfigure code for extracting performance potential of GPU-accelerated nodes. Programming models are evolving to ease the burden on the code developer while at the same time focusing attention on key performance issues. This special session aims to introduce to the EDA community the unique challenges and opportunities that HPC system development presents. It will also discuss the progress that has been made towards applying the codesign principle in HPC system development. There are many new research problems to be addressed in this area and the expertise of EDA researchers can be valuable to tackle these problems.

6D.1 Toward Co-Design in High-Performance Computing Systems
Richard Barrett, Sudip Dosanjh, Michael A. Heroux - *Sandia National Laboratories*
X.S. Hu - *Univ. of Notre Dame*
S. Parker - *NVIDIA Corp.*
J. Shalf - *Lawrence Berkeley National Lab*

Presenters:

John Shalf - *Lawrence Berkeley National Lab*
Richard Barrett - *Sandia National Laboratories*
Stephen Parker - *NVIDIA Corp.*
Sudip Dosanjh - *Sandia National Laboratories*

7A System-Level Modeling and Optimization
Room: Almaden 1

Moderator:

Sri Parameswaran - *Univ. of New South Wales*

The authors of the first paper propose an approach to build efficient and accurate cost models of NoC components. The second paper addresses design optimisation of NoC architectures with stacked DRAMs. The authors propose a memory interface synthesis framework for co-synthesis of both the hardware configuration of the distributed memory interface, and the software architecture of task mapping and data assignment. Finally, in the third talk, a new technique for efficient design space exploration in the context of component-based system design is presented.

7A.1 Accurate On-Chip Router Area Modeling with Kriging Methodology
Florentine Dubois, Valerio Catalano, Marcello Coppola - *STMicroelectronics*
Frederic Petrot - *TIMA Laboratory, CNRS/Grenoble INP/UJF*

7A.2 Distributed Memory Interface Synthesis for Network-on-Chips with 3-D Stacked DRAMs
Yi-Jung Chen - *National Chi Nan Univ.*
Chia-Lin Yang - *National Taiwan Univ.*
Jian-Jia Chen - *Karlsruhe Institute of Technology*

7A.3 Efficient Design Space Exploration for Component-Based System Design
Yinghai Lu - *Synopsys, Inc.*
Hai Zhou - *Northwestern Univ.*

7B High-Level Design Methods
Room: Almaden 2

Moderator:

Mohammad A. Al Faruque - *Univ. of California, Irvine*

This session presents high-level design automation methods applied to three applications. The first paper minimizes hardware for the multiple constant multiplications (MCM) problem, commonly found in DSP applications, by tuning the constant values in the sub-expression elimination using a proper 0-1 ILP formulation. The second paper presents a new FSM synthesis method intended for computing on stochastic bit streams, with hardware overhead for high tolerance to input data errors. The third paper presents a partitioning and scheduling strategy for behavioral synthesis that takes into account multiple memory references to different cyclically partitioned memory banks to support simultaneous memory accesses in loop pipelining.

7B.1 Multiple Tunable Constant Multiplications: Algorithms and Applications
Levent Aksoy - *INESC-ID*
Eduardo Costa - *Catholic Univ. of Pelotas*
Paulo Flores, José Monteiro - *INESC-ID/IST - TU Lisbon*

7B.2 The Synthesis of Complex Arithmetic Computation on Stochastic Bit Streams Using Sequential Logic
Peng Li, David J. Lilja, Kia Bazargan, Marc Riedel - *Univ. of Minnesota*
Weikang Qian - *Univ. of Michigan-Shanghai Jiao Tong Univ. Joint Institute*

7B.3 Memory Partitioning and Scheduling Co-Optimization in Behavioral Synthesis
Peng Li, Yuxin Wang, Guojie Luo, Tao Wang - *Peking Univ.*
Peng Zhang, Jason Cong - *Univ. of California, Los Angeles*

All speakers are denoted in bold | * - denotes best paper candidate

7C Special Session: The Next Wave: Top Challenges in Electromagnetic-Based Design Automation

Room: Winchester

Moderator:

Vikram Jandhyala - *Univ. of Washington*

Organizers:

Marinos Vouvakis - *Univ. of Massachusetts, Amherst*

Joel Phillips - *Cadence Design Systems, Inc.*

Electronic Design Automation and Electromagnetic Simulation have traditionally been different communities, each with a variety of complex algorithms to solve large-scale design problems. With the increasing emphasis on ubiquitous wireless connectivity, higher complexity and speeds, and the requirement for coexistence of multiple systems, electromagnetic-based design automation is becoming an emerging need. The main objective of the special session, entitled "The Next Wave: Top Challenges in Electromagnetic-Based Design Automation" is as a step to bridge the gap between the Electronics Design Automation and Computational Electromagnetics communities. Four invited speakers who are renowned world experts in four of the top critical aspects of electromagnetic-based design automation (variability, scalability, high-dimensional design, multiphysics simulation, and model order reduction) have accepted invitations to speak at this special session.

7C.1 Confronting and Exploiting Operating Environment Uncertainty in Predictive Analysis of Signal Integrity

Andreas Cangellaris - *Univ. of Illinois at Urbana-Champaign*

7C.2 Multi-Scale, Multi-Physics Analysis for Device, Chip, Package, and Board Level

Weng Cho Chew - *Univ. of Illinois at Urbana-Champaign*

7C.3 Design Strategies for High-Dimensional Electromagnetic Systems

Vikram Jandhyala, Arun V. Sathanur - *Univ. of Washington*

7C.4 Co-Simulations of Electromagnetic and Thermal Effects in Electronic Circuits using Non-Conformal Numerical Methods

Jin-Fa Lee, Yang Shao, Zhen Peng - *Ohio State Univ.*

7D Embedded Tutorial: Printable Electronics

Room: Market 1 & 2

Moderator:

Mehdi Tahoori - *Karlsruhe Institute of Technology*

Organizer:

Mehdi Tahoori - *Karlsruhe Institute of Technology*

The notion of printable electronics encompasses any printing technologies or processes to create electronic devices, circuits and systems. Printed electronics will complement rather than compete with silicon-based electronics. It aims at completely different application markets where solution-processable, simple and laterally structured circuitry, such as energy storage devices, radio-frequency identification tags (RFID) tags on plastic foils, flexible displays, artificial skins, electronic textiles, electronic toys, etc. will be manufactured with high throughput. At the advent of the idea of solution-processed devices, organic semiconductors became the immediate choice due to their easy solution processability. Recently, inorganic oxide semiconductors are also considered as a vital component of Printed Electronics since most of the inexpensive, non-toxic, high quality oxide semiconductors are electron conductors. This tutorial provides a cross-cutting overview of recent research findings to develop printable electronics technology. Moreover, the objective of this tutorial is to bring the attention of design automation community to these novel devices, including the challenges and opportunities provided by these novel devices and technologies. Hopefully this will inspire designers and CAD community to come up with intelligent circuit design and automation techniques to fully explore the potentials of these emerging devices for their emerging market sector.

Presenters:

Subho Dasgupta - *Karlsruhe Institute of Technology*

Makoto Takamiya - *Univ. of Tokyo*

IEEE/ACM ICCAD 2012 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

WEDNESDAY, NOVEMBER 7

9:00 - 10:00am - KEYNOTE ADDRESS

KEYNOTE ADDRESS:
Sebastian Thrun, *Udacity, Inc.*
Room: **Almaden 1 & 2**

10:30am - 12:00pm

SESSION 8A: Runtime Adaptation for Performance and Reliability
Room: **Almaden 1**

SESSION 8B: DESIGNER TRACK: Challenges in Embedded CPU/GPU Core Design
Room: **Almaden 2**

SESSION 8C: Emerging Technologies for More-Moore and More-than-Moore Eras
Room: **Winchester**

SESSION 8D: SPECIAL SESSION: The Secret Art of Analog/Mixed-Signal Post-Silicon Validation
Room: **Market 1 & 2**

2:00 - 4:00pm

SESSION 9A: Novel Techniques for Network on Chips and Hardware Security
Room: **Almaden 1**

SESSION 9B: Advances in Logic Synthesis
Room: **Almaden 2**

SESSION 9C: New Approaches in Physical Synthesis of Nano-Scale Analog Circuits
Room: **Winchester**

SESSION 9D: SPECIAL SESSION: Power Grid Simulation and Verification for Billion-Transistor VLSI Designs
Room: **Market 1 & 2**

4:30 - 6:00pm

SESSION 10A: SPECIAL SESSION: Power-Efficient Design and Management of OLED Displays
Room: **Almaden 1**

SESSION 10B: 2-D and 3-D Physical Design Optimization
Room: **Almaden 2**

SESSION 10C: Enabling Design for Resilience
Room: **Winchester**

SESSION 10D: EMBEDDED TUTORIAL: High-Performance, Low-Power Resonant Clocking
Room: **Market 1 & 2**

LUNCH: 12:00 - 1:45pm: Hyatt Hotel - Grand Hall

Colleague Networking Reception **6:00-6:30pm, Almaden Foyer**

Registration: 7:00am - 6:00pm - Almaden Foyer
Parking: $10 per day with in and out privileges
Speakers Breakfast: 7:30 - 8:30am - Santa Clara 1 & 2
AV practice rooms: 7:00am - 4:00pm - Pacific, Executive Boardroom, and University

KEYNOTE: Designing for an Online Learning Community

Room: Almaden 1 & 2

Presenter: Sebastian Thrun - *Udacity, Inc.*

Higher education is going through a disruptive change. While in the past, higher education required physical presence, and learners met in small classrooms with carefully chosen peers and aspiring research professors, in the future the dominant mode of learning will take place at home, or at work, using online media. Most online work attempts to replicate the classroom experience. Just as most early TV work replicated radio. Or most early film replicated stage play. The speaker will discuss his experiences designing a different kind of online learning, which is student-driven and which uses exercises and peer groups as the main vehicle for education.

Sebastian Thrun runs Udacity, a company whose mission is to democratize higher education. He also is a part time Google Fellow and Research Professor at Stanford Univ.. Thrun was elected into the National Academy of Engineering in his Thirties. He has published over 370 research papers, and among his recent awards is the Max-Planck Research award, which carries a prize of $1M. Fast Magazine named him the fifth smartest person in business; he's on Vanity Fair's list of the New Establishment; his inventions have been featured as the best 50 inventions by Time Magazine, and one of his robots was named the top robot of all times by Wired Magazine.

8A Runtime Adaptation for Performance and Reliability
Room: Almaden 1

Moderators:

Jian-Jia Chen - *Karlsruhe Institute of Technology*
Naehyuck Chang - *Seoul National Univ.*

The first paper in this session addresses some of the design challenges with dynamic partial reconfiguration on FPGAs. The authors propose a novel algorithm for the PR Module generation problem which can smoothly be integrated into current FPGA design flows. The second presentation addresses the issue of process migration, a method used in Multi-Processor Systems on Chip to improve reliability, reduce thermal hotspots, and balance loads. The proposed approach leverages custom instructions to integrate a base processor architecture, with process migration functionality. In the last talk the authors deal with process variations of thin-film transistors and the aging degradation of Organic Light Emitting Diode (OLED) devices. The problem is tackled by a nonuniformity detection and compensation technique for thin-film transistor process variation and OLED aging degradation.

8A.1 ISBA: An Independent Set-Based Algorithm for Automated Partial Reconfiguration Module Generation
Ruining He, Yuchun Ma, Kang Zhao, Jinian Bian - *Tsinghua Univ.*

8A.2 Fine-Grained Hardware/Software Methodology for Process Migration in MPSoCs
Tuo Li, Jude Angelo Ambrose, Sri Parameswaran - *Univ. of New South Wales*

8A.3 Active Compensation Technique for the Thin-Film Transistor Variations and OLED Aging of Mobile Device Displays
Xiang Chen, Beiye Liu, Yiran Chen - *Univ. of Pittsburgh*
Mengying Zhao, Chun Jason Xue - *City Univ. of Hong Kong*
Xiaojun Guo - *Shanghai Jiao Tong Univ.*

8B Designer Track: Challenges in Embedded CPU/GPU Core Design
Room: Almaden 2

Moderator:

Sheng Li - *Hewlett-Packard Labs.*

Organizer:

Yao-Wen Chang - *National Taiwan Univ.*

Embedded CPU/GPU cores are pervasive in modern SOC design. This session invites three key companies to address recent technology trends and new challenges in embedded CPU/GPU core design, including architecture design, heterogeneous multi-processor solutions, implementation methodologies, power and performance optimization, tool chain development, and so on.

8B.1 Challenges in Validating Next-Generation GPU Compute Capable GPUs
Paul Martin - *ARM, Inc.*

8B.2 Implementing High-Performance, Low-Power Embedded Processors: Challenges and Solutions
Koen Lampaert - *Broadcom Corp.*

8B.3 Latency Tolerance for Throughput Computing
Chien-Ping Lu, Brian Ko - *MediaTek, Inc.*

All speakers are denoted in bold | * - denotes best paper candidate

8C Emerging Technologies for More-Moore and More-than-Moore Eras
Room: Winchester

Moderator:

Jason Xue - *City Univ. of Hong Kong*

As conventional CMOS technology scaling approaches its physical limits, new technologies are evolving in the More-Moore (smaller feature size via scaling) and More-than-Moore (more functionality via 3-D integration) eras. Both evolution schemes offer new challenges and opportunities for the design automation community. The first paper analyzes the feasibility of multi-level spin-transfer torque memory from a statistical point of view. The second paper demonstrates the implementation of compact NEM-based logic gates and discusses their applications in FPGA design. The third paper shows how EDA flow can be extended to design monolithic 3-D ICs.

8C.1 Multi-level Cell STT-RAM: Is It Realistic or Just a Dream?
Yaojun Zhang, Lu Zhang, Wujie Wen, Yiran Chen - *Univ. of Pittsburgh*
Guangyu Sun - *Peking Univ.*

8C.2 Ultra-Low Power NEMS FPGA
Daniel G. Saab, Sijing Han - *Case Western Reserve Univ.*
Vijay Sirigiri - *Intel Corp.*
Massood Tabib-Azar - *Univ. of Utah*

8C.3 Ultra High Density Logic Designs Using Transistor-Level Monolithic 3-D Integration
Young-Joon Lee, Sung Kyu Lim - *Georgia Institute of Technology*
Patrick Morrow - *Intel Corp.*

8D Special Session: The Secret Art of Analog/Mixed-Signal Post-Silicon Validation
Room: Market 1 & 2

Moderator:

Eli Chiprout - *Intel Corp.*

Organizer:

Eli Chiprout - *Intel Corp.*

This special session deals with post-silicon electrical validation, an area that has not received much CAD attention in the past. The first paper will give an overview of post-silicon I/O validation and outline the challenges and research directions needed for CAD development in the area. The second paper will deal with Baysian model fusion (BMF) techniques with application to modeling and post-silicon tuning of analog circuits. The third paper will propose a post-silicon validation methodology for analog/mixed-signal/RF SoCs that relies on the use of special stimulus designed to expose differences between observed device behavior and its predictive model.

8D.1 Challenges in Post-Silicon Validation of High-Speed I/O Links
Chenjie Gu - *Intel Corp.*

8D.2 Post-Silicon Modeling and Tuning of Analog/Mixed-Signal Circuits via Bayesian Model Fusion
Xin Li - *Carnegie Mellon Univ.*

8D.3 Validation Signature Testing: A Methodology for Post-Silicon Validation of Analog/Mixed-Signal Circuits
A. Chatterjee, S. Deyati, B. Muldrey, S. Devarakond, A. Banerjee - *Georgia Institute of Technology*

9A Novel Techniques for Network on Chips and Hardware Security
Room: Almaden 1

Moderators:

John Bainbridge - *Sonics, Inc.*
Grant Martin - *Tensilica, Inc.*

This session spans aspects of Network on Chips and Hardware Security. The first paper presents a novel method for post silicon functional debugging of complex hardware systems. The next paper is the first effort that exploits adaptivity inside routing elements. The last two papers demonstrate advances in hardware security. One of them introduces a hardware trojan detection approach and the other proposes a hardware-based public key policy where unlimited hardware users can communicate using single-cycle secure communication.

9A.1 Functional Post-Silicon Diagnosis and Debug for Networks-on-Chip
Rawan Abdel-Khalek, Valeria Bertacco - *Univ. of Michigan*

9A.2 TRACKER: A Low Overhead Adaptive NoC Router with Load Balancing Selection Strategy
John Jose, K. V. Mahathi, J. Shiva Shankar, Madhu Mutyam - *Indian Institute of Technology, Madras*

9A.3 Provably Complete Hardware Trojan Detection using Test Point Insertion
Sheng Wei, Miodrag Potkonjak - *Univ. of California, Los Angeles*
Kai Li, Farinaz Koushanfar - *Rice Univ.*

9A.4 Using Standardized Quantization for Multi-Party PPUF Matching: Foundations and Applications
Miodrag Potkonjak, Saro Meguerdichian - *Univ. of California, Los Angeles*

9B Advances in Logic Synthesis
Room: Almaden 2

Moderator:

Iris Hui-Ru Jiang - *National Chiao Tung Univ.*

In this session, novel logic synthesis techniques for solving practical problems are presented. The first paper describes a method for monitoring information flow in Boolean networks. In the second paper, a method for reducing circuit timing error rates and improving throughput is proposed. In the third paper, an efficient logic synthesis approach based on re-using already known good network structures is described. Finally, the last paper presents design of a standard cell library of threshold gates built using differential mode threshold gates (DTGs) and a functional decomposition method to map arbitrary Boolean functions using DTGs.

9B.1 Simultaneous Information Flow Security and Circuit Redundancy in Boolean Gates
Jason Oberg, Ryan Kastner - *Univ. of California at San Diego*
Wei Hu, Dejun Mu - *Northwestern Polytechnical Univ.*

9B.2 On Logic Synthesis for Timing Speculation
Rakesh Kumar - *Univ. of Illinois at Urbana-Champaign*
Yuxi Liu, Rong Ye, Feng Yuan, Qiang Xu - *The Chinese Univ. of Hong Kong*

9B.3 Lazy Man's Logic Synthesis
Wenlong Yang, Lingli Wang - *Fudan Univ.*
Alan Mishchenko - *Univ. of California, Berkeley*

9B.4 Minimizing Area and Power of Sequential CMOS Circuits using Threshold Decomposition
Niranjan Kulkarni, Nishant Nukala, Sarma Vrudhula - *Arizona State Univ.*

All speakers are denoted in bold | * - denotes best paper candidate

9C New Approaches in Physical Synthesis of Nano-Scale Analog Circuits

Room: Winchester

Moderator:

Sheldon Tan - *Univ. of California, Riverside*

This section includes the latest advancements on algorithms for physical design of analog circuits. The first paper discusses monotonic current paths for analog circuit placement and its effectiveness in improving layout performance and size. The second paper proposes a constraint unification representation in OpenAccess and its application to hierarchical routing. The third paper describes Bayesian Model Fusion for speeding up parametric yield estimation.

9C.1 Performance-Driven Analog Placement Considering Monotonic Current Paths

Po-Hsun Wu, Yang-Ru Chen, Bing-Shiun Chou, Tsung-Yi Ho, Bin-Da Liu, Mark Po-Hung Lin - *National Chung Cheng Univ.*

Tung-Chieh Chen - *SpringSoft, Inc.*

9C.2 Configurable Analog Routing Methodology via Technology and Design Constraint Unification

Po-Cheng Pan, Hung-Ming Chen - *National Chiao Tung Univ.*

Yi-Kan Cheng, Jill Liu, Wei-Yi Hu - *Taiwan Semiconductor Manufacturing Co., Ltd.*

9C.3 Efficient Parametric Yield Estimation of Analog/Mixed-Signal Circuits via Bayesian Model Fusion

Xin Li, Wangyang Zhang, Fa Wang, Shupeng Sun - *Carnegie Mellon Univ.*

Chenjie Gu - *Intel Corp.*

9C.4 Analytical-Based Approach for Capacitor Placement with Gradient Error Compensation and Device Correlation Enhancement in Analog Integrated Circuits

Cheng-Wu Lin, Chung-Lin Lee, Jai-Ming Lin, Soon-Jyh Chang - *National Cheng Kung Univ.*

9D Special Session: Power Grid Simulation and Verification for Billion-Transistor VLSI Designs

Room: Market 1 & 2

Moderator:

Claude Moughanni – *Lattice Semiconductor Corp.*

Organizer:

Zhuo Li - *IBM Corp.*

Although power grid analysis has been an active research area for a number of years, increasing chip size has exposed new challenges in this traditional topic. The simulation of these large scale networks is becoming a dominant step in the design verification flow and it often requires the very largest computer available to the design team. To spur academic research in this vital verification step, the IBM Austin Research Lab, with support from the ACM TAU Workshop, has successfully organized two annual TAU Power Grid Simulation Contest, with over twenty Univ. teams across the world participated. For 2012, the contest focused on transient analysis and parallel implementation. This special session starts with the overview of the contest and the release of new IBM benchmarks. The top three winning teams will then disclose the methods/techniques they applied to successfully tackle these large scale industrial power grid designs. Also, three academic and industry experts will review the research history of power grid simulation and verification, how power grid analysis is embedded in the real life chip design process, and lay out the future direction of power grid research and potential problems for future contests.

9D.1 2012 TAU Power Grid Simulation Contest: Benchmark Suite and Results

Zhuo Li, Raju Balasubramanian, Frank Liu - *IBM Corp.*

Sani Nassif - *IBM Research - Austin*

9D.2 PGT_SOLVER: An Efficient Solver for Power Grid Transient Analysis

Ting Yu, Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign*

9D.3 PowerRush: Efficient Transient Simulation for Power Grid Analysis

Jianlei Yang, Zuowei Li, Yici Cai, Qiang Zhou - *Tsinghua Univ.*

9D.4 Parallel Forward and Back Substitution for Efficient Power Grid Simulation

Xuanxing Xiong, Jia Wang - *Illinois Institute of Technology*

9D.5 Design Analysis of IC Power Delivery

Peng Li - *Texas A&M Univ.*

9D.6 Power Grid Effects and Their Impact On-Die

Eli Chiprout - *Intel Corp.*

9D.7 Overview of Vectorless/Early Power Grid Verification

Farid N. Najm - *Univ. of Toronto*

10A Special Session: Power-Efficient Design and Management of OLED Displays

Room: Almaden 1

Moderator:

Jason Xue - *City Univ. of Hong Kong*

Organizer:

Jason Xue - *City Univ. of Hong Kong*

Display is a large power consumer of modern smartphones and tablets. OLED is replacing LCD in recent years because of its power efficiency. However, it is observed by different research communities that there is a significant space for power reduction of OLED displays. This special session brings together researchers for power efficient OLED design and management at different layers and different communities.

10A.1 High-Performance Metal-Oxide TFT and its Application for High-Power Efficiency AMOLED Displays

Gang Yu, Chan-Long Shieh - *CBRITE, Inc.*

10A.2 Transistor Technologies and Pixel Circuit Design for Efficient Active-Matrix Organic Light-Emitting Diode Displays

Xiaojun Guo, Guangyu Yao, Xiaoli Xu, Wenjiang Liu, Tao Liu - *Shanghai Jiao Tong Univ.*

10A.3 Battery Cell Configuration for Organic Light Emitting Diode Display in Modern Smartphones and Tablets-PCs

Naehyuck Chang, Donghwa Shin, Kitae Kim - *Seoul National Univ.*

Massoud Pedram - *Univ. of Southern California*

10A.4 Mobile Devices User - The Subscriber and also the Publisher of Real-Time OLED Display Power Management Plan

Yiran Chen, Xiang Chen - *Univ. of Pittsburgh*

Chun Jason Xue, Mengying Zhao - *City Univ. of Hong Kong*

10B 2-D and 3-D Physical Design Optimization

Room: Almaden 2

Moderator:

Thorlindur Thorolfsson - *North Carolina State Univ.*

This session presents three physical design solutions at different levels of the design process in order to improve the operation of 2D and 3-D ICs. In particular, the power minimization and management of 2D ICs at the clock design and floorplanning stages are investigated in the first two papers. The third paper presents a holistic methodology for 3-D IC design planning.

10B.1 Clock Mesh Synthesis with Gated Local Trees and Activity Driven Register Clustering

Jianchao Lu - *Synopsys, Inc.*

Xiaomi Mao - *Oracle Corp.*

Baris Taskin - *Drexel Univ.*

10B.2 Fast Approximation for Peak Power Driven Voltage Partitioning in Almost Linear Time

Jia Wang, Xiaodao Chen, Lin Liu, Shiyan Hu - *Michigan Technological Univ.*

10B.3 Multiobjective Optimization of Deadspace, a Critical Resource for 3-D-IC Integration

Johann Knechtel, Jens Lienig, Matthias Thiele - *Dresden Univ. of Technology*

Igor L. Markov - *Univ. of Michigan*

10B.4 A Fast Maze-Free Routing Congestion Estimator with Hybrid Unilateral Monotonic Routing

Wen-Hao Liu, Yih-Lang Li - *National Chiao Tung Univ.*

Cheng-Kok Koh - *Purdue Univ.*

All speakers are denoted in bold | * - denotes best paper candidate

10C Enabling Design for Resilience
Room: Winchester

Moderator:

Sung Kyu Lim - *Georgia Institute of Technology*

The first paper describes a compact circuit model for the magnetic tunneling junction (MTJ), with applications to variability modeling and soft error analysis of MTJ-based memory cells. The second paper describes synthesis techniques to tradeoff resilience against quality in approximate adders, with applications to image and media processing. The third paper describes how to synthesize representative critical reliability paths to enable low-cost, accurate on-chip evaluation of circuit aging.

10C.1 A Thermal and Process Variation Aware MTJ Switching Model and Its Applications in Soft Error Analysis

Wei Zhang - *Nanyang Technological Univ.*

Peiyuan Wang, Yiran Chen - *Univ. of Pittsburgh*

Rajiv Joshi - *IBM T.J. Watson Research Center*

Rouwaida Kanj - *American Univ. of Beirut*

10C.2 Modeling and Synthesis of Quality-Energy Optimal Approximate Adders

Jin Miao, Ku He, Andreas Gerstlauer, Michael Orshansky - *Univ. of Texas at Austin*

10C.3 Representative Critical Reliability Paths for Low-Cost and Accurate On-Chip Aging Evaluation

Shuo Wang, Jifeng Chen, Mohammad Tehranipoor - *Univ. of Connecticut*

10D Embedded Tutorial: High-Performance, Low-Power Resonant Clocking
Room: Market 1 & 2

Moderator:

Matthew R. Guthaus - *Univ. of California, Santa Cruz*

Organizers:

Matthew Guthaus - *Univ. of California, Santa Cruz*

Baris Taskin - *Drexel Univ.*

Clock distribution networks consume a significant portion of on-chip power. Traditional buffered clock distribution power is limited by frequency, capacitance, and activity rates. Resonant clock distributions can reduce this power by “recycling” energy on-chip and reducing the overall clock power. This tutorial introduces recent techniques for distributed-LC, traveling wave, and standing wave resonant clock distributions. In particular, the tutorial discusses the open research problems and recent developments. The tutorial covers both circuits and computer-aided design algorithms and methodologies for resonant clocking.

10D.1 High-Performance, Low-Power Resonant Clocking

Matthew R. Guthaus - *Univ. of California, Santa Cruz*

Baris Taskin - *Drexel Univ.*

Presenters:

Matthew R. Guthaus - *Univ. of California, Santa Cruz*

Baris Taskin - *Drexel Univ.*

Vinayak Honkote - *Intel Corp.*

THURSDAY, NOVEMBER 8

8:15am - 5:00pm

WORKSHOP 1W:
International Workshop on Design Automation for Analog and Mixed-Signal Circuits
Room: **Almaden 1**

8:30am - 6:00pm

WORKSHOP 2W:
1st International Workshop on Domain-Specific Multicore Computing (DSMC)
Room: **Winchester**

8:50am - 5:00pm

WORKSHOP 3W:
IEEE Workshop on Variability Modeling and Characterization (VMC)
Room: **Almaden 2**

8:15am - 5:00pm

WORKSHOP 4W:
2012 IEEE/ACM Workshop on CAD for Multi-Synchronous and Asynchronous Circuits and Systems
Room: **Market 1 & 2**

8:30am - 5:30pm

WORKSHOP 5W: International Workshop on Hardware/Software Techniques for Cross-Layer Resiliency
Room: **San Carlos**

LUNCH: 12:00 - 1:00pm Room: San Jose 1 & 2 on the second floor

Registration: 7:30am - 4:00pm - Almaden Foyer
Parking: $10 per day with in and out privileges

All speakers are denoted in bold | * - denotes best paper candidate

1W Workshop: International Workshop on Design Automation for Analog and Mixed-Signal Circuits

Room: Almaden 1

Organizers:

Xin Li - *Carnegie Mellon Univ.*
Chandramouli Kashyap - *Intel Corp.*
Jaeha Kim - *Seoul National Univ.*
Trent McConaghy - *Solido Design Automation, Inc.*
Jun Tao - *Fudan Univ.*
Angan Das - *Intel Corp.*

With the aggressive scaling of advanced IC technologies, today's analog and mixed-signal (AMS) circuits have become extremely complex. As circuit designers have adopted a number of non-traditional methodologies (e.g., multi-mode operation, adaptive self-healing, etc) to address the design challenges associated with technology scaling (e.g., reduced voltage headroom, increased process variation, etc), the corresponding digital-analog interactions have become increasingly difficult to verify. These recent trends of AMS circuits have brought up enormous new challenges and opportunities for AMS CAD. The purpose of this workshop is to report recent advances on AMS CAD and, more importantly, motivate new research topics and directions in this area. Topics of interest include (but not limited to):

- Behavioral and performance modeling at both circuit and system levels
- Analog and mixed-signal simulation and verification AMS self-healing and post-silicon tuning
- AMS circuit optimization and design space exploration
- PVT variations and reliability for AMS circuits
- AMS testing and diagnosis

Speakers:

Joel Phillips - *Cadence Design Systems, Inc.*
Duaine Pryor - *Mentor Graphics Corp.*
Mohan Sunderarajan - *Synopsys, Inc.*
John Carulli - *Texas Instruments, Inc.*
Chris Myer - *Univ. of Utah*
Jesse Chen - *Qualcomm*
Mark Horowitz - *Stanford Univ.*
Rachael Parker - *Intel Corp.*
Bob Mullen - *Taiwan Semiconductor Manufacturing Co., Ltd.*

Panel:
Challenges in Analog Design and How CAD Can Help

Moderator:

Kevin Jones - *City Univ. of London*

Panelists:

Rachael Parker - *Intel Corp.*
John Carulli - *Texas Instruments, Inc.*
Joel Phillips - *Cadence Design Systems, Inc.*
Mohan Sunderarajan - *Synopsys, Inc.*
Duaine Pryor - *Mentor Graphics Corp.*

2W Workshop: 1st International Workshop on Domain-Specific Multicore Computing (DSMC)

Room: Winchester

Organizers:

Jürgen Teich - *Univ. of Erlangen-Nuremberg*
Vijaykrishnan Narayanan - *Pennsylvania State Univ.*

The steady advances in semiconductor technology allow for increasingly complex SoCs, including multiple (heterogeneous) micro processors, large on-chip memories sophisticated interconnection networks, and peripherals. The downside of this technological progress is that computing has hit already a power and complexity wall. In order to scale computing performance in the future, systems' energy efficiency has to be significantly improved. The design of heterogeneous hardware with different specialized resources, such as accelerators dedicated for one application domain is a promising solution to address this challenge. However, design, test and verification, as well as parallel programming of such heterogeneous systems introduce new challenges.

Compared to general-purpose multicore computing, domain-specific multicore computing is tailored for one application domain or problem field, and thus, can enhance performance and energy-efficiency of the system, as well as productivity and portability of the software, and eventually, scalability of the entire system. To realize such systems, significant advances are required in multiple related aspects.

First, methodologies for designing customizable architecture platforms are required. Second, domain-specific languages are needed to permit non-computing domain experts to concentrate on algorithm development rather than on low level implementation details. Third, compilation and code generation techniques as well as methods for runtime management have to identify parallel computation patterns and must employ domain-specific knowledge in order to achieve a reasonable performance.

This workshop aims at bringing researches and experts from both academia and industry together to discuss and exchange research advances on domain-specific computing. A distinctive feature of the workshop is its cross section through all the aforementioned levels, ranging from programming down to custom hardware. Thus, the workshop is targeted for all of those who are interested in understanding the big picture and the potential of domain-specific computing, its challenges, available solutions, and enables for collaboration of the different domains. The workshop will feature invited talks by reputed researchers and cover the following areas:

- **Domain-specific hardware platforms, domain-specific heterogeneous multi-processor systems-on-a-chip, domain-specific accelerators**
- **Domain-specific languages and application design**
- **Domain-specific compilation and mapping methods, and run-time support**

Furthermore, a special issue in ACM TECS dedicated to the subject of "Domain-Specific Multicore Computing" has recently been proposed by the workshop organizers and also got accepted. This special issue might also attract submissions from workshop participants to publish their presented work after ICCAD.

Agenda on the next page.

1st International Workshop on Domain-Specific Multicore Computing (DSMC) Workshop Agenda

8:30 - 10:00am
Keynotes:

Architecting Domain-Specific Solutions: Challenges and Opportunities
Ravi Iyer, *Director SoC Platform Architecture (SPA) group - Intel Corp.*

Reconfigurable Multi-Cores for Streaming DSP
Paul Heysters, *CEO - Recore Systems*

10:00 – 10:30am
Coffee Break

10:30am – 12:00pm
Session 1: Domain-specific Hardware Platforms

TOPSTREAM: A Scalable Heterogeneous Multicore Platform
Yukoh Matsumoto - *TOPS Systems Corp.*

Domain-Specific Architectures for Emerging Data-Centric Workloads
Kevin Lim - *Hewlett-Packard Co.*

Invasive Tightly-Coupled Processor Arrays
Frank Hannig - *Univ. of Erlangen-Nuremberg*

12:00 – 1:00pm
Lunch Break

1:00 - 2:30pm
Session 2: Domain-Specific Computing Systems

GreenDroid: An Architecture for the Dark Silicon Age
Michael Taylor - *Univ. of California at San Diego*

Streaming Similarity Computing on FPGAs
Wang Yu - *Tsinghua Univ.*

Domain Specific Accelerators: Opportunities for Software Library Replacement
John Davis - *Microsoft Research*

2:30 - 3:00pm
Poster Session/Coffee Break

3:00 - 4:00pm
Session 3: Domain-Specific Lanugages

Scalable Development of High Performance Domain-Specific Languages with Delite
Kunle Olukuton - *Stanford Univ.*

Bridging the Productivity-Performance Gap with Selective Embedded Just-in-Time Specialization
Shoaib Kamil - *Univ. of California, Berkeley*

4:00 - 6:00pm
Session 4: Domain-Specific Compilation and Mapping Methods

The Softer Side of Software Defined Radio
Yuan Lin - *MediaTek, Inc.*

Building Predictable Cyber-Physical Systems from Dynamic Applications and Platforms
Sander Stuijk - *Eindhoven Univ.*

Design Methodologies and Tools for Energy Efficient Multi-Core Architecture Platforms
Nagu Dhanwada - *IBM Corp.*

Dynamic Behavior Specification and Dynamic Mapping for Real-Time Embedded Systems in HOPES
Soonhoi Ha - *Seoul National Univ.*

3W Workshop: IEEE Workshop on Variability Modeling and Characterization (VMC)

Room: Almaden 2

Organizers:

Hidetoshi Onodera - *Kyoto Univ.*
Yu Cao - *Arizona State Univ.*

It is widely recognized that process variation is emerging as a fundamental challenge to IC design in scaled CMOS technology; and it will have profound impact on nearly all aspects of circuit performance. While some of the negative effects of variability can be handled with improvements in the manufacturing process, the industry is starting to accept the fact that some of the effects are better mitigated during the design process. Handling variability in the design process will require accurate and appropriate models of variability and its dependence on designable parameters (i.e. layout), and its spatial and temporal distributions. It also requires carefully designed test structures and proper statistical data analysis methods to extract meaningful models from large volumes of silicon measurements.

The resulting compact modeling of systematic, random, spatial, and temporal variations is essential to abstract the physical level variations into a format the designers (and more importantly, the tools they use) can utilize. This workshop provides a forum to discuss current practice as well as near future research needs in test structure design, variability characterization, compact variability modeling, and statistical simulation.

Speakers:

Philip Wong - *Stanford Univ.*
Kaushik Roy - *Purdue Univ.*
Asen Asenov - *Univ. of Glasgow*
David Burnett - *GLOBALFOUNDRIES*
Ken Takeuchi - *Chuo Univ.*
Vivek De - *Intel Corp.*
Makoto Takamiya - *Univ. of Tokyo*
Ronald Dreslinski - *Univ. of Michigan*

All speakers are denoted in bold | * - denotes best paper candidate

4W Workshop: 2012 IEEE/ACM Workshop on CAD for Multi-Synchronous and Asynchronous Circuits and Systems

Room: Market 1 & 2

Organizers:

Ken Stevens - *Univ. of Utah, Granite Mountain Technologies*
Mark Greenstreet - *Univ. of British Columbia*

Many current integrated circuit designs are partitioned into multiple timing domains, allowing each domain to be independently optimized for power and performance. This simplifies timing closure and enables the integration of IP blocks with different timing requirements. One system approach is to use traditional handshaking circuits naturally employ locally generated timing signals that can yield high performance or provide fine-grained activity gating for low power. GALS methods where the asynchrony appears at the level of system integration are another approach. Multi-synchronous and asynchronous architectures present design challenges and require supportive CAD that arise when departing from the timing methodology and determinism of single frequency synchronous designs.

While the departure is already well underway, more systematic CAD support for these designs promises lower power, higher robustness, and better performance. Such a new generation of CAD also enables a much wider base of designers to exploit these advantages. This workshop provides a forum to discuss current challenges of asynchronous design, how to address the CAD problem, and how to gain penetration of this disruptive technology in industry. This is intended for both technical and industry experts in the asynchronous, GALS, elastic-pipelining, and latency insensitive design communities.

Speakers:

Peter Beerel - *Intel Corp., Univ. of Southern California*
Ran Ginosar - *Technion - Israel Institute of Technology, vSync Circuits Ltd.*
Pranav Ashar - *Real Intent, Inc.*
Mark Greenstreet - *Univ. of British Columbia*
Andrew Lines - *Intel Corp.*
Marc Renaudin - *Tiempo-IC*
Ken Stevens - *Univ. of Utah, Granite Mountain Technologies*
Ian W. Jones - *Oracle Corp.*

Technical Program Committee:
Co-Chairs:

Ken Stevens - *Univ. of Utah, Granite Mountain Technologies*
Mark Greenstreet - *Univ. of British Columbia*

TPC Members:

John Bainbridge - *Sonics*
Gary Delp - *The Mayo Clinic*
Jo Ebergen - *Oracle*
Steve Furber - *Univ. of Manchester*
Mike Kishinevsky - *Intel Corp.*
Rajit Manohar - *Cornell Univ.*
Marc Renaudin - *Tiempo-IC*

5W Workshop: International Workshop on Hardware/Software Techniques for Cross-Layer Resiliency

Room: San Carlos

Organizers:

Vikas Chandra - *ARM, Inc.*
Nikil Dutt - *Univ. of California, Irvine*
Siddarth Garg - *Univ. of Waterloo*
Brett Meyer - *McGill Univ.*
Sani Nassif - *IBM Research - Austin*
Hiren Patel - *Univ. of Waterloo*
Mehdi Tahoori - *Karlsruhe Institute of Technology*

Improvements in chip manufacturing technology have propelled an astonishing growth of embedded systems which are integrated into our daily lives. However, this trend is facing serious challenges, both at device and system levels. At the device level, as the minimum feature size continues to shrink, a host of vulnerabilities influence the robustness, reliability, and availability of embedded and critical systems. Some of these factors are caused by the stochastic nature of the nanoscale manufacturing process (e.g., process variability, sub-wavelength lithographic inaccuracies), while other factors appear because of high frequencies and nanoscale features (e.g. RLC noise, on-chip temperature variation, increased sensitivity to radiation and transistor aging). At the other end of the spectrum, embedded systems are seeing a tremendous increase in software content. Whereas traditional software design paradigms have assumed that the underlying hardware is fully predictable and error-free, there is now a critical need to build a software stack that is responsive to variations, and resilient against emerging vulnerabilities in the underlying hardware.

The objective of this workshop is to bring the attention of design automation community to the multilevel reliability challenges and solutions and possible paradigm shift to consider reliability throughout the design flow, from devices to systems and applications.

This workshop will focus on innovative device- level, hardware (circuit and micro-architecture level) and software (application, operating system and compiler level) solutions for fault detection and recovery in multi-processor system-on-chip (MPSoC) platforms, as also on solutions for emerging applications and platforms that are inherently forgiving of errors in the computation and communication of data. In addition, this workshop tries to synchronize various existing coordinated research programs on dependability which are currently underway in Europe, Asia, and USA to deal with multi-level reliability challenges.

Speakers:

Prabhakar Kudva - *IBM Research*
Michael Glass - *Univ. of Erlangen-Nuremberg*
Rakesh Kumar - *Univ. of Illinois at Urbana-Champaign*
Sathish Gopalakrishnan - *Univ. of British Columbia*
Sanjit Seshia - *Univ. of California, Berkeley*
Marc Riedel - *Univ. of Minnesota*
Sankar Basu - *National Science Foundation*
Rajesh Gupta - *Univ. of California at San Diego*
Norbert Wehn - *Univ. of Kaiserslautern*
Sani Nassif - *IBM Research - Austin*
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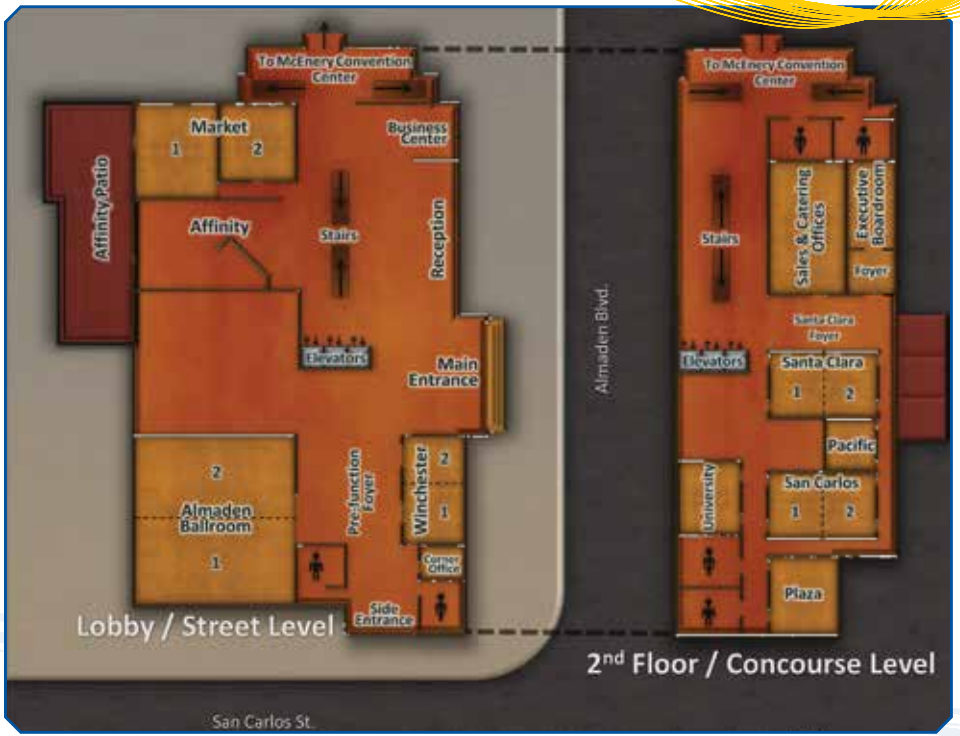

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