NOVEMBER 7-11, 2010 • DOUBLETREE HOTEL • SAN JOSE, CA

IEEE/ACM ICCAD
2010 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

FINAL PROGRAM

The premier conference for Electronic Design Technology

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Sponsored by: IEEE, CEDA IEEE Council on Electronic Design Automation, SIGDA special interest group of ACM design automation

In cooperation with: IEEE, Electron Devices Society, SSCS

Welcome to the 2010 International Conference on Computer-Aided Design (ICCAD)

ICCAD continues to be the premier -- and most selective -- conference devoted to technical innovations in design automation. ICCAD's program of technical papers, tutorials, and keynote highlights the most important current and future research challenges. A day of workshops on hot topics promises non-stop technical excitement. And as always, a large number of side meetings and social events provide plenty of opportunities for networking and meeting colleagues and friends.

This year's ICCAD starts on Monday, November 8 and continues through Wednesday, November 10; you will find up-to-date details on the conference website http://www.iccad.com. This year's CANDE workshop will be held immediately before ICCAD on November 4, only a short hop away in Monterey. ICCAD's workshops will be on Thursday, November 11. Continuing a practice started last year, ICCAD will integrate its tutorials into the technical program Monday through Wednesday. These tutorials, given by world experts, are an excellent opportunity for updating your knowledge in state-of-the-art and emerging areas.

We received 360 worldwide submissions and the technical program committee, after careful deliberation, selected 108 excellent papers for presentation. These papers are split into 40 sessions over the three days of the technical program. In addition, the ICCAD program this year includes eight tutorials, as well as the designer track, all focused on providing additional broad perspectives for our CAD audience.

ICCAD 2010 is privileged to have a keynote address from James Bouwer, from The National Center for Microscopy and Imaging Research (NCMIR) at the University of California, San Diego. James will outline the challenges of imaging in modern biology - a field that shares a number of challenges with IC design, from the design of the detector chips themselves, to the requirements for complex algorithms, huge data sets, and the need for parallel processing. The considerable expertise of the ICCAD community in dealing with problems of scale and technical complexity can be critical to addressing these new challenges successfully, he believes.

I hope you enjoy a week of ICCAD activities!

Louis Scheffer
General Chair
Janelia Farms Research Campus
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IEEE/ACM 2010 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

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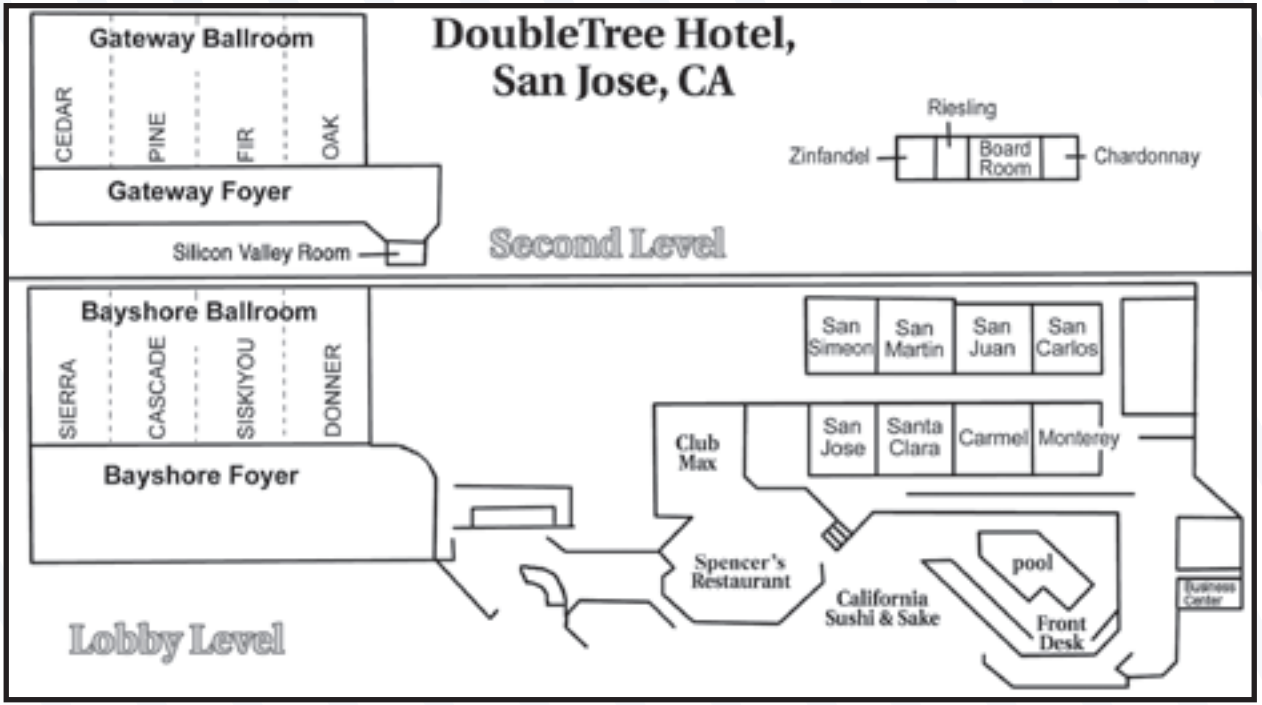
DoubleTree Hotel,
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Best Paper Candidates/Award Committee

Best Paper Award Committee

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Dallas, TX

IEEE/ACM William J. McCalla ICCAD Best Paper Award Candidates

Monday Sessions

1A.1 FIDELITY METRICS FOR ESTIMATION MODELS
Haris Javaid, Aleksander Ignjatovic, Sri Parameswaran - *Univ. of New South Wales*

2B.1 SETS: STOCHASTIC EXECUTION TIME SCHEDULING FOR MULTICORE SYSTEMS BY JOINT STATE SPACE AND MONTE CARLO
Nabeel Iqbal, Jörg Henkel - *Karlsruhe Institute of Technology*

3C.1 YIELD ENHANCEMENT FOR 3-D-STACKED MEMORY BY REDUNDANCY SHARING ACROSS DIES
Li Jiang, Rong Ye, **Qiang Xu** - *The Chinese Univ. of Hong Kong*

Tuesday Sessions

4B.1 GENERALIZED NONLINEAR TIMING/PHASE MACROMODELING: THEORY, NUMERICAL METHODS AND APPLICATIONS
Chenjie Gu, Jaijeet Roychowdhury - *Univ. of California, Berkeley*

5A.1 SELECTIVE INSTRUCTION SET MUTING FOR ENERGY-AWARE ADAPTIVE PROCESSORS
Muhammad Shafique, Lars Bauer, Jörg Henkel - *Karlsruhe Institute of Technology*

7C.1 NATIVE-CONFLICT-AWARE WIRE PERTURBATION FOR DOUBLE PATTERNING TECHNOLOGY
Szu-Yu Chen, Yao-Wen Chang - *National Taiwan Univ.*

Wednesday Sessions

8A.1 BI-DECOMPOSITION OF LARGE BOOLEAN FUNCTIONS USING BLOCKING EDGE GRAPHS
Mihir Choudhury, Kartik Mohanram - *Rice Univ.*

8B.1 OBSTACLE-AVOIDING RECTILINEAR STEINER MINIMUM TREE CONSTRUCTION: AN OPTIMAL APPROACH
Tao Huang, Evangeline F.Y. Young - *The Chinese Univ. of Hong Kong*

9A.1 SIMPL: AN EFFECTIVE PLACEMENT ALGORITHM
Myung-Chul Kim, Dong-Jin Lee, Igor L. Markov - *Univ. of Michigan*

9B.1 CHARACTERIZING THE LIFETIME RELIABILITY OF MANYCORE PROCESSORS WITH CORE-LEVEL REDUNDANCY
Lin Huang, **Qiang Xu** - *The Chinese Univ. of Hong Kong*

The CADathlon at ICCAD

ACM/SIGDA sponsors the ninth annual EDA programming contest at ICCAD

Sunday, November 7, 7:30am - 5:00pm Donner Ballroom

In the spirit of the long-running ACM programming contest, the CADathlon challenges students in their CAD knowledge, and their problem solving, programming, and teamwork skills. It serves as an innovative initiative to assist in the development of top students in the EDA field. The contest will provide a platform for SIGDA, academia, and industry to focus attention on the best and brightest of next generation CAD professionals.

The students will be given a number of problems that range in difficulty and topics. Information about the CAD areas, relevant papers, and potentially a software framework that will run on Linux will be released one week before the competition. Students will be allowed to work in teams of two. At the contest, students will be given the problem statements and an example test data, but they will not have the judges' test data. Solutions will be judged on correctness and efficiency. The team that passes the most testcases is declared the winner. A handsome prize awaits the winning team. The judges are experts in EDA from both academia and industry.

During the competition students will be presented with six problems in the following areas:

- Circuit Design and Analysis Physical Design
- Logic and High-Level Synthesis
- System Design and Analysis
- Functional Verification
- Bio-EDA

The competition is open to all graduate students specializing in CAD currently enrolled full-time in a Ph.D. granting institution in any country. Partial or full travel grants will be provided for qualifying students.

CADathlon Organizing Committee:

Chair, Jarrod Roy, jaroy@us.ibm.com

Vice Chair, Asst. Prof. Sudeep Pasricha, sudeep.pasricha@gmail.com

Vice Chair, Assoc. Prof. Srinivas Katkoori, katkoori@cse.usf.edu

Vice Chair, Sudarshan Banerjee, udarshan_w@yahoo.com

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National Taiwan University of Science and Technology Department Of Electrical Engineering And Technology

43, Keelung Rd., Section 4
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http://vlsi.ee.fju.edu.tw/dat/

The DAT (Design Automation and Test) Consortium, funded by the Ministry of Education, Taiwan, is a technology-oriented, inter-collegiate consortium whose mission is to cultivate high-quality human resources in electronic design automation and test in Taiwan. The main tasks of the consortium are to develop teaching/research materials, hold faculty and academia-industry forums, host workshops and student summer camps, promote international collaboration, etc.

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Si2 (Silicon Integration Initiative) is the largest organization of industry-leading semiconductor, systems, EDA and manufacturing companies focused on the development and adoption of standards to improve the way integrated circuits are designed and manufactured, in order to speed time-to market, reduce costs, and meet the challenges of sub-micron design. Now in its 22nd year, Si2 is uniquely positioned to enable timely collaboration through dedicated staff and a strong implementation focus driven by its member companies. Si2 represents nearly 100 companies involved in all parts of the silicon supply chain throughout the world. See www.si2.org.

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Monday, November 8, 2010

	Registration - 7:00am - 6:00pm (Gateway Foyer) *Speaker's Breakfast - 7:30 - 8:30am (Donner/Siskiyou Ballroom)* *AV Practice Rooms - 7:00am - 6:00pm (Chardonnay, Riesling, Zinfandel)*			
9:00 AM — TO — 10:30 AM	***Opening Session & Award Presentation*** ***Keynote Address:*** *Multi-Scale Microscopy of the Nervous System: The Challenge of Imaging and Organizing Data Across Spatial Scales Spanning Twelve Orders of Magnitude - James C. Bouwer, Ph.D., Physicist and Principal Development Engineer, UCSD*			***(Oak Ballroom)***
	Break: 10:30 - 11:00am			
	Oak Ballroom	**Fir Ballroom**	**Pine Ballroom**	**Cedar Ballroom**
11:00 AM — TO — 12:30 PM	***Tutorial 1*** *Designing for Uncertainty: Addressing Process Variations and Aging Issues in Digital Systems*	***Session 1A*** *Fast and Accurate System Estimation, Evaluation, and Optimization*	***Session 1B*** *Manufacturing-Aware Design*	***Session 1C*** *Analog and Mixed Signal Verification and Optimization*
	Lunch: 12:30 - 1:30pm (Siskiyou Ballroom)			
2:00 PM — TO — 4:00 PM	***Tutorial 2*** *Reliability Analysis and Optimization at System-Level: A Straddle Between Complexity and Accuracy*	***Session 2A*** *Design-Aware Manufacturing*	***Session 2B*** *Advances in Embedded Systems and FPGA Synthesis*	***Session 2C*** *Enhancing Test for Delays and Opens Under Power Sensitive Conditions*
	Break: 4:00 - 4:30pm			
4:30 PM — TO — 6:00 PM	***Tutorial 3*** *Analog Challenges in Nanometer CMOS and Digitalization of Analog Functionality*	***Session 3A*** *Advanced Scheduling for Memory Systems*	***Session 3B*** *Making Critical Decision on Power in Physical Synthesis*	***Session 3C*** *Advances in Yield and Quality Analysis*

ACM/SIGDA Member Meeting: 6:30pm (Donner Ballroom) - Invited Speaker: Scott Kirkpatrick, *The Hebrew University of Jerusalem*

Tuesday, November 9, 2010

	Registration - 7:00am - 6:00pm (Gateway Foyer) *Speaker's Breakfast - 7:30 - 8:30am (Donner/Siskiyou Ballroom)* *AV Practice Rooms - 7:00am - 6:00pm (Chardonnay, Riesling, Zinfandel)*			
	Oak Ballroom	**Fir Ballroom**	**Pine Ballroom**	**Cedar Ballroom**
8:30 AM — TO — 10:00 AM	***Tutorial 4*** *System-Level Design - An Industrial Perspective*	***Session 4A*** *Design Optimization for Power-Efficient Synchronous and Asynchronous Systems*	***Session 4B*** *Improving Simulation Performance*	***Session 4C*** *Advances in Global Routing*
Break: 10:00 - 10:30am				
10:30 AM — TO — 12:00 PM	***Tutorial 4 (cont.)*** *System-Level Design - An Industrial Perspective*	***Session 5A*** *System-Level Static and Dynamic Low Power Design*	***Designer Track*** *Wrapping Up Design Successfully: Sign-Off, Verification, Debug*	***Session 5B*** *Leveraging Logics, Wire and 3-D for Physical Synthesis*
Lunch Presentation 12:00 - 1:15pm (Donner/Siskiyou Ballroom) ***Semiconductor and EDA Industry - A New Business Model - Lucio Lanza - Lanza TechVentures***				*Sponsored By:* CEDA
1:30 PM — TO — 3:30 PM	***Tutorial 5*** *Beyond-Die Designs: Solutions and Challenges*	***Session 6A*** *Advances in Biological and Post-CMOS Systems*	***Session 6B*** *Pushing Clock Distribution Performance*	***Session 6C*** *3-D-ICs and Detection of Faults and Hardware Trojans*
Break: 3:30 - 4:00pm				
4:00 PM — TO — 6:00 PM	***Tutorial 6*** *Organic Electronics*	***Session 7A*** *Advances in Timing Analysis*	***Session 7B*** *Parallel Methods for Power Grid and Interconnect Analysis*	***Session 7C*** *Physical Design for Manufacturability and Variability*
ICCAD Reception: 6:00pm (Gateway Foyer)				

Wednesday, November 10, 2010

	Registration - 7:30am - 4:00pm (Gateway Foyer) *Speaker's Breakfast - 7:30 - 8:30am (Donner/Siskiyou Ballroom)* *AV Practice Rooms - 7:00am - 4:00pm (Chardonnay, Riesling, Zinfandel)*			
	Oak Ballroom	**Fir Ballroom**	**Pine Ballroom**	**Cedar Ballroom**
8:30 AM — TO — 10:00 AM	***Tutorial 7*** *Digital Microfluidic Biochips: A Vision for Functional Diversity and More than Moore*	***Session 8A*** *Advance in Core Logic Synthesis*	***Session 8B*** *Routing - Theory and Practice*	***Session 8C*** *Power Optimization from Systems to Circuits*
Break: 10:00 - 10:30am				
10:30 AM — TO — 12:30 PM	***Tutorial 7 (cont.)*** *Digital Microfluidic Biochips: A Vision for Functional Diversity and More than Moore*	***Session 9A*** *Algorithms for Placement: Full House*	***Session 9B*** *Analysis and Algorithms for Design and Test in 3-D and Many-Core Systems*	***Session 9C*** *Advanced Analysis of Circuit/ Device Reliability*
Lunch: 12:30 - 1:30pm (Donner/Siskiyou Ballroom)				
2:00 PM — TO — 4:00 PM	***Tutorial 8*** *Manufacturing, CAD and Thermal-Aware Architectures for 3-D MPSoCs*	***Session 10A*** *Advanced Applications of Logic Synthesis*	***Session 10B*** *Advances in Verification*	***Session 10C*** *Recent Advances in Power Grid and Interconnect Analysis*

Opening Session & Keynote Address

9:00 - 10:30am • Oak Ballroom

OPENING REMARKS

Louis Scheffer - **General Chair** - *Janelia Farms Research Campus Howard Hughes Medical Institute*

AWARD PRESENTATIONS

IEEE/ACM William J. McCalla ICCAD Best Paper Award

This award is given in memory of William J. McCalla for his contributions to ICCAD and his CAD technical work throughout his career.

SimPL: An Effective Placement Algorithm

Myung-Chul Kim, Dong-Jin Lee and Igor L. Markov - *Univ. of Michigan, Ann Arbor, MI*

IEEE CEDA Early Career Award

Luca Daniel - *Massachusetts Institute of Technology, Cambridge, MA*
For outstanding contributions towards electromagnetic field analysis, parasitic variation-aware extraction and automated parameterized linear and nonlinear stable model reduction.

2010 SIGDA Pioneering Achievement Award

Scott Kirkpatrick - *The Hebrew Univ. of Jerusalem, Jerusalem, Israel*
For his contributions to stochastic optimization, especially simulated annealing, a key element of many modern design automation tool.

Multi-Scale Microscopy of the Nervous System: The Challenge of Imaging and Organizing Data Across Spatial Scales Spanning Twelve Orders of Magnitude

James C. Bouwer, Ph.D., *Physicist and Principal Development Engineer, University of California, San Diego*

Experimental advances of the past few decades have given the individual neuroscientist an increasingly powerful arsenal of tools for obtaining new information, extending from molecular structures to the entire nervous system. Scientists have begun the arduous and challenging process of adapting and assembling neuroscience data at all scales of resolution and across disciplines into computerized databases and other easily accessed sources. These multi-scale brain anatomy databases will complement the vast structural and sequence databases created to catalogue, organize and analyze gene sequences and protein products.

A general premise underlying several movements in modern brain research is that with accomplishments like "complete" knowledge of the genomes, solutions of all protein structures, determination of the functioning of key subcellular structures and a map or wiring diagram of the connections of the nervous system - we will next require an information infrastructure that facilitates cooperative assembly of these different forms of data.

Multi-Scale Microscopy of the Nervous System: The Challenge of Imaging and Organizing Data Across Spatial Scales Spanning Twelve Orders of Magnitude

The ability to explore such a multi-scale composite of knowledge about the brain can be expected to facilitate derivation of new understanding of how the components of the nervous system provide a basis for its complex properties.

Our U.C. San Diego-based group has been leading several interdisciplinary projects central to this grand challenge. While our main goal at the National Center for Microscopy and Imaging Research in San Diego (NCMIR) is to develop advanced technologies which deliver new fundamental understanding of structures on the scale of 1 nm to 100's of µm, a dimensional range that encompasses macromolecular complexes, organelles, and multi-component structures like synapses and key cellular interactions, we have also developed an information infrastructure that is intended to allow these microscopy derived data to be placed in the context of the complex organization of entire nervous systems.

For example, we have developed information systems such as the Whole Brain Catalog and Cell-Centered Database that are tools for mapping molecular and cellular brain anatomy into shared multi-scale mouse brain atlases and databases. To help populate these computerized multi-scale data repositories, our group at NCMIR has developed and disseminated many new molecular labeling methods which allow the same specimens to be examined with both advanced ultra-wide field laser-scanning light microscopy and multi-resolution 3-dimensional electron microscopy methods, like electron tomography. These new labeling and imaging methods are being used to help produce correlated light and electron microscopic data that then flow into the whole brain catalog and its associated databases and neuroscience information frameworks.

Results of research projects where spanning scales has changed previously held views about elements of the nervous system will be presented to illustrate the value of multi-scale anatomical approaches. Examples of how these multi-scale microanatomical frameworks are being used with computer simulations tools to test basic of hypotheses about mechanisms for functioning of the nervous system will also be provided.

In 2000, Dr. Bouwer joined Mark Ellisman's Laboratory, The National Center for Microscopy and Imaging Research (NCMIR). The National Institute of Health (NIH) established National Center for Microscopy and Imaging Research is an internationally acclaimed technology development center and a widely used research resource that develops new technologies and provides researchers with access to many of the most advanced imaging technologies. Dr. Bouwer helped with the launch the development of the NIH Biomedical Informatics Research Network (BIRN) linking major neuroimaging research centers throughout the U.S. BIRN has been a model for multi-disciplinary, multi-investigator collaborations and data-sharing.

In 2002, Dr. Bouwer received his Ph.D. in physics from UCSD for his work in Preparation, Theory, and Biological Applications of Highly Luminescent CdSe/ZnS Quantum Dots in Optical and Electron Microscopy. This early work pioneered the use of quantum dots as biological markers for proteins and anti-bodies for both electron and light microscopy. Since then, he has worked as a professional research scientist at UCSD, leading the instrumentation team at the NCMIR under the mentorship of Dr. Mark Ellisman.

11:00am - 12:30pm Fir Ballroom

SESSION 1A • FAST AND ACCURATE SYSTEM ESTIMATION, EVALUATION, AND OPTIMIZATION

Moderators: Sung Kyu Lim - *Georgia Institute of Technology*
Hao Yu - *Nanyang Technological Univ.*

This session starts with two papers on fast and high fidelity estimation and evaluation of system performance for power and performance optimization. The first paper presents several metrics to measure the fidelity of an estimation model that is used in design space exploration of System-on-Chip. The second paper proposes a hybrid system evaluation methodology for fixed-power systems that combines system simulation and analytical models for faster evaluation. This session concludes with a scheduling work that improves performance yield of systems under process variation.

1A.1ß FIDELITY METRICS FOR ESTIMATION MODELS
Haris Javaid, Aleksander Ignjatovic, Sri Parameswaran - *Univ. of New South Wales*

1A.2 FAST PERFORMANCE EVALUATION OF FIXED-POINT SYSTEMS WITH UN-SMOOTH OPERATORS
Karthick Parashar, Daniel Menard, Romuald Rocher, Olivier Sentieys, - *INRIA*
David Novo, Francky Catthoor - *IMEC*

1A.3 VARIATION-AWARE LAYOUT-DRIVEN SCHEDULING FOR PERFORMANCE YIELD OPTIMIZATION
Deming Chen , Gregory Lucas - *Univ. of Illinois at Urbana-Champaign*

11:00am - 12:30pm Pine Ballroom

SESSION 1B • MANUFACTURING-AWARE DESIGN

Moderator: Azadeh Davoodi - *Univ. of Wisconsin*

This short session discusses four interesting approaches to bridge the gap between design and manufacturing. The first two papers talk about the timely topic of double patterning lithography (DPL). The first paper discusses implications of DPL on SRAM bitcell design while the second paper proposes wire spreading as an approach to reduce coloring conflicts in DPL. The third paper gives an interesting analysis to show how maximizing information density rather than bit density may be a better SRAM design approach. The final paper of the session extends the Virtual Probe approach for variation characterization to efficiently account for wafer-to-wafer variations.

1B.1 ANALYSIS AND OPTIMIZATION OF SRAM ROBUSTNESS FOR DOUBLE PATTERNING LITHOGRAPHY
Vivek Joshi - *Univ. of Michigan*
Kanak Agarwal - *IBM Corp.*
Dennis Sylvester, David Blaauw - *Univ. of Michigan*

1B.2 WISDOM: WIRE SPREADING ENHANCED DECOMPOSITION OF MASKS IN DOUBLE PATTERNING LITHOGRAPHY
Kun Yuan , David Z. Pan - *Univ. of Texas, Austin*

1B.3S MAXIMUM-INFORMATION STORAGE SYSTEM: CONCEPT, IMPLEMENTATION AND APPLICATION
Xin Li - *Carnegie Mellon Univ.*

1B.4S MULTI-WAFER VIRTUAL PROBE: MINIMUM-COST VARIATION CHARACTERIZATION BY EXPLORING WAFER-TO-WAFER CORRELATION
Wangyang Zhang - *Carnegie Mellon Univ.*
Xin Li - *Carnegie Mellon Univ.*
Emrah Acar - *IBM T.J. Watson Research Ctr.*
Frank Liu - *IBM Corp.*
Rob Rutenbar - *Univ. of Illinois at Urbana-Champaign*

11:00am - 12:30pm Cedar Ballroom

SESSION 1C • ANALOG AND MIXED SIGNAL VERIFICATION AND OPTIMIZATION

Moderator: L. Miguel Silveira - *Cadence Research Labs, INESC-ID/IST - TU Lisbon*

The papers in this session provide new ideas for analog and mixed/signal design, analysis and optimization. The first paper addresses the problem of design verification by proposing a semi-formal equivalence checking procedure between behavioral and electrical descriptions. The second paper uses modeling error to improve model fitting and feasibility while meeting constraint targets. The third paper provides a new approach for constructing determinant decision diagrams for symbolic analysis.

1C.1 ON BEHAVIORAL MODEL EQUIVALENCE CHECKING FOR LARGE ANALOG/MIXED SIGNAL SYSTEMS
Amandeep Singh, Peng Li - *Texas A&M Univ.*

1C.2 AN ALGORITHM FOR EXPLOITING MODELING ERROR STATISTICS TO ENABLE ROBUST ANALOG OPTIMIZATION
Michael Orshansky, Mario Lok, Constantine Caramanis, Ashish Kumar Singh, Kareem Ragab - *Univ. of Texas, Austin*

1C.3 A SIMPLE IMPLEMENTATION OF DETERMINANT DECISION DIAGRAM
Guoyong Shi - *Shanghai Jiao Tong Univ.*

11:00am - 12:30pm Oak Ballroom

TUTORIAL 1 • DESIGNING FOR UNCERTAINTY: ADDRESSING PROCESS VARIATIONS AND AGING ISSUES IN DIGITAL SYSTEMS

Moderator: Diana Marculescu - *Carnegie Mellon Univ.*

Driven by aggressive technology scaling and sub-wavelength lithography, there has been a marked increase in the variability of process technology parameters. In addition, due to increased power density and stricter thermal envelopes, environmental parameter variability (e.g., temperature and voltage variation) and their impact on system lifetime increase as well.

Regardless of its source or manifestation, such design uncertainty poses a major challenge in designing complex integrated systems due to increased performance variability, and decreased reliability and system lifetime of logic and memory. Variability-aware and system lifetime-aware design methodologies are needed for all levels of abstraction.

Existing approaches target variability at the circuit/gate/layout level and do not provide sufficient leverage since they do not provide capabilities that can be easily used at higher levels of abstraction, where much of the overall optimization can be done more effectively.

This tutorial will give an overview of the most important aspects of variability and aging at physical, environmental, and circuit levels of abstraction. It will also describe system-level design methodologies capable of capturing these effects at the micro-architecture and architecture levels for both performance and power.

AGING ANALYSIS AT GATE AND MACRO CELL LEVEL
Ulf Schlichtmann, Dominik Lorenz, Martin Barke - *Technische Univ. München*

RESILIENT MICROPROCESSOR DESIGN FOR IMPROVING PERFORMANCE AND ENERGY EFFICIENCY
Keith A. Bowman, James W. Tschanz - *Intel Corp.*

PROCESS VARIATION AWARE PERFORMANCE MODELING AND DYNAMIC POWER MANAGEMENT FOR MULTICORE SYSTEMS
Siddharth Garg, **Diana Marculescu** - *Carnegie Mellon Univ.*
Sebastian X. Herbert - *DC Energy*

Monday, November 8, 2010

2:00 - 4:00pm Fir Ballroom

SESSION 2A • DESIGN-AWARE MANUFACTURING

Moderator: Minsik Cho - *IBM Corp.*

This session discusses several new design-aware and process-aware mask methodologies. The first three papers discuss design-aware mask optimization and inspection. Specifically, they propose a mask inspection technique considering design sensitivity, a mask perturbation methodology to improve manufacturability, and a template mask methodology to reduce mask costs. The fourth paper presents a fast layout decomposition technique for double patterning lithography (DPL). The last paper presents a process monitor methodology to reduce back-end manufacturing costs.

2A.1 DESIGN-AWARE MASK INSPECTION
Abde Ali Kagalwalla, Puneet Gupta - *Univ. of California, Los Angeles*
Chris Progler, Steve McDonald - *Photronics, Inc.*

2A.2 SMATO: SIMULTANEOUS MASK AND TARGET OPTIMIZATION FOR IMPROVING LITHOGRAPHIC PROCESS WINDOW
Shayak Banerjee - *Univ. of Texas, Austin*
Kanak Agarwal - *IBM Corp.*
Michael Orshansky - *Univ. of Texas, Austin*

2A.3 TEMPLATE-MASK DESIGN METHODOLOGY FOR DOUBLE PATTERNING TECHNOLOGY
Chin-Hsiung Hsu, Yao-Wen Chang- *National Taiwan Univ.*
Sani Nassif - *IBM Corp.*

2A.4S FAST AND LOSSLESS GRAPH DIVISION METHOD FOR LAYOUT DECOMPOSITION USING SPQR-TREE
Wai-Shing Luk - *Fudan Univ.*
Huiping Huang - *Cadence Design Systems, Inc.*

2A.5S DESIGN DEPENDENT PROCESS MONITORING FOR BACK-END MANUFACTURING COST REDUCTION
Tuck-Boon Chan, Aashish Pant, Lerong Cheng, Puneet Gupta - *Univ. of California, Los Angeles*

2:00 - 4:00pm Pine Ballroom

SESSION 2B • ADVANCES IN EMBEDDED SYSTEMS AND FPGA SYNTHESIS

Moderator: Swamy Muddu - *GLOBALFOUNDRIES*

This session presents four papers that advance the state-of-the-art in multi-core embedded systems design and FPGA Synthesis. The first paper proposes new state space models and Monte Carlo simulation techniques to provide stochastic estimations of execution time instead of relying on worst-case estimates. The second and third paper propose new theoretical techniques for adaptive and real-time dynamic frequency and voltage scaling of embedded multi-core systems. The fourth paper proposes a new way to decompose FPGA look-up tables to improve the robustness of the FPGA logic fabric.

2B.1ß SETS: STOCHASTIC EXECUTION TIME SCHEDULING FOR MULTICORE SYSTEMS BY JOINT STATE SPACE AND MONTE CARLO
Nabeel Iqbal, Jörg Henkel - *Karlsruhe Institute of Technology*

2B.2 COMBINING OPTIMISTIC AND PESSIMISTIC DVS SCHEDULING: AN ADAPTIVE SCHEME AND ANALYSIS
Simon Perathoner - *ETH Zürich*
Jian-Jia Chen - *Karlsruhe Institute of Technology*
Nikolay Stoimenov, Lothar Thiele, Kai Lampka - *ETH Zürich*

2B.3 UNIFIED THEORY OF REAL-TIME TASK SCHEDULING AND DYNAMIC VOLTAGE/FREQUENCY SCALING ON MPSOCS
Hessam Kooti, Eli Bozorgzadeh - *Univ. of California, Irvine*

2B.4 IN-PLACE DECOMPOSITION FOR ROBUSTNESS IN FPGA
Ju-Yueh Lee, Zhe Feng, Lei He - *Univ. of California, Los Angeles*

2:00 - 4:00pm Cedar Ballroom

SESSION 2C • ENHANCING TEST FOR DELAYS AND OPENS UNDER POWER-SENSITIVE CONDITIONS

Moderator: Suriyaprakash Natarajan - *Intel Corp.*

This session presents four papers which focus on the test of power-sensitive circuits for delays and opens. The first paper presents a method for reducing switching activity and maximizing fault coverage though intelligent partitioning of scan chains. The second paper proposes a framework for detecting stuck-open faults on power switches used in MTCMOS circuits where multiple thresholds to enable the moderation of power consumption via gating. The third paper presents an analysis of IR-drop that includes modeling the power grid. The last paper presents novel methods for selecting traced signals to determine the root cause of timing failures in the presence of power droop.

2C.1 MVP: CAPTURE-POWER REDUCTION WITH MINIMUM-VIOLATIONS PARTITIONING FOR DELAY TESTING
Zhen Chen - *Tsinghua Univ.*
Krishnendu Chakrabarty - *Duke Univ.*
Dong Xiang - *Tsinghua Univ.*

2C.2 TESTING METHODS FOR DETECTING STUCK-OPEN POWER SWITCHES IN COARSE-GRAIN MTCMOS DESIGNS
Szu-Pang Mu, Willy Wang, Hao-Yu Yang, Mango Chao - *National Chiao Tung Univ.*
Shi-Hao Chen, Chih-Mou Tseng, Tsung-Ying Tsai - *Global Unichip Corp.*

2C.3 A SCALABLE QUANTITATIVE MEASURE OF IR-DROP EFFECTS FOR SCAN PATTERN GENERATION
Meng-Fan Wu - *National Taiwan Univ.*
Kun-Han Tsai, Wu-Tung Cheng - *Mentor Graphics Corp.*
Hsin-Cheih Pan, **Jiun-Lang Huang,** - *National Taiwan Univ.*
Augusli Kifli - *Faraday Technology Corp.*

2C.4 TRACE SELECTION FOR IMPROVING TIMING AND LOGIC VISIBILITY FOR POST-SILICON VALIDATION
Hamid Shojaei, Azadeh Davoodi - *Univ. of Wisconsin*

2:00 - 4:00pm Oak Ballroom

TUTORIAL 2 • RELIABILITY ANALYSIS AND OPTIMIZATION AT SYSTEM-LEVEL: A STRADDLE BETWEEN COMPLEXITY AND ACCURACY

Moderator: Jürgen Teich - *Univ. of Erlangen-Nuremberg*

Ever shrinking device structures and the rapidly growing number of system makes system level reliability analysis and optimization mandatory. A prerequisite to find a reasonable trade-off between reliability and other design objectives is an understanding of the complexity of the mathematical models typically applied at system level and, at the same time, a detailed knowledge about the physical mechanisms that cause component failures during both manufacturing and operation. This makes system level reliability analysis and optimization a multi-disciplinary task. However, reliability analysis as an enabler to introduce reliability-increasing techniques efficiently raises two important questions for the designer:

(1) How to appropriately model and quantify the significant causes of failures at system level where significant design decisions typically made at lower levels may not be even taken?

(2) How to handle the complexity of reliability analysis at system level where a system may be composed of hundreds or thousands of components and subsystems?

In this tutorial, we will cover the key concepts and state-of-the-art methodologies for reliability analysis and optimization at system level. A special emphasis is put on how efficient system level models that aim to cope with the complexity may interact with models to quantify the effects of physical causes of failure applied at lower levels of abstraction. We will give a bottom up survey of the state-of-the-art for a wide range of aspects including symbolic system level analysis, efficient analysis of thermal effects on reliability, design of error-resilient components, and the impact of design variability on system level reliability analysis.

SYSTEM-LEVEL IMPACT OF CHIP-LEVEL FAILURE MECHANISMS AND SCREENS
Anne Gattiker - *IBM Corp.*

CROSS-LAYER ERROR RESILIENCE FOR ROBUST SYSTEMS
Larkhoon Leem, Hyungmin Cho, Hsiao-Heng Lee, Young Moon Kim, Yanjing Li, **Subhasish Mitra** - *Stanford Univ.*

RELIABILITY, THERMAL, AND POWER MODELING AND OPTIMIZATION
Robert Dick - *Univ. of Michigan*

SYMBOLIC SYSTEM-LEVEL RELIABILITY ANALYSIS
Michael Glass, Martin Lukasiewycz, Felix Reimann, Christian Haubelt, Jürgen Teich - *Univ. of Erlangen-Nuremberg*

Monday, November 8, 2010

4:30 - 6:00pm Fir Ballroom

SESSION 3A • ADVANCED SCHEDULING FOR MEMORY SYSTEMS

Moderators: Deming Chen - *Univ. of Illinois at Urbana-Champaign*
Sung Kyu Lim - *Georgia Institute of Technology*

This session presents scheduling works that achieve performance and power-efficient usage in various memory systems. The first paper proposes a hierarchical memory scheduling policy to minimize interferences among requests in Multimedia Multi-Processor System-on-Chip. The second paper applies so called Credit-Borrow-and-Repay technique from the networking community for multi-port DRAM sharing. The last paper presents a 3-stage ILP-based scheduling work for scratchpad memory system in embedded processors for code overlay overhead minimization.

3A.1 HIERARCHICAL MEMORY SCHEDULING FOR MULTIMEDIA MPSOCS
Ye-Jyun Lin, Chia-Lin Yang, Jiao-Wei Huang - *National Taiwan Univ.*
Tay-Jyi Lin - *Industrial Technology Research Institute*
Jiao-Wei Huang - *National Taiwan Univ.*
Naehyuck Chang - *Seoul National Univ.*

3A.2 CREDIT BORROW AND REPAY: SHARING DRAM WITH MINIMUM LATENCY AND BANDWIDTH GUARANTEES
Zefu Dai, Mark Jarvin, Jianwen Zhu - *Univ. of Toronto*

3A.3 SCHEDULING OF SYNCHRONOUS DATA FLOW SPECIFICATIONS ON SCRATCHPAD MEMORY BASED EMBEDDED PROCESSORS
Weijia Che, Karam S. Chatha - *Arizona State Univ.*

4:30 - 6:00pm Pine Ballroom

SESSION 3B • MAKING CRITICAL DECISION ON POWER IN PHYSICAL SYNTHESIS

Moderators: Gi-Joon Nam - *IBM Corp.*
Lars Hagen - *Cadence Design Systems, Inc.*

Several novel ideas for power minimization in physical synthesis optimization will be presented in this session. The session starts with the fast and optimal peak power density minimization idea for voltage partitioning applications where an elegant binary search-based algorithm is devised. The second paper demonstrates that the significant power saving is possible even under density/timing constraints during post-placement optimization with multi-bit flip-flops. The final paper reveals interesting relationship between power optimization and fault-tolerancy in FPGA physical synthesis, showing great promise for co-optimization of power and reliability in FPGA CAD systems.

3B.1 THE FAST OPTIMAL VOLTAGE PARTITIONING ALGORITHM FOR PEAK POWER DENSITY MINIMIZATION
Jia Wang, **Shiyan Hu** - *Michigan Technological Univ.*

3B.2 POST-PLACEMENT POWER OPTIMIZATION WITH MULTI-BIT FLIP-FLOPS
Yao-Tsung Chang, Chih-Cheng Hsu, Mark Po-Hung Lin - *National Chung Cheng Univ.*
Yu-Wen Tsai , Sheng-Fong Chen - *Faraday Technology Corp.*

3B.3 ON POWER AND FAULT-TOLERANT OPTIMIZATION IN FPGA PHYSICAL SYNTHESIS
Manu Jose - *Univ. of California, Los Angeles*
Yu Hu - *Univ. of Alberta*
Rupak Majumdar - *Univ. of California, Los Angeles*

4:30 - 6:00pm Cedar Ballroom

SESSION 3C • ADVANCES IN YIELD AND QUALITY ANALYSIS

Moderator: Haluk Konuk - *Broadcom Corp.*

This session presents three papers which enhance analysis of yield and test quality for memories and analog circuits. The first paper presents a means of sharing redundant resources in 3-D memory architectures to maximize yield. The second paper presents a mathematical model for estimating yield--bypassing the need for expensive simulation. Finally, the third paper introduces a statistical method for estimating analog test metrics (i.e. test escapes and yield loss) for alternate tests with parts-per-million accuracy prior to production.

3C.1ß YIELD ENHANCEMENT FOR 3-D-STACKED MEMORY BY REDUNDANCY SHARING ACROSS DIES
Li Jiang, Rong Ye, **Qiang Xu** - *The Chinese Univ. of Hong Kong*

3C.2 MATHEMATICAL YIELD ESTIMATION FOR TWO-DIMENSIONAL-REDUNDANCY MEMORY ARRAYS
Mango Chao, **Ching-Yu Chin**, Chen-Wei Lin - *National Chiao Tung Univ.*

3C.3 ANALOG TEST METRICS ESTIMATES WITH PPM ACCURACY
Haralampos-G. Stratigopoulos, Salvador Mir - *TIMA Laboratory/CNRS*

4:30 - 6:00pm Oak Ballroom

TUTORIAL 3 • ANALOG CHALLENGES IN NANOMETER CMOS AND DIGITALIZATION OF ANALOG FUNCTIONALITY

Moderator: Stephan Henzler - *Infineon Technologies AG*

Analog integrated circuits are a key component in many mixed-signal systems. Their design complexity, however, poses serious challenges in terms of design and verification productivity. This tutorial presents recent developments in this area.

It first reviews state-of-the-art techniques for automated design of analog circuits. Recently developed extensions towards the hierarchical design of larger building blocks and towards considering the growing variability and growing impact of time-dependent degradation phenomena such as NBTI on the performance and lifetime of analog integrated circuits will be described. Now that CMOS transistors have clearly demonstrated the ability to operate with high performance at mm-wave frequencies, there has been significant recent interest in leveraging the 60GHz band to enable multi-Gb/s wireless communications, e.g., for embedding low-cost, multi-Gb/s transceivers for file transfer and data synchronization into mobile devices such as smart-phones and digital cameras. However, realizing this scenario requires complete transceivers that dissipate roughly an order of magnitude lower power than current designs without sacrificing throughput.

The second part will discuss how to substantially improve transceiver energy-efficiency by utilizing simple modulation schemes with broadband mixed-signal circuits performing the majority of the high-speed signal processing. Mixed-signal circuit design in nanometer technologies becomes increasingly challenging due to reduced intrinsic transistor gain, diminishing voltage head-room, and variations. Digital assist techniques, however, help to circumvent these challenges. Calibration techniques or advanced system architectures such as the non-binary successive approximation ADCs are early but successful examples. The move from the voltage to the time-domain is a recent approach to take best advantage from technology scaling, to overcome parasitic analog effects, and to enable completely new functionality.

In the third part, the reason for the push to the time domain is explained. The most important TDC applications are introduced and compared to their analog counterpart. TDC fundamentals, design challenges and latest results are discussed.

DESIGN AUTOMATION TOWARDS RELIABLE ANALOG INTEGRATED CIRCUITS
Georges Gielen, Elie Maricau, Pieter De Wit - *Katholieke Univ. Leuven*

ENERGY-EFFICIENT 60GHZ WIRELESS TRANSCEIVER DESIGN
Elad Alon - *Univ. of California, Berkeley*

DIGITALIZATION OF MIXED-SIGNAL IN NANOMETER TECHNOLOGIES
Stephan Henzler - *Technische Univ. München*

ACM/SIGDA Member Meeting

6:30 - 8:30pm
Donner Ballroom

2010 SIGDA Pioneering Achievement Award Recipient

INVITED SPEAKER: Scott Kirkpatrick, *The Hebrew Univ. of Jerusalem*

Please join us for dinner and an entertaining talk by Scott Kirkpatrick, a pioneer in stochastic optimization. Simulated annealing, a key element of many modern design automation tools, has its roots in the early work done by Kirkpatrick's group at IBM.

Please join us!

Meetings at ICCAD

Sunday, November 7

The ACM/SIGDA CADathlon
7:30am – 5:00pm
Donner Ballroom

Monday, November 8

ACM/SIGDA Member Meeting
6:30 -8:30pm
Donner Ballroom

48th DAC Technical Program Committee Meeting
6:30 - 8:30pm
Siskiyou Ballroom

Tuesday, November 9

48th DAC Exhibitor Meeting
3:00pm
Carmel Room

Wednesday, November 10

EDAC Emerging Companies Committee
6:30 – 10:00pm
Oak Ballroom

8:30 - 10:00am Fir Ballroom

SESSION 4A • DESIGN OPTIMIZATION FOR POWER-EFFICIENT SYNCHRONOUS AND ASYNCHRONOUS SYSTEMS

Moderator: Sung Kyu Lim - *Georgia Institute of Technology*

This session begins with two papers on low power Network-on-Chip (NOC). The first paper presents a virtual channel failure metric to capture the impact of virtual channels on the power and performance profile of NoC. The second paper proposes a Lagrangian relaxation-based simultaneous task and voltage scheduling algorithm for energy minimization in NoC. The third paper presents a methodology that characterizes aging-duty cycle and aging-supply voltage relationships to minimize power consumption and task execution time. The last paper presents a branch-and-bound-based scheduling algorithm for asynchronous systems under latency, area, energy, and power constraints.

4A.1 EFFICIENT TRACE-DRIVEN METAHEURISTICS FOR OPTIMIZATION OF NETWORKS-ON-CHIP CONFIGURATIONS
Andrew B. Kahng, Bill Lin, **Kambiz Samadi**, Rohit Sunkam Ramanujam - *Univ. of California, San Diego*

4A.2 A SELF-EVOLVING DESIGN METHODOLOGY FOR POWER EFFICIENT MULTI-CORE SYSTEMS
Jin Sun, - *Univ. of Arizona*
Rui Zheng, Jyothi Velamala, Yu Cao - *Arizona State Univ.*
Roman Lysecky, Karthik Shankar, **Janet Roveda** - *Univ. of Arizona*

4A.3S AN ENERGY AND POWER-AWARE APPROACH TO HIGH-LEVEL SYNTHESIS OF ASYNCHRONOUS SYSTEMS
John Hansen , Montek Singh - *Univ. of North Carolina, Chapel Hill*

4A.4S CLUSTERING-BASED SIMULTANEOUS TASK AND VOLTAGE SCHEDULING FOR NOC SYSTEMS
Yifang Liu - *Google Inc.*
Yu Yang, **Jiang Hu** - *Texas A&M Univ.*

8:30 - 10:00am Pine Ballroom

SESSION 4B • IMPROVING SIMULATION PERFORMANCE

Moderators: L. Miguel Silveira - *Cadence Research Labs, INESC-ID/IST - TU Lisbon*
Ting Mei - *Sandia National Labs*

The papers in this session address the issue of simulation performance. The first two papers consider macromodeling as a way to improve simulation efficiency and extend concepts from oscillator analysis to more general systems. The first paper extends the notion of timing/phase macromodels to general oscillatory and non-oscillatory systems. The second paper extends the notion of phase equations to quasi-periodic systems. The last paper considers runtime adaption for improving the efficiency of multi-algorithm parallel simulation.

4B.1ß GENERALIZED NONLINEAR TIMING/PHASE MACROMODELING: THEORY, NUMERICAL METHODS AND APPLICATIONS
Chenjie Gu, Jaijeet Roychowdhury - *Univ. of California, Berkeley*

4B.2 PHASE EQUATIONS FOR QUASI-PERIODIC OSCILLATORS
Alper Demir - *Koç Univ.*
Chenjie Gu, Jaijeet Roychowdhury - *Univ. of California, Berkeley*

4B.3 ON-THE-FLY RUNTIME ADAPTATION FOR EFFICIENT EXECUTION OF PARALLEL MULTI-ALGORITHM CIRCUIT SIMULATION
Xiaoji Ye, Peng Li - *Texas A&M Univ.*

8:30 - 10:00am Cedar Ballroom

SESSION 4C • ADVANCES IN GLOBAL ROUTING

Moderators: Patrick Groeneveld - *Magma Design Automation, Inc.*
Mustafa Ozdal - *Intel Corp.*

This session focuses on the recent advances in global routing. In the first presentation, a novel pre-processing technique is proposed to resolve congestion hot-spots efficiently by pre-determining the detours. The second presentation focuses on the antenna avoidance problem, and shows that antenna violations can be reduced significantly when considered during global routing. The third presentation proposes an approach for global routing, where the runtime advantages of 2-D routing are maintained while 3-D layer constraints for critical nets are considered.

4C.1 AN AUCTION BASED PRE-PROCESSING TECHNIQUE TO DETERMINE DETOUR IN GLOBAL ROUTING
Yue Xu, Chris Chu - *Iowa State Univ.*

4C.2 SIMULTANEOUS ANTENNA AVOIDANCE AND VIA OPTIMIZATION IN LAYER ASSIGNMENT OF MULTI-LAYER GLOBAL ROUTING
Tsung-Hsien Lee, Ting-Chi Wang - *National Tsing-Hua Univ.*

4C.3 GLADE: A MODERN GLOBAL ROUTER CONSIDERING LAYER DIRECTIVES
Yen-Jung Chang, Tsung-Hsien Lee, Ting-Chi Wang - *National Tsing-Hua Univ.*

8:30am - 12:00pm Oak Ballroom

TUTORIAL 4 • SYSTEM-LEVEL DESIGN - AN INDUSTRIAL PERSPECTIVE

Moderator: Guido Stehr - *Infineon Technologies AG*

The term system-level design does not mean a certain methodology, but refers to a variety of design techniques well above RTL. It is a vibrant and evolving area from a methodological point of view.

This tutorial dips into the topic from a variety of angles and examines what has arrived in the industrial practice. The tutorial starts off with an introductory overview presentation on transaction level modeling.

The following five focus presentations zoom in on particular aspects touched in the first talk and elaborate on them:

The first focus presentation discusses how standardization is key for the advancement of industrial-level system design methodologies.

The next talk shows how complex on-chip communication networks can be mastered through abstraction.

The third focus presentation discusses how low-power design starts at system-level. The particular challenges of parallel system design will be explained next.

The final presentation shows how to design application specific processors, which are a compromise between general purpose cores and custom hardware.

TRANSACTION LEVEL MODELING IN PRACTICE: MOTIVATION AND INTRODUCTION
Guido Stehr, Josef Eckmueller - *Infineon Technologies AG*

STANDARDS FOR SYSTEM-LEVEL DESIGN
Laurent Maillet-Contoz - *STMicroelectronics*

DESIGN SPACE EXPLORATION AND PERFORMANCE EVALUATION AT ELECTRONIC SYSTEM-LEVEL FOR NOC-BASED MPSOC
Soeren Sonntag, Francisco Gilabert - *Lantiq Deutschland GmbH*

ESL SOLUTIONS FOR LOW POWER DESIGN
Sylvian Kaiser, Ilija Materic, Rabih Saade - *DOCEA Power SAS*

HW/SW CO-DESIGN OF PARALLEL SYSTEMS
Enno Wein - *ProximusDA GmbH*

APPLICATION SPECIFIC PROCESSOR DESIGN
Achim Nohl, Frank Schirrmeister, **Drew Taussig** - *Synopsys, Inc.*

10:30am - 12:00pm Fir Ballroom

SESSION 5A • SYSTEM-LEVEL STATIC AND DYNAMIC LOW POWER DESIGN

Moderators: Karam Chatha - *Arizona State Univ.*
Sri Parameswaran - *Univ. of New South Wales*

The session includes three papers that address compiler oriented and memory access pattern based low power design approaches. The compiler oriented approaches address selective power gating of functional units in the context of reconfigurable and general purpose processors, respectively. Memory access pattern approach utilizes cache miss statistics for run time dynamic voltage frequency scaling.

5A.1ß SELECTIVE INSTRUCTION SET MUTING FOR ENERGY-AWARE ADAPTIVE PROCESSORS
Muhammad Shafique, Lars Bauer, Jörg Henkel - *Karlsruhe Institute of Technology*

5A.2 OPTIMAL ALGORITHM FOR PROFILE-BASED POWER GATING: A COMPILER TECHNIQUE FOR REDUCING LEAKAGE ON EXECUTION UNITS IN MICROPROCESSORS
Danbee Park - *Seoul National Univ.*
Nam Sung Kim, Jungseob Lee - *Univ. of Wisconsin*
Taewhan Kim - *Seoul National Univ.*

5A.3 MEMORY ACCESS AWARE ON-LINE VOLTAGE CONTROL FOR PERFORMANCE AND ENERGY OPTIMIZATION
Xi Chen, Chi Xu - *Univ. of Minnesota*
Robert P. Dick - *Univ. of Michigan*

10:30am - 12:00pm Cedar Ballroom

SESSION 5B • LEVERAGING LOGICS, WIRE AND 3-D FOR PHYSICAL SYNTHESIS

Moderators: Shiyan Hu - *Michigan Technological Univ.*
Gi-Joon Nam - *IBM Corp.*

The papers of this session address various topics related to physical synthesis. The first paper proposes a retiming-based transformation system that performs multiple optimizations simultaneously on large design partitions. The second paper proposes a post-mask ECO timing optimization flow consisting of resource-aware spare-cell selection and redundant-wire-aware ECO routing. The last paper in the session discusses the impact of TSV management and develops a 3-D physical design flow that controls the number of TSVs for performance improvement.

5B.1 SPIRE: A RETIMING-BASED PHYSICAL-SYNTHESIS TRANSFORMATION SYSTEM
David A. Papa - *IBM Corp., Univ. of Michigan*
Smita Krishnaswamy - *IBM Corp.*
Igor L. Markov - *Univ. of Michigan*

5B.2 REDUNDANT-WIRES-AWARE ECO TIMING AND MASK-COST OPTIMIZATION
Shao-Yun Fang - *National Taiwan Univ.*
Yao-Wen Chang, Tzuo-Fan Chien - *National Taiwan Univ.*

5B.3 THROUGH SILICON VIA MANAGEMENT DURING 3-D PHYSICAL DESIGN: WHEN TO ADD AND HOW MANY?
Mohit Pathak, Young-Joon Lee, Thomas Moon, Sung Kyu Lim - *Georgia Institute of Technology*

Tuesday, November 9, 2010

10:30am - 12:00pm Pine Ballroom

DESIGNER TRACK • WRAPPING UP DESIGN SUCCESSFULLY: SIGN-OFF, VERIFICATION, DEBUG

Moderator: Andreas Herkersdorf - *Technische Univ. München*

This session addresses important design flow issues from a practical point of view. The first talk discusses the burning problem of an analog and mixed-signal design flow with seamless propagation of the specification through abstraction levels and tools. It analyzes today's industrial design flow and proposes practical requirements for a specification-driven flow. The second talk's topic is assertion-based verification of digital designs. Using an AHB2Wishbone bus bridge, the talk presents how a verification plan and design specifications can be completed in practice. The third talk deals with designing chips such that bug hunting in silicon is facilitated. A structured process using formal methods for handling traces and fixing bugs is presented and illustrated in practice.

5D.1 INDUSTRY NEEDS A NEW MIXED SIGNAL DESIGN AND SIGN-OFF SIMULATION FLOW
Stephan Endrass, Matthias Arnold - *Texas Instruments, Inc.*

5D.2 HOW DO I KNOW I HAVE WRITTEN ENOUGH ASSERTIONS?
Anders Nordstrom - *OneSpin Solutions*

5D.3 FORMAL METHODS APPLIED IN POST-SILICON DEBUG
Lawrence Loh - *Jasper Design Automation, Inc.*

12:00 - 1:15pm Donner/Siskiyou Ballrooms

LUNCH PRESENTATION • SEMICONDUCTOR AND EDA INDUSTRY - A NEW BUSINESS MODEL

Organizer: **Shishpal Rawat** - *Intel Corp.*
Speaker: **Lucio Lanza** - *Lanza TechVentures*

EDA industry path to revenues beyond the $4 billion mark, where it has been stuck for its core technologies, will have to make some serious course corrections to surpass it. It is clear that to find growth again, the EDA industry needs to embrace new business models. As the cost of building ICs has ballooned the EDA industry has not done much to help new start ups reduce the cost of new design either via flexible software services or flexible manufacturing operations. New process nodes are coming on as fast as ever, but they are not ramping to use by mainstream chip designers nearly as fast due to the escalated costs. The traditional industry segments are holding on too long to their old business models. We will discuss how new business models may resurrect the chip design industry and create new focus areas for design and EDA professionals.

Sponsored by:

CEDA
Council on Electronic Design Automation

1:30 - 3:30pm Oak Ballroom

TUTORIAL 5 • BEYOND-DIE DESIGNS: SOLUTIONS AND CHALLENGES

Moderator: Yao-Wen Chang - *National Taiwan Univ.*

Due to the higher complexity and performance requirements in chip designs, the I/O count increases significantly, and thus more I/O signals come out of chips and run among chips, packages, and printed circuit boards (PCBs). How to complete the layout design and simultaneously satisfy various physical and electrical constraints for so many I/O signals has become a significant challenge to chip, package, and PCB designers.

This tutorial provides attendees state-of-the-art knowledge about the current industry practice and research and development for the designs of packages and PCBs and chip-package-board co-design, co-extraction, and co-simulation.

The tutorial will first describe the often overlooked design bottleneck of PCBs which are a significant cost element of the final product. This bottleneck can be greatly reduced by implementing a cross-domain co-design flow that considers the physical layout requirements of the package substrate, and the PCB in the context of planning the chip.

The tutorial will then describe the challenges that the industry encounters in moving towards a true cross-domain co-design platform, propose some possible solutions, and cover what leading companies are already doing today in the area of physical codesign. Then, recent research progress in the physical design of PCBs and packages and their codesign with chips will be treated; in particular, new models and algorithms for handling the individual- and codesign problems will be presented.

Finally, the growing electromagnetic coupling among chips, packages and PCBs, due to the ever-increasing system performance and integration density, will be described. With emphasis on power delivery network and high-speed signaling, existing solutions to estimate and model SI and PI for chip, package and PCB without completed designs are introduced, strategies to comodel and co-optimize chip, package and PCB for SI and PI are discussed, and pressing open challenges are identified.

BEYOND DIE DESIGN: BOARD DRIVEN I/O PLANNING & OPTIMIZATION
John F. Park - *Mentor Graphics Corp.*

RECENT RESEARCH DEVELOPMENT IN PCB LAYOUT
Tan Yan - *Synopsys, Inc., Univ. of Illinois at Urbana-Champaign*
Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign*

RECENT RESEARCH DEVELOPMENT IN FLIP-CHIP ROUTING
Hsu-Chieh Lee, **Yao-Wen Chang**, Po-Wei Lee - *National Taiwan Univ.*

MODELING AND DESIGN FOR BEYOND-THE-DIE POWER INTEGRITY
Yiyu Shi, **Lei He** - *Univ. of California, Los Angeles*

1:30 - 3:30pm Fir Ballroom

SESSION 6A • ADVANCES IN BIOLOGICAL AND POST-CMOS SYSTEMS

Moderators: Radu Zlatanovici - *Cadence Design Systems, Inc.*
Nishant Patil - *Stanford Univ.*

This session presents three papers describing recent advances in biological and post-CMOS systems. The first paper presents a synthesis approach for digital signal processing operations with DNA and demonstrates the methodology on digital filters. The second paper introduces pin-count reduction algorithm for microfluidic applications based on a two-step flow formulation procedure that minimizes pin-count and wirelength. The third paper provides a comprehensive survey and modeling of sensing circuits for spin-transfer torque random access memory (STT-RAM) and propose a voltage-driven sensing scheme to improve sense margin and yield.

6A.1 A SYNTHESIS FLOW FOR DIGITAL SIGNAL PROCESSING WITH BIOMOLECULAR REACTIONS
Hua Jiang, Aleksandra Kharam, Marc Riedel, Keshab Parhi - *Univ. of Minnesota*

6A.2 A NETWORK-FLOW BASED PIN-COUNT AWARE ROUTING ALGORITHM FOR BROADCAST ELECTRODE-ADDRESSING EWOD CHIPS
Tsung-Wei Huang, Shih-Yuan Yeh, Tsung-Yi Ho - *National Cheng Kung Univ.*

6A.3 VARIATION TOLERANT SENSING SCHEME OF SPIN-TRANSFER TORQUE MEMORY FOR YIELD IMPROVEMENT
Zhenyu Sun, Hai Li - *Polytechnic Institute of New York Univ.*
Yiran Chen, Xiaobin Wang - *Seagate Technology*

1:30 - 3:30pm Pine Ballroom

SESSION 6B • PUSHING CLOCK DISTRIBUTION PERFORMANCE

Moderators: Chris Chu - *Iowa State Univ.*
Dwight Hill - *Synopsys, Inc.*

The clocks in a chip represent its pulse, and the energy they consume comprise a major portion of its power consumption. Each picosecond of clock skew comes right off the top of critical-path timing. These four papers present new techniques for squeezing out the skew in clock networks while simultaneously minimizing power. They use the ISPD clock tree synthesis benchmarks to demonstrate effectiveness.

6B.1 NOVEL BINARY LINEAR PROGRAMMING FOR HIGH PERFORMANCE CLOCK MESH SYNTHESIS
Minsik Cho - *IBM Corp.*
David Z. Pan - *Univ. of Texas, Austin*
Ruchir Puri - *IBM Corp.*

6B.2 LOW-POWER CLOCK TREES FOR CPUS
Dong-Jin Lee, Myung-Chul Kim, Igor L. Markov - *Univ. of Michigan*

6B.3 HIGH VARIATION-TOLERANT OBSTACLE-AVOIDING CLOCK MESH SYNTHESIS WITH SYMMETRICAL DRIVING TREES
Xin-Wei Shih, Hsu-Chieh Lee, Kuan-Hsien Ho, Yao-Wen Chang - *National Taiwan Univ.*

6B.4 LOCAL CLOCK SKEW MINIMIZATION USING BLOCKAGE-AWARE MIXED TREE-MESH CLOCK NETWORK
Linfu Xiao, Zigang Xiao, Zaichen Qian, Yan Jiang, Tao Huang, Haitong Tian, Evangeline F.Y. Young - *The Chinese Univ. of Hong Kong*

1:30 - 3:30pm Cedar Ballroom

SESSION 6C • 3-D-ICS AND DETECTION OF FAULTS AND HARDWARE TROJANS

Moderators: Jinfeng Liu - *Synopsys, Inc.*
Zhenyu Qi - *Broadcom Corp.*

This session presents three papers on 3-D-ICs, a paper on the detection of faults and another on the detection of Hardware Trojans (HTs). The first paper on 3-D-ICs focuses on thermal modeling of 3-D-ICs cooled using microfluidic chanels, the second focuses on the test cost for 3-D-ICs, and the third one considers alternatives to Through-Silicon Vias (TSVs) by using inductive or capacitive coupling solutions.

6C.1 3-D-ICE: FAST COMPACT TRANSIENT THERMAL MODELING FOR3-D ICS WITH INTER-TIER LIQUID COOLING
Arvind Sridhar, Alessandro Vincenzi, Martino Ruggiero, - *Ecole Polytechnique Fédérale de Lausanne*
Thomas Brunschwiler - *IBM Corp.*
David Atienza - *Ecole Polytechnique Fédérale de Lausanne*

6C.2 COST-EFFECTIVE INTEGRATION OF THREE-DIMENSIONAL (3-D) ICS EMPHASIZING TESTING COST ANALYSIS
Yibo Chen, Dimin Niu, Yuan Xie - *Pennsylvania State Univ.*
Krishnendu Chakarabarty - *Duke Univ.*

6C.3S EVALUATION OF USING INDUCTIVE/CAPACITIVE-COUPLING VERTICAL INTERCONNECTS IN 3-D NETWORK-ON-CHIP
Jin Ouyang, Jing Xie, Matthew Poremba, Yuan Xie - *Pennsylvania State Univ.*

6C.4 SCALABLE SEGMENTATION-BASED MALICIOUS CIRCUITRY DETECTION AND DIAGNOSIS
Sheng Wei, **Miodrag Potkonjak** - *Univ. of California, Los Angeles*

6C.5S APPLICATION-AWARE DIAGNOSIS OF RUNTIME HARDWARE FAULTS
Andrea Pellegrini, Valeria Bertacco - *Univ. of Michigan*

Tuesday, November 9, 2010

4:00 - 6:00pm Oak Ballroom

TUTORIAL 6 • ORGANIC ELECTRONICS

Moderator: Hagen Klauk - *Max Planck Institute for Solid State Research*

Electronic devices based on conjugated organic semiconductors hold great promise for emerging applications in flexible and printed electronics. In this tutorial we will provide an overview of:

- Materials and manufacturing of organic transistors
- Design and manufacturing of organic RFID circuits
- Design of sensor and memory arrays with organic transistors
- Design of analog circuits with organic transistors

MATERIALS AND MANUFACTURING OF ORGANIC TRANSISTORS
Hagen Klauk, Ute Zschieschang - *Max Planck Institute for Solid State Research*

DESIGN AND MANUFACTURING OF ORGANIC RFID CIRCUITS
Jan Genoe, Kris Myny, Soeren Steudel, Paul Heremans - *IMEC*

DESIGN OF LARGE AREA ELECTRONICS WITH ORGANIC TRANSISTORS
Makoto Takamiya, Koichi Ishida, Tsuyoshi Sekitani, Takao Someya, Takayasu Sakurai - *The Univ. of Tokyo*

DESIGN OF ANALOG CIRCUITS USING ORGANIC FIELD-EFFECT TRANSISTORS
Boris Murmann, Wei Xiong - *Stanford Univ.*

4:00 - 6:00pm Fir Ballroom

SESSION 7A • ADVANCES IN TIMING ANALYSIS

Moderators: Igor Keller - *Cadence Design Systems, Inc.*
Yaping Zhan - *Advanced Micro Devices, Inc.*

This session presents several recent advances in timing analysis and their applications. The first paper proposes an active learning scheme for low-cost adaptive testing based on timing modeling. The second paper develops a new tool of ternary decision diagram to analyze circuit dynamic behavior. The third paper discusses modeling and analysis techniques for latch-controlled circuits. The final paper focuses on timing-independent false path identification.

7A.1 ACTIVE LEARNING FRAMEWORK FOR POST-SILICON VARIATION EXTRACTION AND TEST COST REDUCTION
Cheng Zhuo - *Univ. of Michigan*
Kanak Agarwal - *IBM Corp.*
David Blaauw, Dennis Sylvester - *Univ. of Michigan*

7A.2 ANALYSIS OF CIRCUIT DYNAMIC BEHAVIOR WITH TIMED TERNARY DECISION DIAGRAM
Lu Wan, Deming Chen - *Univ. of Illinois at Urbana-Champaign*

7A.3 FAST STATISTICAL TIMING ANALYSIS OF LATCH-CONTROLLED CIRCUITS FOR ARBITRARY CLOCK PERIODS
Bing Li, Ning Chen, Ulf Schlichtmann - *Technische Univ. München*

7A.4 ON TIMING-INDEPENDENT FALSE PATH IDENTIFICATION
Feng Yuan, Qiang Xu - *The Chinese Univ. of Hong Kong*

4:00 - 5:30pm Pine Ballroom

SESSION 7B • PARALLEL METHODS FOR POWER GRID AND INTERCONNECT ANALYSIS

Moderators: Eric Keiter - *Sandia National Labs*
Heidi Thornquist - *Sandia National Labs*

This session presents three papers on exploiting multi-core/threads for interconnect and power grid analysis. The first paper presents a technique for parameterized model-order reduction. The second paper presents a hierarchical matrix inversion algorithm for power grid analysis and the last paper presents an analysis method for the thermals in 3-D ICs.

7B.1S 3POR - PARALLEL PROJECTION BASED PARAMETERIZED ORDER REDUCTION FOR MULTI-DIMENSIONAL LINEAR MODELS
Jorge Fernández Villena - *INESC-ID/IST - TU Lisbon*
L. Miguel Silveira - *Cadence Research Labs, INESC-ID/IST - TU Lisbon*

7B.2S A HIERARCHICAL MATRIX INVERSION ALGORITHM FOR VECTORLESS POWER GRID VERIFICATION
Xuanxing Xiong, Jia Wang - *Illinois Institute of Technology*

7B.3S FAST THERMAL ANALYSIS ON GPU FOR 3-D-ICS WITH INTEGRATED MICROCHANNEL COOLING
Zhuo Feng - *Michigan Technological Univ.*
Peng Li - *Texas A&M Univ.*

4:00 - 5:30pm Cedar Ballroom

SESSION 7C • PHYSICAL DESIGN FOR MANUFACTURABILITY AND VARIABILITY

Moderators: Yufeng Luo - *Mentor Graphics Corp.*
Yongseok Cheon - *Synopsys, Inc.*

With aggressive technology scaling that creates complicated design with staggering complexity, manufacturability and variability are important factors that cannot be ignored any futher in physical optimization. The papers in this session address manufacturability and variability at different levels and applications: wire perturbation optimization for double patterning technology, statistical design techniques and discrete gate-sizing for timing yield optimization. The first paper presents a wire perturbation algorithm to fix as many native conflicts as possible in the double patterning technology. The second paper presents a lower bound computation technique to evaluate statistical design optimization methods. The last one demonstrates that significant timing yield improvement via globally-informed discrete gate-sizing algorithm.

7C.1ß NATIVE-CONFLICT-AWARE WIRE PERTURBATION FOR DOUBLE PATTERNING TECHNOLOGY
Szu-Yu Chen, Yao-Wen Chang - *National Taiwan Univ.*

7C.2 A LOWER BOUND COMPUTATION METHOD FOR EVALUATION OF STATISTICAL DESIGN TECHNIQUES
Vineeth Veeti, Dennis Sylvester, David Blaauw - *Univ. of Michigan*

7C.3 TIMING YIELD OPTIMIZATION VIA DISCRETE GATE-SIZING USING GLOBALLY-INFORMED DELAY PDFS
Shantanu Dutt, **Huan Ren** - *Univ. of Illinois*

8:30am - 12:30pm Oak Ballroom

TUTORIAL 7 • DIGITAL MICROFLUIDIC BIOCHIPS: A VISION FOR FUNCTIONAL DIVERSITY AND MORE THAN MOORE

Moderator: Krishnendu Chakrabarty - *Duke Univ.*

Advances in droplet-based "digital" microfluidics have led to the emergence of biochip devices for automating laboratory procedures in biochemistry and molecular biology. These devices enable the precise control of nanoliter-volume droplets of biochemical samples and reagents. Therefore, integrated circuit (IC) technology can be used to transport and transport "chemical payload" in the form of micro/nanofluidic droplets. As a result, non-traditional biomedical applications and markets (e.g., high-throughout DNA sequencing, portable and point-of-care clinical diagnostics, protein crystallization for drug discovery), and fundamentally new uses are opening up for ICs and systems. However, continued growth (and larger revenues resulting from technology adoption by pharmaceutical and healthcare companies) depends on advances in chip integration and design-automation tools. In particular, design-automation tools are needed to ensure that biochips are as versatile as the macro-labs that they are intended to replace. This is therefore an opportune time for the semiconductor industry and circuit/system designers to make an impact in this emerging field.

This tutorial offers attendees an opportunity to bridge the semiconductor ICs/systems industry with the biomedical and pharmaceutical industries.

The tutorial will first describe emerging applications (market drivers) in biology and biochemistry that can benefit from advances in electronic "biochips". The presenter will next describe technology platforms for accomplishing "biochemistry on a chip", and introduce the audience to microarrays and fluidic actuation methods based on microfluidics. The droplet-based "digital" microfluidic platform based on electrowetting will be described in considerable detail.

Next, the presenter will describe fabrication techniques for digital microfluidic biochips, followed by computer-aided design, design-for-testability, and reconfiguration aspects of chip/system design. The physics of droplet flow, and advances ion modeling and simulation techniques will be covered. Synthesis algorithms and methods will be presented to map behavioral descriptions to a digital microfluidic platform, and generate an optimized schedule of bioassay operations, chip layout, and droplet-flow paths. In this way, the audience will see how a "biochip compiler" can translate protocol descriptions provided by an end user (e.g., a chemist or a nurse at a doctor's clinic) to a set of optimized and executable fluidic instructions that will run on the underlying digital microfluidic platform. Testing techniques will be described to detect faults after manufacture and during field operation. A number of case studies based on representative assays and laboratory procedures will be interspersed in appropriate places throughout the tutorial.

The tutorial presenters envision an automated design flow for biochips, in the same way as design automation revolutionized IC design in the 80s and 90s. Biochip users (e.g., chemists, nurses, doctors and clinicians) and the biotech/pharmaceutical industry will adapt more easily to new technology if appropriate design tools and in-system automation methods are made available.

DIGITAL MICROFLUIDIC BIOCHIPS: A VISION FOR FUNCTIONAL DIVERSITY AND MORE THAN MOORE

Tsung-Yi Ho - *National Cheng Kung Univ.*
Jun Zeng - *Hewlett-Packard Labs*
Krishnendu Chakrabarty - *Duke Univ.*

Wednesday, November 10, 2010

8:30 - 10:00am Fir Ballroom

SESSION 8A • ADVANCES IN CORE LOGIC SYNTHESIS

Moderators: Thomas Shiple - *Synopsys, Inc.*
Philip Brisk - *Univ. of California, Riverside*

This session consists of four papers on classical logic synthesis. The first two deal with efficient bi-decomposition and state re-encoding for low power respectively. The last two papers address multi-output Boolean matching and techniques for interpolant compression respectively.

8A.1ß BI-DECOMPOSITION OF LARGE BOOLEAN FUNCTIONS USING BLOCKING EDGE GRAPHS
Mihir Choudhury, Kartik Mohanram - *Rice Univ.*

8A.2 PEAK CURRENT REDUCTION BY SIMULTANEOUS STATE REPLICATION AND RE-ENCODING
Junjun Gu - *Univ. of Maryland*
Lin Yuan - *Synopsys, Inc.*
Gang Qu - *Univ. of Maryland*
Qiang Zhou - *Tsinghua Univ.*

8A.3S BOOLEAN MATCHING OF FUNCTION VECTORS WITH STRENGTHENED LEARNING
Chih-Fan Lai, Jie-Hong Roland Jiang - *National Taiwan Univ.*
Kuo-Hua Wang - *Fu Jen Catholic Univ.*

8A.4S REDUCTION OF INTERPOLANTS FOR LOGIC SYNTHESIS
John Backes, Marc Riedel - *Univ. of Minnesota*

8:30 - 10:00am Pine Ballroom

SESSION 8B • ROUTING -- THEORY AND PRACTICE

Moderators: Cheng-Kok Koh - *Purdue Univ.*
Ting-Chi Wang - *National Tsing-Hua Univ.*

The papers in this session address theoretical and practical aspects of routing. The first paper presents an algorithm for the construction of optimal obstacle-avoiding rectilinear Steiner minimum trees. Using network-flow ons, the second paper solves the problem of escape routing of multiple differential pairs in a printed circuit board. The third paper models routing congestion caused by bottleneck in local pin access and presents detailed placement techniques to relieve local routing congestion.

8B.1ß OBSTACLE-AVOIDING RECTILINEAR STEINER MINIMUM TREE CONSTRUCTION: AN OPTIMAL APPROACH
Tao Huang, Evangeline F.Y. Young - *The Chinese Univ. of Hong Kong*

8B.2 ON THE ESCAPE ROUTING OF DIFFERENTIAL PAIRS
Tan Yan - *Synopsys, Inc., Univ. of Illinois at Urbana-Champaign*
Pei-Ci Wu, Qiang Ma - *Univ. of Illinois at Urbana-Champaign*
Martin D. F. Wong - *Univ. of Illinois*

8B.3 NEW PLACEMENT PREDICTION AND MITIGATION TECHNIQUES FOR LOCAL ROUTING CONGESTION
Taraneh Taghavi, Charles Alpert, Andrew Huber, Zhuo Li, Gi-Joon Nam, Shyam Ramji, Lakshmi Reddy, Jarrod Roy, Gustavo Tellez, Paul Villarrubia, Natarajan Viswanathan - *IBM Corp.*

8:30 - 10:00am Cedar Ballroom

SESSION 8C • POWER OPTIMIZATION FROM SYSTEMS TO CIRCUITS

Moderators: Muhammad Shafique - *Karlsruhe Institute of Technology*
Jiong Luo - *Synopsys, Inc.*

This session covers power optimization from system-level to circuit-level designs. The first paper discusses the pitfalls that designers in sub/near-threshold systems often not consider for power optimization in system levels. The second paper presents a scheme based on counters to allow Vth hopping to achieve power optimization. The last paper studies the circuit-level design methodology for fast and reliable power mode transition.

8C.1 MISLEADING ENERGY AND PERFORMANCE CLAIMS IN SUB/NEAR THRESHOLD DIGITAL SYSTEMS
Yu Pu, Xin Zhang, Jim Huang- *The Univ. of Tokyo*
Atsushi Muramatsu, Masahiro Nomura, Koji Hirairi, Hidehiro Takata, Taro Sakurabayashi, Shinji Miyano - *STARC*
Makoto Takamiya , Takayasu Sakurai - *The Univ. of Tokyo*

8C.2 STRETCHING THE LIMIT OF MICROARCHITECTURAL LEVEL LEAKAGE CONTROL WITH ADAPTIVE LIGHT-WEIGHT VTH HOPPING
- *Univ. of Cincinnati*
Hao Xu, Wen-Ben Jone, Ranga Vemuri - *Univ. of Cincinnati*

8C.3 CURRENT SHAPING AND MULTI-THREAD ACTIVATION FOR FAST AND RELIABLE POWER MODE TRANSITION IN MULTICORE DESIGNS
Hao Xu, Ranga Vemuri, Wen-Ben Jone - *Univ. of Cincinnati*

10:30am - 12:30pm Fir Ballroom

SESSION 9A • ALGORITHMS FOR PLACEMENT: FULL HOUSE

Moderators: Bill Halpin - *Synopsys, Inc.*
Yegna Parasuram - *Mentor Graphics Corp.*

This session offers advanced placement algorithms that target speed, routability, mixed-size netlists, 3-D and analog circuits. The three long and two short presentations showcase the great variety of modern placement research.

9A.1ß SIMPL: AN EFFECTIVE PLACEMENT ALGORITHM
Myung-Chul Kim, Dong-Jin Lee, Igor L. Markov - *Univ. of Michigan*

9A.2 UNIFIED ANALYTICAL GLOBAL PLACEMENT FOR LARGE-SCALE MIXED-SIZE CIRCUIT DESIGNS
Meng-Kai Hsu, Yao-Wen Chang - *National Taiwan Univ.*

9A.3 DESIGN-HIERARCHY AWARE MIXED-SIZE PLACEMENT FOR ROUTABILITY OPTIMIZATION
Yi-Lin Chuang - *National Taiwan Univ.*
Gi-Joon Nam, Charles J. Alpert - *IBM Corp.*
Yao-Wen Chang - *National Taiwan Univ.*
Jarrod Roy, Natarajan Viswanathan - *IBM Corp.*

9A.4S STRESS-DRIVEN 3-D-IC PLACEMENT WITH TSV KEEP-OUT ZONE AND REGULARITY STUDY
Krit Athikulwongse - *Georgia Institute of Technology*
Ashutosh Chakraborty, Jae-Seok Yang, David Z. Pan - *Univ. of Texas, Austin*
Sung Kyu Lim - *Georgia Institute of Technology*

9A.5S PRACTICAL PLACEMENT AND ROUTING TECHNIQUES FOR ANALOG CIRCUIT DESIGNS
- *The Chinese Univ. of Hong Kong*
Linfu Xiao, Evangeline F.Y. Young, Xiaoyong He, K.P. Pun - *The Chinese Univ. of Hong Kong*

10:30am - 12:30pm Pine Ballroom

SESSION 9B • ANALYSIS AND ALGORITHMS FOR DESIGN AND TEST IN 3-D AND MANY-CORE SYSTEMS

Moderators: Arijit Raychowdhury - *Intel Corp.*
Saibal Mukhopadhyay - *Georgia Institute of Technology*

This session comprises of four papers discussing different aspects of design and test in 3-D and manycore systems. The first paper provides a framework for characterizing reliability in many-core systems. The second paper addresses the issue of electrical characterization of RF TSVs for heterogeneous ICs. The next paper provides design and test methodologies for characterizing and repairing defects in 3-D ICs. The last paper of the session discusses a new and more efficient Poisson solver for thermal analysis.

9B.1ß **CHARACTERIZING THE LIFETIME RELIABILITY OF MANYCORE PROCESSORS WITH CORE-LEVEL REDUNDANCY**
Lin Huang, **Qiang Xu** - *The Chinese Univ. of Hong Kong*

9B.2 **ELECTRICAL CHARACTERIZATION OF RF TSV FOR 3-D MULTI-CORE AND HETEROGENEOUS ICS**
Haigang Yang, Le Yu - *Chinese Academy of Sciences*
Tom T. Jing, Min Xu, Robert Geer, **Wei Wang** - *University at Albany, State Univ. of New York*

9B.3 **DESIGN METHOD AND TEST STRUCTURE TO CHARACTERIZE AND REPAIR TSV DEFECT INDUCED SIGNAL DEGRADATION IN 3-D SYSTEM**
Minki Cho, Chang Liu, Dae Hyun Kim, Sung Kyu Lim, Saibal Mukhopadhyay - *Georgia Institute of Technology*

9B.4 **FAST POISSON SOLVERS FOR THERMAL ANALYSIS**
Haifeng Qian - *IBM T.J. Watson Research Ctr.*
Sachin Sapatnekar - *Univ. of Minnesota*

10:30am - 12:30pm Cedar Ballroom

SESSION 9C • ADVANCED ANALYSIS OF CIRCUIT/ DEVICE RELIABILITY

Moderators: Bruce W. McGaughy - *ProPlus Design Solutions, Inc.*
Eric R. Keiter - *Sandia National Labs*

This session focuses on techniques for the analysis of circuit reliability and variability. The first paper proposes a new technique for speeding up importance-sampling based yield analysis. The second paper presents a method for circuit-level simulation of Random Telegraph Noise. The third paper analyzes the effects of work-function variation on bias temperature instabilities. The last paper proposes an approach for structured layout generation based on transistor decomposition.

9C.1 SEQUENTIAL IMPORTANCE SAMPLING FOR LOW-PROBABILITY AND HIGH-DIMENSIONAL SRAM YIELD ANALYSIS
Kentaro Katayama - *Kyoto Univ.*
Shiho Hagiwara - *Tokyo Institute of Technology*
Hiroyuki Ochi, Takashi Sato, Hiroshi Tsutsui - *Kyoto Univ.*

9C.2 SIMULATION OF RANDOM TELEGRAPH NOISE WITH 2-STAGE EQUIVALENT CIRCUIT
Yun Ye, Chi-Chao Wang, Yu Cao - *Arizona State Univ.*

9C.3 WORK-FUNCTION VARIATION INDUCED FLUCTUATION IN BIAS-TEMPERATURE-INSTABILITY CHARACTERISTICS OF EMERGING METAL-GATE DEVICES AND IMPLICATIONS FOR DIGITAL DESIGN
Seid Hadi Rasouli - *Univ. of California, Santa Barbara*
Kazuhiko Endo - *National Institute of Advanced Industrial Science and Technology, Japan*
Kaustav Banerjee - *Univ. of California, Santa Barbara*

9C.4 STRUCTURED ANALOG CIRCUIT DESIGN AND MOS TRANSISTOR DECOMPOSITION FOR HIGH ACCURACY APPLICATIONS
Bo Yang, Shigetoshi Nakatake, Jing Lin, Qing Dong - *Univ. of Kitakyushu*

2:00 - 4:00pm Oak Ballroom

TUTORIAL 8 • MANUFACTURING, CAD AND THERMAL-AWARE ARCHITECTURES FOR 3-D MPSoCS

Moderator: David Atienza - *Ecole Polytechnique Fédérale de Lausanne*

Multiprocessor systems-on-chip (MPSoCs) have penetrated the consumer electronics market as a powerful solution to answer the strong and steadily growing demand for scalable and high performance systems, at limited design complexity. Furthermore, technical advances in manufacturing technologies are fueling the trend towards more powerful 3-D MPSoC designs, as it provides a very promising opportunity to continue performance improvements using CMOS technology, with smaller form factor, higher integration density, and even the support for the realization of mixed-technology chips.

However, if planar MPSoCs are prone to alarming temperature variations on the die, which seriously decrease their expected reliability and lifetime, 3-D stacking (in addition to larger manufacturing complexity) creates even higher power and heat density, leading to degraded performance if thermal management is not handled properly in novel system-level design flows, which can combine mature multi-tier IC stacking manufacturing, appropriate 3-D computer-aided design (CAD) tools and sensible hardware/software thermal-aware architectures for 3-D MPSoCs.

This tutorial brings together leading 3-D IC and MPSoC design experts, in order to cover in a comprehensive and structured way the key aspects related to manufacturing and system-level EDA topics in 3-D MPSoC design.

In the first part, we introduce the key manufacturing technology aspects in 3-D VLSI integration of multiple active tiers (processors, memories, I/O, etc.) and the CAD support to enable efficient alignment of the different tiers to efficiently interconnect them with vertical interconnects (Through-Silicon-Vias or TSVs).

In the second part, we propose different alternatives for 3-D microprocessor design for MPSoC architectures, which exploit the use of multi-layer TSVs as basic communication links in Network-on-Chip (NoC)-based interconnects to minimize the memory access bottleneck in classical planar MPSoCs.

In the third part, we present sensible methods to characterize the thermal behavior of forthcoming 3-D MPSoC architectures exploiting both hardware-based system emulation and software-based thermal modeling, and motivate the need for inter-tier 3-D active (liquid) cooling in high-performance 3-D MPSoCs.

Finally, we discuss reactive and proactive run-time thermal management methods, which achieve thermal runaway prevention while incurring negligible performance degradation in 3-D MPSoCs. Moreover, we show that effective energy-efficient thermal balancing can be achieved in future high-performance 3-D MPSoCs by exploiting these new active management methods (liquid cooling-based) in combination to task migration and dynamic frequency and voltage scaling at the hardware and OS levels.

FUZZY CONTROL FOR ENFORCING ENERGY EFFICIENCY IN HIGH PERFORMANCE 3-D SYSTEMS

Ayse K. Coskun - *Boston Univ.*
David Atienza - *Ecole Polytechnique Fédérale de Lausanne*
Mohamed Sabry - *Ecole Polytechnique Fédérale de Lausanne*

2:00 - 4:00pm Fir Ballroom

SESSION 10A • ADVANCED APPLICATIONS OF LOGIC SYNTHESIS

Moderators: Naehyuck Chang - *Seoul National Univ.*
Vigyan Singhal - *Oski Technology, Inc.*

This session consists of papers in which logic synthesis is applied to diverse problems. The first two papers deal with logic techniques for ECOs and synthesis of multipliers for FFTs respectively. The remaining papers present techniques to scale the precision of arithmetic variables, synthesize control structures for post-silicon tuning, perform distributed Boolean matching and polynomial factoring respectively.

10A.1 A ROBUST FUNCTIONAL ECO ENGINE BY SAT PROOF MINIMIZATION AND INTERPOLATION TECHNIQUES
Bo-Han Wu, Chun-Ju Yang, Chung-Yang (Ric) Huang, Jie-Hong Roland Jiang - *National Taiwan Univ.*

10A.2 EFFICIENT ARITHMETIC SUM-OF-PRODUCT (SOP) BASED MULTIPLE CONSTANT MULTIPLICATION (MCM) FOR FFT
Vinay Karkala - *Texas A&M Univ.*
Joseph Wanstrath - *Rose-Hulman Institute of Technology*
Travis Lacour, **Sunil P. Khatri** - *Texas A&M Univ.*

10A.3S ANALYSIS OF PRECISION FOR SCALING THE INTERMEDIATE VARIABLES IN FIXED-POINT ARITHMETIC CIRCUITS
Omid Sarbishei, Katarzyna Radecka - *McGill Univ.*

10A.4S SYNTHESIS OF AN EFFICIENT CONTROLLING STRUCTURE FOR THE POST-SILICON CLOCK SKEW MINIMIZATION
Mac Y.C. Kao, Hsuan-Ming Chou, Kun-Ting Tsai, Shih-Chieh Chang, - *National Tsing-Hua Univ.*

10A.5S ENGINEERING A SCALABLE BOOLEAN MATCHING BASED ON EDA SAAS 2.0
Chun Zhang - *Fudan Univ.*
Yu Hu - *Univ. of Alberta*
Lingli Wang - *Fudan Univ.*
Lei He - *Univ. of California, Los Angeles*
Jiarong Tong - *Fudan Univ.*

10A.6S POLYNOMIAL DATAPATH OPTIMIZATION USING CONSTRAINT SOLVING AND FORMAL MODELLING
Finn Haedicke - *Univ. Bremen*
Bijan Alizadeh - *The Univ. of Tokyo*
Goerschwin Fey - *Univ. Bremen*
Masahiro Fujita - *The Univ. of Tokyo*
Rolf Drechsler - *Univ. Bremen*

2:00 - 4:00pm Pine Ballroom

SESSION 10B • ADVANCES IN VERIFICATION

Moderators: Anubhav Gupta - *Synopsys, Inc.*
Sanjit A. Seshia - *Univ. of California, Berkeley*

This session presents five papers on simulation and formal verification. The first paper addresses the problem of selecting functional tests for quickly attaining high coverage. The second paper presents an approach to generate interpolants easily from proof-generating SMT solvers. The third paper proposes new symbolic techniques for performance analysis. Improved model checking through a hybrid of stateless and state-based search is the contribution of the fourth paper. The last paper of the session presents methods for finding deadlocks in SystemC designs.

10B.1 ONLINE SELECTION OF EFFECTIVE FUNCTIONAL TEST PROGRAMS BASED ON NOVELTY DETECTION
Po-Hsien Chang, Dragoljub Gagi Dramanac, Li.-C Wang - *Univ. of California, Santa Barbara*

10B.2 FLEXIBLE INTERPOLATION WITH LOCAL PROOF TRANSFORMATIONS
Roberto Bruttomesso, **Simone Fulvio Rollini**, Natasha Sharygina, Aliaksei Tsitovich - *Univ. della Svizzera Italiana*

10B.3 SYMBOLIC PERFORMANCE ANALYSIS OF ELASTIC SYSTEMS
Marc Galceran-Oms, Jordi Cortadella - *Univ. Politècnica de Catalunya*
Michael Kishinevsky - *Intel Corp.*

10B.4S EFFICIENT STATE SPACE EXPLORATION: INTERLEAVING STATELESS AND STATE-BASED MODEL CHECKING
Malay Ganai, **Chao Wang**, Weihong Li - *NEC Corp.*

10B.5S FORMAL DEADLOCK CHECKING ON HIGH-LEVEL SYSTEMC DESIGNS
Chun-Nan Chou, Chang-Hong Hsu, Yueh-Tung Chao, Chung-Yang (Ric) Huang - *National Taiwan Univ.*

2:00 - 4:00pm Cedar Ballroom

SESSION 10C • RECENT ADVANCES IN POWER GRID AND INTERCONNECT ANALYSIS

Moderators: Nagib Hakim - *Intel Corp.*
Marek Patyra - *Intel Corp.*

This session has four papers describing recent advances in this area. The first paper presents a passivity enforcement technique for descriptor systems. The next paper shows how to fix problems in power grids using sensitivity analysis. The third paper describes techniques for verifying both power and ground grids at the same time. The final paper shows how to characterize worst case current waveforms for RLC grids.

10C.1 PEDS: PASSIVITY ENFORCEMENT FOR DESCRIPTOR SYSTEMS VIA HAMILTONIAN-SYMPLECTIC MATRIX PENCIL PERTURBATION
Yuanzhe Wang, Zheng Zhang - *The Univ. of Hong Kong*
Cheng-Kok Koh - *Purdue Univ.*
Grantham K.H. Pang, Ngai Wong - *The Univ. of Hong Kong*

10C.2 POWER GRID CORRECTION USING SENSITIVITY ANALYSIS
Meric Aydonat, Farid N. Najm - *Univ. of Toronto*

10C.3S EARLY P/G GRID VOLTAGE INTEGRITY VERIFICATION
Mehmet Avci, Farid N. Najm - *Univ. of Toronto*

10C.4S CHARACTERIZATION OF THE WORST-CASE CURRENT WAVEFORM EXCITATIONS IN GENERAL RLC-MODEL POWER GRID ANALYSIS
Nestor Evmorfopoulos, Maria-Aikaterini Rammou, George Stamoulis, John Moondanos - *Univ. of Thessaly*

WORKSHOP: INTERNATIONAL WORKSHOP ON BIOMEDICAL SYSTEM DESIGN

Time: 8:30am - 6:00pm

Oak Ballroom

Organizers: Xin Li - *Carnegie Mellon Univ.*
Joel Phillips - *Cadence Design Systems, Inc.*
Douglas Weber - *Univ. of Pittsburgh*
Dejan Markovic - *Univ. of California, Los Angeles*
Luca Daniel - *Massachusetts Institute of Technology*

Biomedical circuit and system design has become an emerging area in recent years. The rapid growth in this field poses a broad range of new challenges in multiple areas such as electrical engineering, computer science, biometrical engineering, etc. Solving these open problems requires interdisciplinary collaboration among scientists and engineers from different research communities. The International Workshop on Biomedical System Design (BSD 2010) provides an open forum for discussions on important issues related to biomedical circuit and system design. The intent of this workshop is to encourage informal discussions of the latest advances in the field and motivate close interaction and collaboration between different researchers. Topics of interest include (but not limited to):

- Design and implementation of biomedical signal processing
- Circuit and system design method for implantable electronics
- Modeling and simulation for biomedical systems
- Software and hardware infrastructure for biomedical applications

Invited Talks:

Jack Judy, *Defense Advanced Research Projects Agency, Univ. of California, Los Angeles*
Keynote: **SYSTEMS ISSUES FOR RELIABLE NEURAL INTERFACES**

James Bower, *Univ. of Texas, San Antonio*
Keynote: **HOW SHOULD MODELS BE PUBLISHED? IS IT TIME TO CHANGE THE PARADIGM FOR PUBLISHING BIOMEDICAL RESEARCH?**

Pradeep Fernandes, *Cellworks Group Inc.*
DISEASE MODELS AND THEIR USE IN DESIGNING THERAPIES

Ada Poon, *Stanford Univ.*
AUTONOMOUS AND MINIATURE IMPLANTABLE SYSTEMS

Joel Dawson, *Massachusetts Institute of Technology*
NEW ARCHITECTURES FOR IMPLANTABLE AND WEARABLE TRANSCEIVERS

Zhi-Hong Mao, *Univ. of Pittsburgh*
DIMENSIONALITY REDUCTION IN CONTROL AND COORDINATION OF HUMAN HAND

Dejan Markovic, *Univ. of California, Los Angeles*
SPIKE SORTING: THE FIRST STEP IN DECODING THE BRAIN

Xin Li, *Carnegie Mellon Univ.*
REAL-TIME ROBUST SIGNAL SPACE SEPARATION FOR MAGNETOENCEPHALOGRAPHY

Lou Scheffer, *Janelia Farms Research Campus, Howard Hughes Medical Institute*
REVERSE ENGINEERING OF NERVOUS SYSTEM CONSTRUCTS THROUGH ELECTRON MICROSCOPY

Junghoon Lee, *Merck & Co., Inc.*
CARDIOVASCULAR CIRCULATION MODELS IN HYPERTENSION RESEARCH

WORKSHOP: WORKSHOP ON VARIABILITY MODELING AND CHARACTERIZATION (VMC)

Time: 8:30am - 5:00pm

Fir Ballroom

Organizers: Hidetoshi Onodera - *Kyoto Univ.*
Frank Liu - *IBM Corp.*
Yu Cao - *Arizona State Univ.*

Sponsored by: acm, sigda, IEEE, Electron Devices Society, SRC Semiconductor Research Corporation

It is widely recognized that process variation is emerging as a fundamental challenge to IC design in scaled CMOS technology; and it will have profound impact on nearly all aspects of circuit performance. While some of the negative effects of variability can be handled with improvements in the manufacturing process, the industry is starting to accept the fact that some of the effects are better mitigated during the design process. Handling variability in the design process will require accurate and appropriate models of variability and its dependence on designable parameters (i.e. layout), and its spatial and temporal distributions. It also requires carefully designed test structures and proper statistical data analysis methods to extract meaningful models from large volumes of silicon measurements. The resulting compact modeling of systematic, random, spatial, and temporal variations is essential to abstract the physical level variations into a format the designers (and more importantly, the tools they use) can utilize. This workshop provides a forum to discuss current practice as well as near future research needs in test structure design, variability characterization, compact variability modeling, and statistical simulation.

Key topics of this workshop includes (but not limited to):

- Physics mechanisms and technology trends of device-level variations
- First-principles simulation methods for predicting variability
- Time-dependent variation and their interaction with other variation sources.
- Compact modeling of variations in transistors and interconnec
- Device and circuit level modeling techniques
- Test structure design for variability
- Variability characterization and bounding
- Statistical data analysis and model extraction methods
- Novel implementation and simulation techniques for dealing with variability

8:30 – 8:40am Opening Remarks

8:40 – 10:10am **PROCESS VARIABILITY IN SCALED VLSI DESIGN**

1. Test Structures, Circuits, and Extraction Methods for Determining Pattern Density Effects: **Duane Boning,** *Massachusetts Institute of Technology*
2. Measurements and Post-Fabrication Self-Improvement of SRAM Cell Stability: **Toshiro Hiramoto,** *The Univ. of Tokyo*
3. Improving Design, Manufacturing, and Even Test through Test-Data Mining: **Shawn Blanton,** *Carnegie Mellon Univ.*

10:10 – 10:30am Morning Break

10:30 – 12:00pm **ANALOG DESIGN VARIABILITY**

1. The Impact of Process Variability as It Relates to Modeling and Design in Advanced CMOS Technologies: **Brandt Braswell,** *Freescale Semiconductor, Inc.*
2. Characterization and Modeling of MOSFET Noise in Sub-threshold Region: **Purushothaman Srinivasan**, *Texas Instruments, Inc.*
3. Handling Process Variability: Self-Testing and Self-Tuning Mixed-Signal/RF Circuits and Systems: **Abhijit Chatterjee**, *Georgia Institute of Technology*

12:00 – 1:30pm Lunch Break

1:30 – 3:30pm **VARIABILITY IN 3-D INTEGRATION**

1. New Sources of Variability in 3D TSS Technologies: **Riko Radojcic**, *Qualcomm, Inc.*
2. Managing Variability in 3D IC: **Paul Franzon**, *North Carolina State Univ.*
3. Interconnect Networks in 2D and 3D Nanoelectronic Systems: **Azad Naeemi,** *Georgia Institute of Technology*
4. TSV Stress Effects for Digital and Analog Circuits: **Victor Moroz**, *Synopsys, Inc.*

3:30 – 5:00pm **POSTER SESSION AND DISCUSSION**

Workshop website: http://nimo.asu.edu/vmc

WORKSHOP: PARCAD 2010

Time: 9:00am - 6:30pm
Pine Ballroom

Sponsored by:

CEDA Council on Electronic Design Automation DATC

Organizers: Andreas Kuehlmann - *Coverity, Inc.*
David Kung - *IBM Corp.*

The IEEE Council on EDA and the IEEE Design Automation Committee have jointly organized a workshop on Parallel Programming for EDA.

The workshop will bring together experts from the design automation and parallel programming community to discuss the timely issue of parallelization of EDA tools. This challenging topic has received significant attention from EDA vendors, industry CAD groups and the design community. Design complexity is exponentially increasing driven by density scaling and 3-D integration – leading to a dramatic growth of the verification needs and optimization opportunities. Furthermore, future technology nodes are becoming more difficult to develop due to lithographic challenges and increase in variability. In order to keep up with these trends, the computational requirements of design tools are rapidly growing, which translates into the need of more compute cycles. In the past, the increasing computing demand was addressed by Moore's Law, which offered an exponential growth of single thread performance. However, with the demise of frequency scaling, effective solutions must now leverage multi-core CPUs, distributed computing architectures or special co-processors. Efficient parallelization of EDA applications is now a must for any modern EDA tool.

This workshop provides a forum for leading experts from the CAD, parallel programming and high-performance computing community to present their latest research, exchange ideas, and conduct brainstorming. Computing platforms are central to parallel programming, so we have invited luminaries from HPC centers and Cloud Computing to explain how EDA applications might be deployed there. Circuit simulation and place&route are core algorithms in design automation – we have two practicing experts to share their insights on parallelization of these algorithms. Parallel programming is intrinsically a difficult proposition and most CAD developers are new to this arena. Several parallel programming evangelists will be talking about parallel programming paradigms and tools that enhance the productivity of the code developers. We round up the workshop with a panel of CAD development architects, who have parallelized key EDA applications, to share their success stories.

The goal of ParCAD 2010 is to educate the participants on the various challenges of parallelization, give them concrete advice on tools and methods for parallel code development and offer insight into new cross-disciplinary solutions that target the characteristics of EDA applications.

WORKSHOP: PARCAD 2010

9:00 -10:00am **Keynote**
"PREPARING FOR PARALLEL COMPUTING: LESSONS FROM THE FAILED REVOLUTION OF THE 80'S"
Prof. Arvind, *Massachusetts Institute of Technology*

10:00 -10:15am **Break**

10:15 - 11:15am **Computing Platforms**
"UNSTRUCTURED MESH ADAPTIVE SIMULATIONS ON MASSIVELY PARALLEL COMPUTERS"
Mark Shephard, *CCNI, Rensselaer Polytechnic Institute*

"ARCHITECTING FOR AMAZON WEB SERVICES"
Matt Tavis, *Amazon.com, Inc.*

11:15am - 12:15pm **Applications**
"PRACTICAL PARALLELISM: TALES FROM THE TRENCHES OF COMMERCIAL PLACE AND ROUTE TOOLS"
Adrian Ludwin, *Altera Corp*.

"DEVELOPING SOFTWARE FOR LARGE-SCALE CIRCUIT SIMULATION USING TRILINOS"
Heidi Thornquist, Sandia National Labs

12:15 - 1:30pm **Lunch**

1:30 - 2:30 **Tools for Parallel Programming I**
"INTEL'S PROFILING AND DEBUGGING TOOLS"
Vasanth Tovinkere, *Intel Corp*.

2:30 - 3:00pm **Break**

3:00 - 4:30pm **Tools for Parallel Programming II**
"DESIGN PATTERNS AND PARALLEL PROGRAMMING LANGUAGES: PRACTICAL ADVICE FOR REAL PROGRAMMERS"
Tim Mattson, *Intel Corp.*

"USE PATTERNS TO UNDERSTAND, ARCHITECT, AND PARALLELIZE CAD APPLICATIONS"
Bor-Yiing Su, *Univ. of California, Berkeley*

4:30 - 5:00pm Break

5:00 - 6:30pm **Panel: "PRACTICAL EXPERIENCE WITH PROGRAMMING PARALLEL EDA APPLICATIONS"**

Moderator: **Patrick Madden,**
State Univ. of New York, Binghamton

Panelists: **Jay Adams,** *Synopsys, Inc.*
John Croix, *Cadence Design Systems, Inc.*
Patrick Groeneveld, *Magma Design Automation, Inc.*
Duaine Pryorgot, *Mentor Graphics Corp.*
Uli Finkler, *IBM Corp.*
Guy Maor, *Extreme DA*

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571-209-4151
schefferl@janelia.hhmi.org

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Alan J. Hu
Dept. of Computer Science
Univ. of British Columbia
2366 Main Mall,
Vancouver, BC V6T 1Z4, Canada
604-822-6667
ajh@cs.ubc.ca

ASIAN REPRESENTATIVE
Yao-Wen Chang
National Taiwan Univ.
Dept. of Electrical Eng.
Taipei 106, Taiwan
886-2-33663556
ywchang@cc.ee.ntu.edu.tw

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Louisville, CO 80027
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kathy@mpassociates.com

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Technische Universitaet Muenchen
Institute for Electronic Design Automation,
Arcisstr. 21
Munich, 80333 Germany
49-89-289-23679
graeb@tum.de

ACM/SIGDA REPRESENTATIVE
Massoud Pedram
Univ. of Southern California
EE Building, Rm. 344
3740 McClintock Ave.
Los Angeles, CA 90089
213-740-4458
pedram@usc.edu

PROGRAM CHAIR
Joel Phillips
Cadence Research Labs
2150 Shattuck Ave., 10th Fl.
Berkeley, CA 94704
510-647-2804
jrp@cadence.com

EUROPEAN REPRESENTATIVE
Andreas Herkersdorf
Technische Universitaet Muenchen
Institute for Integrated Systems
Arcisstr. 21
Munich, 80333 Germany
49-89-289-22515
herkersdorf@tum.de

CEDA REPRESENTATIVE
Andreas Kuehlmann
Coverity, Inc.
185 Berry St., Ste. 1600
San Francisco, CA 94107
415-321-5233
akuehlmann@coverity.com

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