FINAL PROGRAM

IEEE/ACM ICCAD
2008 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

The premier conference for Electronic Design Technology

WWW.ICCAD.COM

November 10 - 13, 2008
DoubleTree Hotel
San Jose, CA

Sponsored by:

IEEE IEEE CAS/CANDE | IEEE CIRCUITS & SYSTEMS SOCIETY® | CANDE | acm | SIGDA | CEDA IEEE Council on Electronic Design Automation

In cooperation with:

IEEE DATC | IEEE ELECTRON DEVICES SOCIETY | SSCS

Welcome to the 2008 International Conference on Computer-Aided Design (ICCAD)

Welcome to the 2008 International Conference on Computer-Aided Design. ICCAD continues to be the premier and most selective technical conference devoted to technical innovations in the design automation of devices, circuits, and systems. This exciting program of technical papers, tutorials, keynotes and panels will highlight the most important current and future research challenges. The new addition of colocated workshops on hot topics promises non-stop technical excitement. As always, a large number of side meetings and social events provide plenty of opportunities for networking and meeting colleagues and friends.

We invite you to find all the up to date details on the conference website www.iccad.com. To accommodate the new colocated workshops, which will be on Sunday, November 9 and Thursday November 13, this year's schedule starts on Monday, November 10 and integrates the four excellent tutorials into the traditional ICCAD technical program by adding a fifth track. These tutorials, given by world experts, are a great opportunity for updating your knowledge in state-of-the-art and emerging areas. Further recognizing this educational value, and new for 2008, the conference is opening these tutorials to all student attendees at no charge.

This year we received 458 worldwide submissions and the technical program committee, after careful deliberation, selected 122 exceptional papers for presentation. These papers are split into 40 sessions over the three days of the technical program. In addition, the ICCAD program this year includes three embedded tutorials, as well as two designer sessions, all focused on providing additional broad perspectives for our CAD audience.

For 2008 we are excited to have two outstanding plenary keynote speakers. The first is from Mary Lou Jepsen, chief hardware architect of the famous "One Laptop per Child" project. She will talk about that project and about future challenges in CAD for displays, an area of immense potential as new display technologies are deployed. Our second keynote is by Dmitri "Mitya" Chklovskii, world renowned for his research on the human brain and how it relates to traditional computers. In addition, CAD veteran Giovanni De Micheli, well known by the ICCAD community for his distinguished contributions over decades, will be giving a Tuesday lunch talk about exciting new frontiers in biology and environmental engineering.

ICCAD 2008 is the place to be this November! Hot on the heels of the US presidential election, the conference promises a level of technical excitement that is sure to satisfy. See you in San Jose!

Sani Nassif
General Chair

Jaijeet Roychowdhury
Program Chair

IEEE/ACM 2008 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

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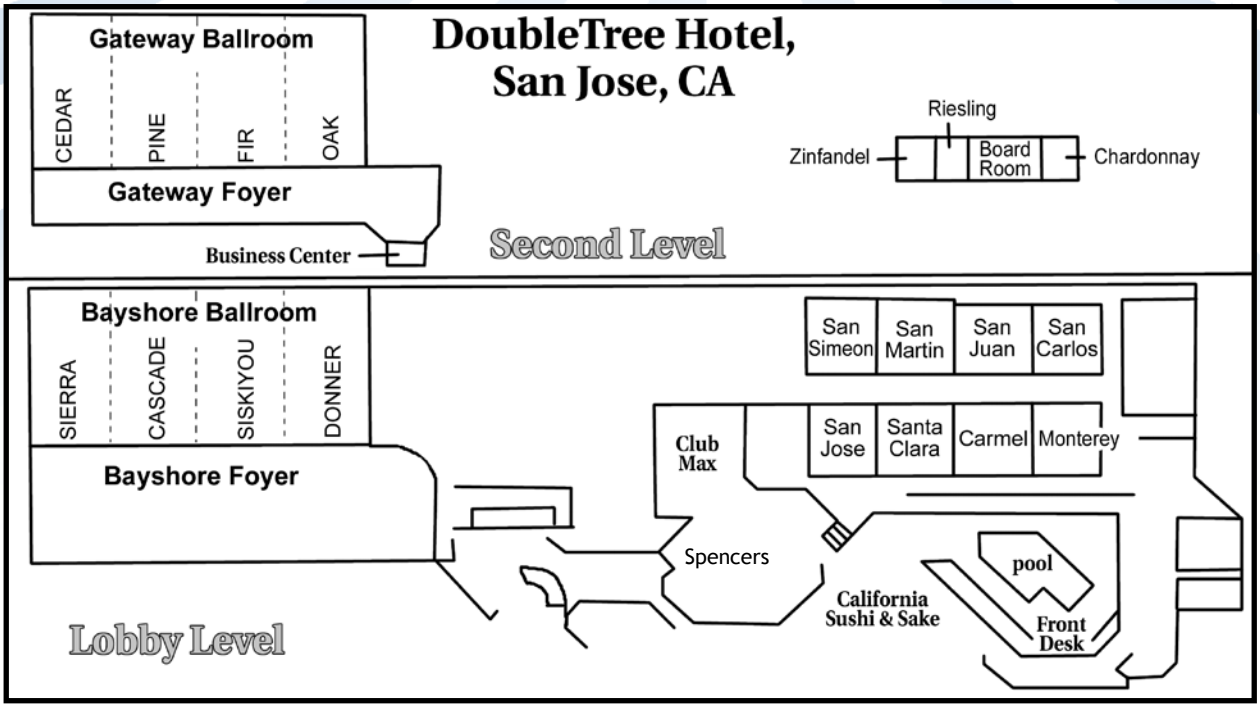
DoubleTree Hotel,
San Jose, CA
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Chardonnay
Second Level
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San Juan
San Carlos
San Jose
Santa Clara
Carmel
Monterey
Club Max
Spencers
California Sushi & Sake
pool
Front Desk
Lobby Level

Best Paper Candidates/Award Committee

Best Paper Award Committee

Louis Scheffer
Janelia Farms Research Campus
Howard Hughes Medical Institute
Ashburn, VA

Joel Phillips
Cadence Research Labs
Berkeley, CA

L. Miguel Silviera
INESC ID/IST
Lisboa, Portugal

Patrick Groeneveld
Magma Design Automation, Inc.
Santa Clara, CA

Sachin Sapatnekar
Univ. of Minnesota
Minneapolis, MN

Helmut Gräb
Technische Universität München
Munich, Germany

Michael Orshansky
Univ. of Texas
Austin, TX

IEEE/ACM William J. McCalla ICCAD Best Paper Award Candidates

Monday Sessions

2D.1 EFFICIENT BLOCK-BASED PARAMETERIZED TIMING ANALYSIS COVERING ALL POTENTIALLY CRITICAL PATHS

Khaled R. Heloue, Sari Onaissi, Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*

3A.1 PYRAMIDS: AN EFFICIENT COMPUTATIONAL GEOMETRY-BASED APPROACH FOR TIMING-DRIVEN PLACEMENT

Tao Luo - *Magma Design Automation, Inc. and Univ. of Texas, Austin, TX*
David A. Papa - *Univ. of Michigan, Ann Arbor, MI and IBM Corp., Austin, TX*
Zhuo Li, C. N. Sze, Charles J. Alpert - *IBM Corp., Austin, TX*
David Z. Pan - *Univ. of Texas, Austin, TX*

3D.1 STATISTICAL MODELING OF METAL-GATE WORK-FUNCTION VARIABILITY IN EMERGING DEVICE TECHNOLOGIES AND IMPLICATIONS FOR CIRCUIT DESIGN

Hamed Dadgour, Kaustav Banerjee - *Univ. of California, Santa Barbara, CA*
Vivek De - *Intel Corp., Hillsboro, OR*

Tuesday Sessions

4B.1 OPTIMIZATION-BASED FRAMEWORK FOR SIMULTANEOUS CIRCUIT-AND-SYSTEM DESIGN-SPACE EXPLORATION: A HIGH-SPEED LINK EXAMPLE

Ranko Sredojević, Vladimir Stojanović - *Massachusetts Institute of Tech., Cambridge, MA*

5C.1 SRAM DYNAMIC STABILITY: THEORY, VARIABILITY AND ANALYSIS

Wei Dong, Peng Li, Garng M. Huang - *Texas A&M Univ., College Station, TX*

6C.1 LAYOUT DECOMPOSITION FOR DOUBLE PATTERNING LITHOGRAPHY

Andrew B. Kahng, Chul-Hong Park, Hailong Yao - *Univ. of California, San Diego, La Jolla, CA*
Xu Xu - *Blaze DFM, Inc., Sunnyvale, CA*

7A.1 BSG-ROUTE: A LENGTH-MATCHING ROUTER FOR GENERAL TOPOLOGY

Tan Yan, Martin D.F. Wong - *Univ. of Illinois, Urbana-Champaign, IL*

Wednesday Sessions

8B.1 THERMALSCOPE: MULTI-SCALE THERMAL ANALYSIS FOR NANOMETER-SCALE INTEGRATED CIRCUITS

Nicholas Allec – *Queen's Univ., Kingston, ON, Canada*
Zyad Hassan, Li Shang, Ronggui Yang – *Univ. of Colorado, Boulder, CO*
Robert P. Dick - *Northwestern Univ., Evanston, IL*

8C.1 STATISTICAL PATH SELECTION FOR AT-SPEED TEST

Vladimir Zolotov, Jinjun Xiong, Chandu Visweswariah - *IBM Corp., T.J. Watson Research Center, Yorktown Hts., NY*
Hanif Fatemi – *Synopsys, Inc., Mountain View, CA*

8D.1 MULTIGRID ON GPU: TACKLING POWER GRID ANALYSIS ON PARALLEL SIMT PLATFORMS

Zhuo Feng, Peng Li - *Texas A&M Univ., College Station, TX*

9C.1 ROBUST FPGA RESYNTHESIS BASED ON FAULT-TOLERANT BOOLEAN MATCHING

Yu Hu, Zhe Feng, Lei He, Rupak Majumdar - *Univ. of California, Los Angeles, CA*

9D.1 GUARANTEED STABLE PROJECTION-BASED MODEL REDUCTION FOR INDEFINITE AND UNSTABLE LINEAR SYSTEMS

Bradley N. Bond, Luca Daniel - *Massachusetts Institute of Tech., Cambridge, MA*

Sunday, November 9, 2008

EDA Education and Research Workshop (EDA) - Colocated Workshop

9:00am - 6:00pm **Oak Ballroom**

Organizers: Satoshi Goto - *Waseda Univ., Kitakyusha, Japan*
Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

Sponsored by the Ministry of Education of Taiwan, Waseda University in Japan, National Taiwan University, and ICCAD, this workshop invites EDA educators and researchers to have a one-day forum on EDA education and research, including curriculum development, education/teaching experience sharing, recent research topics and directions for the next 10 years. The purpose is to connect worldwide EDA educators and researchers and to provide guidance for the aforementioned issues.

SESSION I: EDA EDUCATION PROGRAMS IN THE WORLD - *9:10 -11:10am*

Chair: Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
Speakers: Georges Gielen - *Katholieke Univ., Leuven, Belgium*
Sheqin Dong - *Tsinghua Univ., Beijing, China*
Shinji Kimura - *Waseda Univ., Kitakyushu, Japan*
Jong-Wha Chong - *Hangyang Univ., Seoul, Korea*
Jyuo-Min Shyu - *National Tsing Hua Univ., Hsinchu, Taiwan*

COFFEE BREAK: *11:00 - 11:30am*

SESSION II: FUTURE EDA EDUCATION AND RESEARCH DIRECTIONS FROM THE IEDM AND FOUNDRY PERSPECTIVE - *11:30am - 12:30pm*

Chair: Louis Scheffer - *Janelia Farms Research Campus, Ashburn, VA*
Speakers: Chuck Alpert - *IBM Corp., Austin, TX*
Kazutoshi Wakabayashi - *NEC Corp., Kanagawa, Japan*
David Lan - *TSMC Ltd., Hsinchu, Taiwan*

LUNCH: *12:30 - 2:00pm, Fir Ballroom*

SESSION III: FUTURE EDA EDUCATION AND RESEARCH DIRECTIONS FROM THE EDA VENDORS' PERSPECTIVES - *2:00 - 3:00pm*

Chair: Ting-Chi Wang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Speakers: Louis Scheffer - *Janelia Farms Research Campus, Ashburn, VA*
Patrick Groeneveld - *Magma Design Automation, Inc., San Jose, CA*
Charles Chiang - *Synopsys, Inc., Mountain View, CA*

COFFEE BREAK: *3:00 - 3:30pm*

SESSION IV: FUTURE EDA EDUCATION AND RESEARCH DIRECTIONS FROM THE ACADEMIC PERSPECTIVE - *3:30 - 5:50pm*

Chair: Satoshi Goto - *Waseda Univ., Kitakyusha, Japan*
Speakers: C. K. Cheng - *Univ. of California, San Diego, La Jolla, CA*
Giovanni De Micheli - *Ecole Polytèchniquè Federale de Lausanne, Lausanne, Switzerland*
Tei-Wei Kuo - *National Taiwan Univ., Taipei, Taiwan*
Malgorzata Marek-Sadowska - *Univ. Of California, Santa Barbara, CA*
Hidetoshi Onodera - *Kyoto Univ., Kyoto, Japan*
Jan Rabaey - *Univ. of California, Berkeley, CA*
Martin D. F. Wong - *Univ. of Illinois, Urbana-Champaign, IL*

CLOSING: *5:50 - 6:00pm*
Satoshi Goto - *Waseda Univ., Kitakyusha, Japan*

DINNER: *6:10 - 8:00pm, Fir Ballroom*

The CADathlon at ICCAD

ACM/SIGDA sponsors the seventh annual EDA programming contest at ICCAD

Sunday, November 9, 7:30am - 5:00pm Donner Ballroom

The CADathlon is a challenging, all-day, programming competition focusing on practical problems at the forefront of Computer-Aided Design, and Electronic Design Automation in particular. The contest emphasizes the knowledge of algorithmic techniques for CAD applications, problem-solving and programming skills, as well as teamwork.

In its seventh year as the "Olympic games of EDA", the contest brings together the best and the brightest of the next generation of CAD professionals. It gives academia and the industry a unique perspective on challenging problems and rising stars, and it also helps attract top graduate students to the EDA field.

The contest is open to two-person teams of graduate students specializing in CAD and currently full-time enrolled in a Ph.D. granting institution in any country. Students are selected based on their academic backgrounds and their relevant EDA programming experiences. Travel grants are provided to qualifying students.

The CADathlon competition consists of six problems in the following areas:

(1) circuit analysis

(2) physical design

(3) logic and behavioral synthesis

(4) system design and analysis

(5) functional verification

(6) timing, test, and manufacturing

More specific information about the problems and relevant research papers will be released on the Internet one week prior to the competition. The writers and judges that construct and review the problems are experts in EDA from both academia and industry. At the contest, students will be given the problem statements and example test data, but they will not have the judges' test data. Solutions will be judged on correctness and efficiency. Where appropriate, partial credit might be given. The team that earns the highest score is declared the winner. In addition to handsome trophies, the first place team's prize is a $2,000 cash award. The second place team's prize is a $1,000 cash award.

Contest winners will be announced at the ICCAD Opening Session on Monday morning and celebrated at the ACM/SIGDA Dinner and Member Meeting on Monday evening.

The CADathlon competition is sponsored by ACM/SIGDA and several Computer and EDA companies. For detailed contest information and sample problems from last year's competition, please visit the ACM/ SIGDA website at http://www.sigda.org/programs/cadathlon.

Or contact members of the **CADathlon organizing committee:**

Chair, Asst. Prof. Jennifer Dworak, Jennifer_Dworak@brown.edu

Vice Chair, Donald Chai, donald.chai@gmail.com

Vice Chair, Satrajit Chatterjee, satrajit.chatterjee@intel.com

Website Chair, Jarrod Roy, royj@eecs.umich.edu

SIGDA Liaison: Asst. Prof. Matthew Guthaus, mrg@soe.ucsc.edu

IEEE CEDA Reception

IEEE's Future in Electronic Design Automation

Sunday, November 9, 5:30 - 7:00pm ***Sierra Ballroom***

Organizers: Soha Hassoun - Tufts Univ., Medford, MA
Juan-Antonio Carballo - IBM Venture Capital Group., San Mateo, CA

Join us for the Annual Reception of the Council of Electronic Design Automation, IEEE's foremost institution in EDA, on Sunday November 9, 2008, at 5:30pm. We will offer drinks and hors d'oeuvres and plenty of opportunities to network with the industry's most respected technical leaders. We will start with a brief introduction to the Council's mission by our President John Darringer from IBM Corporation, followed by brief descriptions of the Council's activities by the Chairs of its respective committees. You will be able to meet in person the leaders of this IEEE organization and discuss the future of EDA and how you would like to shape it.

CEDA
IEEE Council on Electronic Design Automation

Monday, November 10, 2008

IEEE/ACM ICCAD 2008 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

Registration - 7:00am - 6:00pm (Bayshore Foyer) ***Technology Fair*** - 10:00am - 4:00pm (Gateway Foyer) **Speakers' Breakfast** - 7:30 - 8:30am (Siskiyou Ballroom)

8:30 **Opening Session and Keynote Address:** *CAD for Displays!* **(Oak/Fir Ballroom)**

10:00 **Mary Lou Jepsen** - *Founder and CEO of Pixel Qi, Previously Founding CTO of OLPC Project*

Break *Event supporter:* MAGMA

	Oak Ballroom	Fir Ballroom	Pine Ballroom	Cedar Ballroom	Donner Ballroom
10:30	**SESSION 1A**	**SESSION 1B**	**SESSION 1C**	**SESSION 1D**	**SESSION 1E**
	Floorplanning	Logic and High Level Synthesis	Test Power and Temperature Control	Simulation and Optimization of Analog Systems	Green Data Centers
12:00	**12:00 - 1:00pm Luncheon (Siskiyou Ballroom), 1:00 - 1:30pm Dessert (Technology Fair - Gateway Foyer)**				
1:30	**SESSION 2A**	**SESSION 2B**	**SESSION 2C**	**SESSION 2D**	**TUTORIAL 1**
	Physical Synthesis and Optimization	Decision Procedures in Verification	Power Estimation and Optimization	Recent Progress in SSTA	Reliable System Design: Models, Metrics and Design Techniques
3:30	**Break** *Event supporter:* SpringSoft				
4:00	**SESSION 3A**	**SESSION 3B**	**SESSION 3C**	**SESSION 3D**	**TUTORIAL 1 (CONT.)**
	Placement	Sequential Synthesis	System-level Thermal and Power Management	Modeling and Simulation of Process Variability	Reliable System Design: Models, Metrics and Design Techniques
5:00					
5:30					

Reception • **5:30 - 6:15pm**

PANEL: *MORE MOORE: FOOLISH, FEASIBLE, OR FUNDAMENTALLY DIFFERENT?* **6:15 - 7:15pm** (Oak/Fir Ballroom)

ACM/SIGDA DINNER with INVITED SPEAKER Edward J. McCluskey, the 2008 SIGDA Pioneering Achievement Award Recipient • **7:30pm** • **Siskiyou Ballroom**

Tuesday, November 11, 2008

Registration - 7:00am - 6:00pm (Bayshore Foyer) ***Technology Fair*** - 10:00am - 4:00pm (Gateway Foyer) **Speakers' Breakfast -** 7:30 - 8:30am (Siskiyou Ballroom)

	Oak Ballroom	Fir Ballroom	Pine Ballroom	Cedar Ballroom	Donner Ballroom
8:30	**SESSION 4A** Placement and Beyond	**SESSION 4B** Circuit and System Optimization and Modeling	**SESSION 4C** Embedded Tutorial: The New Memory Revolution. New Devices, Circuits and Systems		**TUTORIAL 2** Architecting Parallel Programs
10:00			**Break**		
10:30	**SESSION 5A** Global Routing	**SESSION 5B** System-level Simulation	**SESSION 5C** Analog and Memory Design Enablers	**SESSION 5D** Embedded Tutorial: Graphene Electronics: Design and CAD Challenges and Opportunities	**TUTORIAL 2 (CONT.)** Architecting Parallel Programs
12:00					
1:15	**Invited Luncheon Talk:** *Biology and the Environment: Frontiers for EDA?* **(Siskiyou Ballroom)** *Event supporter:* CEDA **Giovanni De Micheli** - *Professor and Director, Institute of Electrical Engneering, EPFL, Lausanne, Switzerland*				
1:30	**SESSION 6A** Physical Design for Performance Improvement and Noise Immunity	**SESSION 6B** Novel Design Methodologies for System Architecture	**SESSION 6C** DFM Methods for Advanced Lithography	**SESSION 6D** Designers' Panel: Challenges at 45nm and Beyond	**TUTORIAL 3** Embedded Software Verification: Challenges and Solutions
3:30			**Break**		
4:00	**SESSION 7A** Advances in Routing	**SESSION 7B** System-level Optimization Issues in Highly Parallel Architectures	**SESSION 7C** Advances in Embedded Systems	**SESSION 7D** Designers' Panel: Mixed-signal Simulation Challenges and Solutions (Ends at 5:30)	**TUTORIAL 3 (CONT.)** Embedded Software Verification: Challenges and Solutions
5:00					
6:00					
	ICCAD SOCIAL EVENT			**7:00pm, Siskiyou Ballroom**	

IEEE/ACM 2008 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

Wednesday, November 12, 2008

Registration - 7:00am - 4:00pm (Bayshore Foyer) **Speakers' Breakfast -** 7:30 - 8:30am (Siskiyou Ballroom)

	Oak Ballroom	Fir Ballroom	Pine Ballroom	Cedar Ballroom	Donner Ballroom
8:30	**SESSION 8A**	**SESSION 8B**	**SESSION 8C**	**SESSION 8D**	**TUTORIAL 4**
	Alternative Circuit Fabrics	Thermal Analysis and Optimization	Path Delay Anomaly Identification for Quality and Security	Techniques for Next Generation Interconnect Modeling	Nanolithography and CAD Challenges for 32nm/22nm and Beyond
10:00			**Break**		
10:30	**SESSION 9A**	**SESSION 9B**	**SESSION 9C**	**SESSION 9D**	**TUTORIAL 4 (CONT.)**
	Security Issues in ICs	Modeling Approaches for Reliability and Stress Analysis	Improving FPGA Reliability	Advances in Model Order Reduction	Nanolithography and CAD Challenges for 32nm/22nm and Beyond
12:00					
12:45	**12:00 - 12:45pm Luncheon (Siskiyou Ballroom)**				
	Keynote: *What Can Brain Researchers Learn from Computer Engineers and Vice Versa?* **(Oak Ballroom)**				
1:30	**Dmitri "Mitya" Chklovskii** - *Janelia Farm, Howard Hughes Medical Institute, Ashburn, VA*				
2:00	**SESSION 10A**	**SESSION 10B**	**SESSION 10C**	**SESSION 10D**	
	Design Techniques for Emerging Technologies	Embedded Tutorial: Learning from Silicon: Correlating Measurements, Models, and Design	Exploiting Logic Constraints for Noise Analysis	Advances in Oscillator Macromodeling	
3:30					
4:00	**VLSI-DAT SPECIAL SESSION**	*IEEE DATC Annual Meeting* • **6:00 - 7:30pm • Donner Ballroom**			
6:00		*EDA Bloggers' "Birds-of-a-Feather"* • **4:00 - 6:00pm • Fir Ballroom** *sponsored by* CEDA			

Monday, November 10, 2008

Technology Fair 10:00am - 4:00pm Gateway Foyer

8:30 - 10:00am • Opening Session/Awards • Oak/Fir Ballroom

Opening Remarks

Sani Nassif - **General Chair** - *IBM Corp., Austin, TX*

Award Presentations

IEEE/ACM William J. McCalla ICCAD Best Paper Award

This award is given in memory of William J. McCalla for his contributions to ICCAD and his CAD technical work throughout his career.

Bradley N. Bond and Luca Daniel

For the paper entitled, ***Guaranteed Stable Projection-based Model Reduction for Indefinite and Unstable Linear Systems***

Ranko Sredojević and Vladimir Stojanović

For the paper entitled, ***Optimization-based Framework for Simultaneous Circuit-and-System Design-space Exploration: A High-speed Link Example***

IEEE Transactions on Circuits and Systems Society 2008 Outstanding Young Author Award

Fei Su - *Intel Corp., Folsom, CA*

For the paper entitled, ***Defect Tolerance Based on Graceful Degradation and Dynamic Reconfiguration for Digital Microfluidics-based Biochips***, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 25, no. 12, pp. 2944-2953, December 2006 (with Krishnendu Chakrabarty).

2008 IEEE Fellow

Jacob White - *Massachusetts Institute of Tech., Cambridge, MA*

For contributions to simulation tools for RF circuits, electrical interconnects, and micro machined devices.

IEEE Circuits and Systems Society 2008 Mac Van Valkenburg Award

Jan M. Rabaey - *Univ. of California, Berkeley, CA*

For seminal contributions to the fields of VLSI implementation of signal processing and communication algorithms, design methodologies and computer-aided design tools, configurable computing, and low-power digital and RF circuit and system design. For his dedication to undergraduate and graduate education.

SIGDA Pioneering Achievement Award

Edward J. McCluskey - *Stanford Univ., Stanford, CA (emeritus)*

For outstanding contributions to the areas of CAD, test and reliable computing during the past half of century.

Keynote Address

CAD for Displays

Mary Lou Jepsen - *Founder and CEO of Pixel Qi, Previously Founding CTO of OLPC Project*

Keynote Address

8:30 - 10:00am • Monday, November 10 • Oak/Fir Ballroom

CAD for Displays!

Mary Lou Jepsen - *Founder and CEO of Pixel Qi, Previously Founding CTO of OLPC Project*

We take displays for granted in devices like our laptops, television, cell phones, and cars–to name a few places. The TFT LCD processes in use now are as mature as CMOS was 20 years ago, which is when we started seeing ASIC companies doing fabless chip design and investing heavily in CAD. Today, the display, as I believe I showed while working on the OLPC, is really just an ASIC!

Why focus on the display? The display is the most expensive and power-hungry component in your laptops, it can now be "taped out" just like an ASIC using standard TFT LCD fabs, and–in the limit–the laptop or the cell phone will become just a display to which the electronics are integrated. I believe that we are about to see a revolution in display design, with gradual subsumption of more and more of the CPU and motherboard electronics, to further drive down cost and power consumption.

In 2008, Time Magazine named Mary Lou Jepsen one of the 100 most influential people in the world for her work in starting Pixel Qi and previously as co-founder and CTO of One Laptop per Child. Pixel Qi is a new company that grew out of OLPC and is focused on creating innovative displays that can quickly get into mass production. Previously, Jepsen was lead innovator and architect of the lowest-cost, lowest-power, and greenest laptop ever made, making possible the distribution of millions of computers to children in developing countries. Notably she convinced Asian manufacturers to join the effort despite widespread disparagement about its viability, led the development of the laptop and saw it into mass production. She is also responsible for the most significant innovations in the laptop - the innovative sunlight-readable screen, and the laptop's power management system. She has a PhD in Optics and a BS in Electrical Engineering from Brown University and a MS in Holography from the MIT Media Lab.

Time: 10:30am to 12:00pm Room: Oak Ballroom

SESSION 1A • FLOORPLANNING

Moderators: Bill Halpin - *Synopsys, Inc., San Jose, CA*
Louis Scheffer - *Janelia Farm, Howard Hughes Medical Institute, Ashburn, VA*

Floorplanning has become an essential component of any successful integrated circuit design. Over the years, the problem has changed from focusing primarily on area utilization and compact representation, to one where objectives such as timing, power, and multiple voltage regions are considered. The papers in this session consider modern objectives, simplifying power optimization and adjusting block sizes while keeping the overall design compact.

1A.1 NETWORK FLOW-BASED POWER OPTIMIZATION UNDER TIMING CONSTRAINTS IN MSV-DRIVEN FLOORPLANNING

Qiang Ma (qma@cse.cuhk.edu.hk), Evangeline F.Y. Young - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

1A.2 LINEAR CONSTRAINT GRAPH FOR FLOORPLAN OPTIMIZATION WITH SOFT BLOCKS

Jia Wang (jwa112@eecs.northwestern.edu) - *Illinois Institute of Tech., Chicago, IL*
Hai Zhou - *Northwestern Univ., Evanston, IL*

1A.3 A NOVEL FIXED-OUTLINE FLOORPLANNER WITH ZERO DEADSPACE FOR HIERARCHICAL DESIGN

Ou He, Sheqin Dong (dongsq@mail.tsinghua.edu.cn) - *Tsinghua Univ., Beijing, China*
Satoshi Goto - *Waseda Univ., Kitakyushu, Japan*
Chung-Kuan Cheng - *Univ. of California, San Diego, La Jolla, CA*

Time: 10:30am to 12:00pm Room: Fir Ballroom

SESSION 1B • LOGIC AND HIGH-LEVEL SYNTHESIS

Moderators: Sunil P. Khatri - *Texas A&M Univ., College Station, TX*
Victor Kravets - *IBM Corp., T.J. Watson Research Center, Yorktown Hts., NY*

The first paper in the session presents a synthesis method for multi-cycle atomic actions. The second and third papers explore the decomposition space of Boolean functions. The last paper deals with the minimum number of variables required to represent a Boolean function.

1B.1 SYNTHESIS FROM MULTI-CYCLE ATOMIC ACTIONS AS A SOLUTION TO THE TIMING CLOSURE PROBLEM

Michal Karczmarek (karczma@alum.mit.edu), **Arvind** - *Massachusetts Institute of Tech., Cambridge, MA*

1B.2 TO SAT OR NOT TO SAT: ASHENHURST DECOMPOSITION IN A LARGE SCALE

Hsuan-Po Lin, Jie-Hong R. Jiang (jhjiang@cc.ee.ntu.edu.tw), Ruei-Rung Lee - *National Taiwan Univ., Taipei, Taiwan*

1B.3S BOOLEAN FACTORING AND DECOMPOSITION OF LOGIC NETWORKS

Alan Mishchenko (alanmi@eecs.berkeley.edu), **Robert K. Brayton** - *Univ. of California, Berkeley, CA*
Satrajit Chatterjee - *Intel Corp., Hillsboro, OR*

1B.4S ON THE NUMBERS OF VARIABLES TO REPRESENT SPARSE LOGIC FUNCTIONS

Tsutomu Sasao (sasao@cse.kyutech.ac.jp) - *Kyushu Institute of Tech., Ilzuka, Japan*

Time: 10:30am to 12:00pm Room: Pine Ballroom

SESSION 1C • TEST POWER AND TEMPERATURE CONTROL

Moderators: Kartik Mohanram - *Rice Univ., Houston, TX*
Jim Plusquellic - *Univ. of New Mexico, Albuquerque, NM*

The three papers in this session cover two hot topics in test. The first paper proposes a novel test relaxation method that reduces IR-drop by evenly distributing the X-bits across the test set. The second paper describes an approach for minimum-duration temperature-constrained test scheduling of MPSoCs. The last paper proposes a solution that simultaneously achieves test data compression and capture power reduction.

1C.1 EFFECTIVE IR-DROP REDUCTION IN AT-SPEED SCAN TESTING USING DISTRIBUTION-CONTROLLING X-IDENTIFICATION

Kohei Miyase (k_miyase@cse.kyutech.ac.jp), Yuta Yamato, Hiroshi Furukawa, Xiaoqing Wen, Seiji Kajihara - *Kyushu Institute of Tech., Iizuka, Japan*
Kenji Noda, Hideaki Ito, Kazumi Hatayama, Takashi Aikyo - *STARC, Yokohama, Japan*

1C.2 TEMPERATURE-AWARE TEST SCHEDULING FOR MULTIPROCESSOR SYSTEMS-ON-CHIP

David R. Bild (d-bild@u.northwestern.edu), Sanchit Misra, Prabhat Kumar, Robert P. Dick, Alok Choudhary - *Northwestern Univ., Evanston, IL*
Thidapat Chantem, X. Sharon Hu - *Univ. of Notre Dame, Notre Dame, IN*
Li Shang - *Univ. of Colorado, Boulder, CO*

1C.3 ON CAPTURE POWER-AWARE TEST DATA COMPRESSION FOR SCAN-BASED TESTING

Jia Li , Yu Hu, Xiaowei Li (lxw@ict.ac.cn) - *Chinese Academy of Sciences, Beijing, China*
Xiao Liu, Yubin Zhang, Qiang Xu - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

Time: 10:30am to 12:00pm Room: Cedar Ballroom

SESSION 1D • SIMULATION AND OPTIMIZATION OF ANALOG SYSTEMS

Moderators: Eric Grimme - *Intel Corp., Hillsboro, OR*
Saurabh Tiwary - *Cadence Research Labs, Berkeley, CA*

The first paper presents a new approach to speed up circuit simulation through parallelism. The next work extends the Pareto optimal method for hierarchical synthesis of mixed-signal designs. The final paper advances trajectory based nonlinear system modeling.

1D.1 MAPS: MULTI-ALGORITHM PARALLEL CIRCUIT SIMULATION

Xiaoji Ye (yexiaoji@tamu.edu)**,** Wei Dong, Peng Li - *Texas A&M Univ., College Station, TX*
Sani Nassif - *IBM Corp., Austin, TX*

1D.2 YIELD-AWARE HIERARCHICAL OPTIMIZATION OF LARGE ANALOG INTEGRATED CIRCUITS

Guo Yu (yuguo@neo.tamu.edu), Peng Li - *Texas A&M Univ., College Station, TX*

1D.3 MODEL REDUCTION VIA PROJECTION ONTO NON-LINEAR MANIFOLDS WITH APPLICATIONS TO ANALOG CIRCUITS AND BIO-CHEMICAL SYSTEMS

Chenjie Gu (gcj@umn.edu), Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*

Monday, November 10, 2008

Time: 10:30am to 12:00pm Room: Donner Ballroom

SESSION 1E • GREEN DATA CENTERS

Moderator: **Massoud Pedram** - *University of Southern California, Los Angeles, CA*

Presenters: **Greg Papadopoulos** - *Sun Microsystems, Santa Clara, CA*
Urs Holzle - *Google, Mountain View, CA*

The increasing demand for higher processing power and storage capacity, along with the shift to high-density computing, is driving the energy expenses of data centers through the roof. Indeed by the end of 2009, energy costs will emerge as the second-highest operating cost (behind labor) in 70% of datacenter facilities worldwide. According to an Environmental Protection Agency report, data centers in US alone consumed about 61 billion kilowatt-hours in 2006 for a total electricity cost of about $4.5 billion. If current trends continue, this demand would double by 2012. In an energy-constrained world, this level of consumption is unsustainable and comes at increasingly unacceptable social and environmental costs.

This session invites two industry leaders/visionaries to provide perspectives on this problem and highlight some of the promising hardware design technologies and system software strategies that could help rein in the energy consumption in data centers.

Visit www.iccad.com for presenter bios.

Time: 1:30 to 5:00pm Room: Donner Ballroom

Tutorial 1 - Reliable System Design: Models, Metrics and Design Techniques

Organizer: **Subhasish Mitra** – *Stanford Univ., Stanford, CA*

Presenters: **Ravishankar K. Iyer** – *Univ. of Illinois, Urbana-Champaign, IL*
Kishor Trivedi - *Duke Univ., Durham, NC*
James W. Tschanz - *Intel Corp., Hillsboro, OR*

Design of reliable systems meeting stringent quality, reliability, and availability requirements is becoming increasingly difficult in advanced technologies. The current design paradigm, which assumes that no gate or interconnect will ever operate incorrectly within the lifetime of a product, must change to cope with this situation. Future systems must be designed with built-in mechanisms for failure tolerance, prediction, detection and recovery during normal system operation.

This tutorial will focus on models and metrics for designing reliable systems, algorithms and tools for modeling and evaluating such systems. We will discuss a broad spectrum of techniques for building such systems with support for concurrent error detection, failure prediction, error correction, recovery, and self-repair. Complex interplay between power, performance and reliability requirements in future systems, and associated constraints will also be discussed.

Visit www.iccad.com for presenter bios.

Time: 1:30 to 3:30pm Room: Oak Ballroom

SESSION 2A • PHYSICAL SYNTHESIS AND OPTIMIZATION

Moderators: Masanori Hashimoto - *Osaka Univ., Suita, Japan*
Patrick Groeneveld - *Magma Design Automation, Inc., San Jose, CA*

Several novel ideas related to physical optimization for timing closure will be presented in this session. It starts with a novel approach that simultaneously considers buffering, cloning, cell replacement and sizing for timing optimization. The second paper unifies technology mapping and placement into a single step. A parallel approach towards discrete gate sizing is presented in the third paper of the session, while layer assignment is addressed in the next paper. The final paper questions the usefulness of traditional technology mapping, showing that small gates are preferable for timing and power consumption.

2A.1 ALGORITHMS FOR SIMULTANEOUS CONSIDERATION OF MULTIPLE PHYSICAL SYNTHESIS TRANSFORMS FOR TIMING CLOSURE

Huan Ren, **Shantanu Dutt** (dutt@ece.uic.edu) - *Univ. of Illinois, Chicago, IL*

2A.2 DELAY-OPTIMAL SIMULTANEOUS TECHNOLOGY MAPPING AND PLACEMENT WITH APPLICATIONS TO TIMING OPTIMIZATION

Yifang Liu, Jiang Hu - *Texas A&M Univ., College Station, TX*
Rupesh S. Shelar (rupesh.s.shelar@intel.com) - *Intel Corp., Hillsboro, OR*

2A.3 PARS: FAST AND NEAR-OPTIMAL GRID-BASED CELL SIZING FOR LIBRARY-BASED DESIGN

Tai-Hsuan Wu, Azadeh Davoodi (adavoodi@wisc.edu) - *Univ. of Wisconsin, Madison, WI*

2A.4S A POLYNOMIAL TIME APPROXIMATION SCHEME FOR TIMING CONSTRAINED MINIMUM COST LAYER ASSIGNMENT

Shiyan Hu (shiyan@mtu.edu) - *Michigan Technological Univ., Houghton, MI*
Zhuo Li, Charles J. Alpert - *IBM Corp., Austin, TX*

2A.5S ON THE DECREASING SIGNIFICANCE OF LARGE STANDARD CELLS IN TECHNOLOGY MAPPING

Jae-sun Seo (jseo@umich.edu), Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Igor L. Markov - *Univ. of Michigan, Ann Arbor, MI and Synopsys, Inc., Sunnyvale, CA*

Time: 1:30 to 3:30pm Room: Fir Ballroom

SESSION 2B • DECISION PROCEDURES IN VERIFICATION

Moderators: Sanjit Seshia - *Univ. of California, Berkeley, CA*
Chung-Yang (Ric) Huang - *National Taiwan Univ., Taipei, Taiwan*

Decision procedures for propositional logic (SAT) and finite-precision arithmetic play a central role in formal verification. This session includes four papers on this topic. The first paper uses a solver for polynomial congruences for the equivalence checking of arithmetic datapaths. The second paper integrates interpolation and abstraction techniques to speed up model checking. The third paper proposes an efficient memory model to speed up error diagnosis. The final paper uses SAT for the analysis of cyclic combinational circuits.

2B.1 VERIFICATION OF ARITHMETIC DATAPATHS USING POLYNOMIAL FUNCTION MODELS AND CONGRUENCE SOLVING

Neal Tew, **Priyank Kalla** (kalla@ece.utah.edu), Sivaram Gopalakrishnan - *Univ. of Utah, Salt Lake City, UT*
Namrata Shekhar - *Synopsys, Inc., Marlboro, MA*

2B.2 AUTOMATED ABSTRACTION BY INCREMENTAL REFINEMENT IN INTERPOLANT-BASED MODEL CHECKING

Marco Murciano (marco.murciano@polito.it), **Gianpiero Cabodi**, Paolo Camurati - *Politecnico di Torino, Torino, Italy*

2B.3 A SUCCINCT MEMORY MODEL FOR AUTOMATED DESIGN DEBUGGING

Brian Keng (briank@eecg.toronto.edu), Hratch Mangassarian, Andreas Veneris - *Univ. of Toronto, Toronto, ON, Canada*

2B.4 THE ANALYSIS OF CYCLIC CIRCUITS WITH BOOLEAN SATISFIABILITY

John D. Backes, Brian D. Fett (fett@umn.edu), Marc D. Riedel - *Univ. of Minnesota, Minneapolis, MN*

Time: 1:30 to 3:30pm Room: Pine Ballroom

SESSION 2C • POWER ESTIMATION AND OPTIMIZATION

Moderators: Jörg Henkel - *Univ. of Karlsruhe, Karlsruhe, Germany*
Youngsoo Shin - *KAIST, Daejeon, Republic of Korea*

This session addresses issues related to power estimation and optimization, ranging from on-chip power estimation to power reduction in pipelined systems and power gating techniques.

2C.1 SYSTEM-LEVEL POWER ESTIMATION USING AN ON-CHIP BUS PERFORMANCE MONITORING UNIT

Youngjin Cho, Younghyun Kim, Sangyoung Park, Naehyuck Chang (naehyuck@snu.ac.kr) - *Seoul National Univ., Seoul, Republic of Korea*

2C.2 MINIMIZING THE ENERGY COST OF THROUGHPUT IN A LINEAR PIPELINE BY OPPORTUNISTIC TIME BORROWING

Mohammad Ghasemaza (ghasemaz@usc.edu), **Massoud Pedram** - *Univ. of Southern California, Los Angeles, CA*

2C.3 ACCURATE ENERGY BREAKEVEN TIME ESTIMATION FOR RUN-TIME POWER GATING

Hao Xu (xuho@email.uc.edu), Wen-Ben Jone, Ranga Vemuri - *Univ. of Cincinnati, Cincinnati, OH*

2C.4 SIMULTANEOUS CONTROL OF POWER/GROUND CURRENT, WAKEUP TIME AND TRANSISTOR OVERHEAD IN POWER GATED CIRCUITS

Yongho Lee, Deog-Kyoon Jeong, Taewhan Kim (tkim@ssl.snu.ac.kr) - *Seoul National Univ., Seoul, Republic of Korea*

Time: 1:30 to 3:30pm Room: Cedar Ballroom

SESSION 2D • RECENT PROGRESS IN SSTA

Moderators: Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*
Dusan Petranovic - *Mentor Graphics Corp., San Jose, CA*

Statistical static timing analysis is a vital tool for addressing the impact of increasing variability. The first paper proposes an efficient algorithm, based on computational geometry, to calculate delay values at all possible process corners. The second paper develops a novel approach that applies gaussian processes to improve the accuracy of statistical timing analysis. The third paper borrows from the recently-developed compressed sensing technique to reduce post-silicon characterization cost. The last two papers discuss the merits of quasi Monte Carlo techniques for fast statistical timing analysis.

2D.1 ß EFFICIENT BLOCK-BASED PARAMETERIZED TIMING ANALYSIS COVERING ALL POTENTIALLY CRITICAL PATHS

Khaled R. Heloue, Sari Onaissi, Farid N. Najm (f.najm@utoronto.ca) - *Univ. of Toronto, Toronto, ON, Canada*

2D.2 ADJUSTMENT-BASED MODELING FOR STATISTICAL STATIC TIMING ANALYSIS WITH HIGH DIMENSION OF VARIABILITY

Lin Xie, **Azadeh Davoodi** (adavoodi@wisc.edu), Jun Zhang, Tai-Hsuan Wu - *Univ. of Wisconsin, Madison, WI*

2D.3 POST-SILICON TIMING CHARACTERIZATION BY COMPRESSED SENSING

Davood Shamsi, **Farinaz Koushanfar** (fk1@rice.edu), Petros Boufounos, Farinaz Koushanfar - *Rice Univ., Houston, TX*

2D.4S PRACTICAL, FAST MONTE CARLO STATISTICAL STATIC TIMING ANALYSIS: WHY AND HOW

Amith Singhee (asinghe@us.ibm.com) - *IBM Research, Yorktown Hts., NY*
Sonia Singhal, Rob A. Rutenbar - *Carnegie Mellon Univ., Pittsburgh, PA*

2D.5S ON EFFICIENT MONTE CARLO-BASED STATISTICAL STATIC TIMING ANALYSIS OF DIGITAL CIRCUITS

Javid Jaffari (jjaffari@vlsi.uwaterloo.ca), Mohab Anis - *Spry Design Automation and Univ. of Waterloo, Waterloo, ON, Canada*

Monday, November 10, 2008

Time: 4:00 to 5:30pm Room: Oak Ballroom

SESSION 3A • PLACEMENT

Moderators: Bill Halpin - *Synopsys, Inc., San Jose, CA*
Patrick Madden - *Binghamton Univ., Binghamton, NY*

Diving under the micron feature size has created more complicated design objectives, as well as problems of staggering complexity. Placement is in as much need of fresh ideas and implementation skills now as it was 45 years ago when design automation was born. In this session, timing, wire density, and the mix of sizes in placeable objects are all considered.

3A.1 ß PYRAMIDS: AN EFFICIENT COMPUTATIONAL GEOMETRY-BASED APPROACH FOR TIMING-DRIVEN PLACEMENT

Tao Luo (luotaok@hotmail.com) - *Magma Design Automation, Inc. and Univ. of Texas, Austin, TX*
David A. Papa - *Univ. of Michigan, Ann Arbor, MI and IBM Corp., Austin, TX*
Zhuo Li, C. N. Sze, Charles J. Alpert - *IBM Corp., Austin, TX*
David Z. Pan - *Univ. of Texas, Austin, TX*

3A.2 GUIDING GLOBAL PLACEMENT WITH WIRE DENSITY

Kalliopi Tsota (ktsota@purdue.edu), Cheng-Kok Koh - *Purdue Univ., West Lafayette, IN*
Venkataramanan Balakrishnan - *Purdue Univ., West Lafayette, IN*

3A.3 CONSTRAINT GRAPH-BASED MACRO PLACEMENT FOR MODERN MIXED-SIZE CIRCUIT DESIGNS

Yi-Lin Chuang, Hsin-Chen Chen, Yi-Lin Chuang, Yao-Wen Chang (ywchang@cc.ee.ntu.edu.tw) - *National Taiwan Univ., Taipei, Taiwan*
Yung-Chung Chang - *Genesys Logic, Inc., Taipei, Taiwan*

Time: 4:00 to 5:30pm Room: Fir Ballroom

SESSION 3B • SEQUENTIAL SYNTHESIS

Moderators: Timothy Kam - *Intel Corp., Hillsboro, OR*
Satrajit Chatterjee - *Intel Corp., Hillsboro, OR*

The first paper in the session explores clock skew scheduling for pulsed flip-flop circuits. The second paper explores sequential flexibility in clock-gating, while the last paper addresses robust verifiable synthesis.

3B.1 PULSE WIDTH ALLOCATION WITH CLOCK SKEW SCHEDULING FOR OPTIMIZING PULSED LATCH-BASED SEQUENTIAL CIRCUITS

Hyein Lee (hilee@dtlab.kaist.ac.kr), **Seungwhun Paik**, Youngsoo Shin - *KAIST, Daejeon, Republic of Korea*

3B.2 A NOVEL SEQUENTIAL CIRCUIT OPTIMIZATION WITH CLOCK GATING LOGIC

Yu-Min Kuo, Shih-Hung Weng, Shih-Chieh Chang (scchang@cs.nthu.edu.tw) - *National Tsing-Hua Univ., Hsinchu, Taiwan*

3B.3 SCALABLE AND SCALABLY-VERIFIABLE SEQUENTIAL SYNTHESIS

Alan Mishchenko (alanmi@eecs.berkeley.edu), Michael L. Case, Robert K. Brayton - *Univ. of California, Berkeley, CA*
Stephen Jang - *Xilinx, Inc., San Jose, CA*

Time: 4:00 to 5:30pm Room: Pine Ballroom

SESSION 3C • SYSTEM-LEVEL THERMAL AND POWER MANAGEMENT

Moderators: Naehyuck Chang - *Seoul National Univ., Seoul, Republic of Korea*
Jinfeng Liu - *Synopsys, Inc., Mountain View, CA*

This session addresses topics related to multi- and single-core system thermal management and power reduction for voltage-frequency island based network-on-chip systems.

ß3C.1 SYSTEM-LEVEL THERMAL AWARE DESIGN OF APPLICATIONS WITH UNCERTAIN EXECUTION TIMES

Sushu Zhang, Karam S. Chatha (kchatha@asu.edu) - *Arizona State Univ., Tempe, AZ*

3C.2 PROACTIVE TEMPERATURE BALANCING FOR LOW COST THERMAL MANAGEMENT IN MPSoCS

Ayse Kivilcim Coskun (acoskun@cs.ucsd.edu), Tajana Simunic Rosing - *Univ. of California, San Diego, La Jolla, CA*
Kenny C. Gross - *Sun Microsystems, Inc., San Diego, CA*

3C.3S A FRAMEWORK FOR PREDICTIVE DYNAMIC TEMPERATURE MANAGEMENT OF MICROPROCESSOR SYSTEMS

Omer Khan, Sandip Kundu (kundu@ecs.umass.edu) - *Univ. of Massachusetts, Amherst, MA*

3C.4S A VOLTAGE-FREQUENCY ISLAND AWARE ENGERY OPTIMIZATION FRAMEWORK FOR NETWORKS-ON-CHIP

Wooyoung Jang (wooyoung.jjang@gmail.com), Duo Ding, David Z. Pan - *Univ. of Texas, Austin, TX*

Time: 4:00 to 5:30pm Room: Cedar Ballroom

SESSION 3D • MODELING AND SIMULATION OF PROCESS VARIABILITY

Moderators: Eric R. Keiter - *Sandia National Labs, Albuquerque, NM*
Subarna Sinha - *Synopsys, Inc., Menlo Park, CA*

Variation modeling is an essential bridge between the underlying technology and robust design practice. This session presents four papers that address statistical modeling and simulation of emerging variability mechanisms in scaled CMOS design, including those related to the implementation of metal gates, random dopant fluctuations, and non-rectangular gates. Analysis at both device and circuit levels is explored to efficiently handle variations.

ß3D.1 STATISTICAL MODELING OF METAL-GATE WORK-FUNCTION VARIABILITY IN EMERGING DEVICE TECHNOLOGIES AND IMPLICATIONS FOR CIRCUIT DESIGN

Hamed Dadgour (hamed@ece.ucsb.edu), Vivek De, Kaustav Banerjee - *Univ. of California, Santa Barbara, CA*

3D.2 LARGE-SCALE ATOMISTIC APPROACH TO RANDOM-DOPANT-INDUCED CHARACTERISTIC VARIABILITY IN NANOSCALE CMOS DIGITAL AND HIGH-FREQUENCY INTEGRATED CIRCUITS

Yiming Li (ymli@faculty.nctu.edu.tw), Chih-Hong Hwang, Ta-Ching Yeh, Tien-Yeh Li - *National Chaio Tung Univ., Hsinchu, Taiwan*

3D.3S A NEW METHOD TO IMPROVE ACCURACY OF LEAKAGE CURRENT ESTIMATION FOR TRANSISTORS WITH NON-RECTANGULAR GATES DUE TO SUB-WAVELENGTH LITHOGRAPHY EFFECTS

Kuen-Yu Tsai (kytsai@cc.ee.ntu.edu.tw), Meng-Fu You, Yi-Chang Lu, Philip C.W. Ng - *National Taiwan Univ., Taipei, Taiwan*

3D.4S LINEAR ANALYSIS OF RANDOM PROCESS VARIABILITY

Victoria Wang (vluluw@ucla.edu), Dejan Marković - *Univ. of California, Los Angeles, CA*

ICCAD Panel: More Moore: Foolish, Feasible, or Fundamentally Different?

IEEE/ACM 2008 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

6:15 - 7:15pm • Oak/Fir Ballroom

Organizer: **Louis Scheffer** - *Janelia Farms Research Campus, Howard Hughes Medical Institute, Ashburn, VA*

Moderator: **Andreas Kuehlmann** - *Cadence Research Labs, Berkeley, CA*

Moore's law has been a foundation of modern electronics, sustained primarily by scaling. But can this continue despite the serious problems of lithography, variability, device physics, and cost? This panel looks at several possibilities. Perhaps Moore's law will muddle through, as it has so far, with a combination of tools, process, and design. But even if technically possible, Moore's law is in practice driven by economics, and economics might turn against further scaling. Also, we've all seen how performance of single cores has topped out, despite scaling. Might this be a fundamental problem with planar technologies, prompting the need to go 3-D to get further performance increases? Or might CMOS itself give way to other technologies, allowing Moore's law yet another respite?

Compare and contrast for yourself these four very different visions of the future of your job, your industry, and your personal gadgets.

Panelists: **Rob Aitken** - *ARM, Sunnyvale, CA*
Jerry R. Bautista - *Microprocessor Research, Intel Corp., Santa Clara, CA*
Wojceich Maly - *CMU, Pittsburgh, PA*
Jan M. Rabaey - *Univ. of California, Berkeley, CA*

Monday, November 10, 2008

Annual ACM/SIGDA Dinner at ICCAD

7:30pm

INVITED SPEAKER: Edward J. McCluskey **Siskiyou Ballroom**

2008 SIGDA Pioneering Achievement Award Recipient

Please join us for a unique event with Edward J. McCluskey, the recipient of this year's SIGDA Pioneering Achievement Award for his outstanding contributions to the areas of CAD, test and reliable computing during the past half of century.

Don't miss this unique event, along with a brief review of SIGDA's activities, and the winners of Sunday's SIGDA CADathlon.

The event is sponsored in part by the SIGDA Technical Committee on Testing and Reliable Design.

Dinner will be served to the first 80 attendees. Additional seating will be available to see the presentation only.

Please join us!

Sunday, November 9

The ACM/SIGDA Cadathlon
Sunday, November 9, 7:30am – 5:00pm
Donner Ballroom

IEEE CEDA Reception
IEEE's Future in Electronic Design Automation
Sunday, November 9, 5:30 - 7:00pm
Sierra Ballroom

Monday, November 10

46th DAC Technical Program Committee Meeting
Monday, November 10, 7:30 - 9:30pm
Donner Ballroom

ACM/SIGDA Dinner
Invited Speaker Edward J. McCluskey, the 2008 SIGDA Pioneering Achievement Award Recipient
Monday, November 10, 7:30 - 10:00pm
Siskiyou Ballroom

Tuesday, November 11

46th DAC Exhibitor Meeting
Tuesday, November 11, 1:30 - 2:30pm
San Martin/San Simeon Room

CANDE Meeting
Tuesday, November 11, 5:45 - 7:00pm
San Martin/San Simeon Room
CANDE is the Computer Aided Network Design Technical Committee of IEEE CAS and CEDA. CANDE is dedicated to bringing design automation professionals together to further their education, to assist in building relationships, and to sponsor initiatives that grow the CAD/EDA industry. CANDE sponsors a yearly workshop to address emerging technologies and to provide an opportunity for the generation of new ideas. Everyone is invited to attend the meeting on Tuesday evening, with an informal get together starting at 5:45pm and the meeting to start at 6:15pm. Meeting topics will include the recent (2008) workshop, initial planning for the 2009 workshop and CANDE officers. If you have an interest in the goals of CANDE, please plan to stop by!

Wednesday, November 12

EDA Bloggers' "Birds-of-a-Feather" Meeting
sponsored by CEDA
Wednesday, November 12, 4:00 - 6:00pm
Fir Ballroom

IEEE DATC Annual Meeting
Wednesday, November 12, 6:00 - 7:30pm
Donner Ballroom

Time: 8:30 to 10:00am Room: Oak Ballroom

SESSION 4A • PLACEMENT AND BEYOND

Moderators: Louis Scheffer - *Janelia Farm, Howard Hughes Medical Institute, Ashburn, VA*
Evangeline F.Y. Young - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

Research in design automation has always relied on strong background in combinatorial computation, optimization techniques and creative approaches. The papers in this session bring a fresh set of problems for the research community to consider. Approaches ranging from enumeration, to combinatorics, to game strategies provide fertile ground for further innovation and new applications.

4A.1 DESIGN AND OPTIMIZATION OF A DIGITAL MICROFLUIDIC BIOCHIP FOR PROTEIN CRYSTALLIZATION
Tao Xu (tx@ee.duke.edu) Krishnendu Chakrabarty - *Duke Univ., Durham, NC*
Vamsee K. Pamula - *Advanced Liquid Logic, RTP, NC*

4A.2 THERMAL-AWARE FLOORPLANNING FOR TASK MIGRATION ENABLED ACTIVE SUB-THRESHOLD LEAKAGE REDUCTION
Hushrav D. Mogal (mhush@umn.edu), Kia Bazargan - *Univ. of Minnesota, Minneapolis, MN*

4A.3 DETERMINISTIC ANALOG CIRCUIT PLACEMENT USING HIERARCHICALLY BOUNDED ENUMERATION AND ENHANCED SHAPE FUNCTIONS
Martin Strasser (strasser@tum.de), Michael Eick, Helmut Gräb, Ulf Schlichtmann, Frank M. Johannes - *Technische Universität München, Munich, Germany*

Time: 8:30 to 10:00am Room: Fir Ballroom

SESSION 4B • CIRCUIT AND SYSTEM OPTIMIZATION AND MODELING

Moderators: Elad Alon - *Univ. of California, Berkeley, CA*
Dejan Marković - *Univ. of California, Los Angeles, CA*

This session presents optimization-enabled advances in circuit and system design. The first paper provides an optimization framework to connect system-level parameters with the underlying circuit/process technology. The second paper describes an analysis framework for the effect of workload on power supply noise in multi-core processors. The third paper presents adaptive baseband DSP architectures and algorithms for robust low-power operation.

4B.1ß OPTIMIZATION-BASED FRAMEWORK FOR SIMULTANEOUS CIRCUIT-AND-SYSTEM DESIGN-SPACE EXPLORATION: A HIGH-SPEED LINK EXAMPLE
Ranko Sredojević (rasha@mit.edu), Vladimir Stojanović - *Massachusetts Institute of Tech., Cambridge, MA*

4B.2 BREAKING THE SIMULATION BARRIER: SRAM EVALUATION THROUGH NORM MINIMIZATION
Lara Dolecek (dolecek@mit.edu), Masood Qazi, Devavrat Shah, Anantha Chandrakasan - *Massachusetts Institute of Tech., Cambridge, MA*

4B.3 POWER SUPPLY NOISE AWARE WORKLOAD ASSIGNMENT FOR MULTI-CORE SYSTEMS
Aida Todri (atodri@ece.ucsb.edu), Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*
Joseph Kozhaya - *IBM Corp., T.J. Watson Research Center, Yorktown Hts., NY*

Time: 8:30 to 10:00am Room: Pine Ballroom

SESSION 4C • EMBEDDED TUTORIAL:

THE NEW MEMORY REVOLUTION. NEW DEVICES, CIRCUITS AND SYSTEMS

Moderator: Juan-Antonio Carballo - *IBM Venture Capital Group, San Francisco, CA*

Memory is undergoing a most spectacular revolution in technology. New types of memory devices, architectures, and protocols are springing rapidly and are expanding the breadth and depth of memory, increasingly replacing hard drives and more expensive, conventional memories. This tutorial will cover the emerging field of new memory, from the perspective of devices, architectures and protocols. Various approaches will be examined, including conventional CMOS SRAM/DRAM/Flash, MRAM, thyristor-based RAM, other MOS-based new devices, etc. The implications for design methodologies and design automation will be described in sufficient detail.

4C.1 INTRODUCTION
Jean-Pierre Nozieres (jpnozieres@crocus-technology.com) - *Crocus Tech., Grenoble, France*

4C.2 VOLATILE MEMORIES
Farid Nemati (farid@t-ram.com) - *T-RAM Semiconductor Inc., Milpitas, CA*

4C.3 SPECIAL ISSUES IN FLASH
Tei-Wei Kuo (ktw@csie.ntu.edu.tw) - *National Taiwan Univ., Taipei, Taiwan*

4C.4 SPECIAL ISSUES IN MRAM
Virgile Javerliac - *Crocus Tech., Grenoble, France*

Time: 8:30am to 12:00pm Room: Donner Ballroom

Tutorial 2 - Architecting Parallel Programs

Organizer: Joel Phillips - *Cadence Research Labs, Berkeley, CA*

Presenters: Kurt Keutzer - *Univ. of California, Berkeley, CA*

Tim G. Mattson - *Intel Corp., DuPont, WA*

Michael Wrinn - *Intel Corp., Hillsboro, OR*

The current shift from sequential to multicore and many-core processors presents serious challenges to software developers. A significant part of the industrial and research communities believes that either a) they can squeak by or b) the right compiler, parallel language etc. will save them. Such ad hoc responses are likely to prove neither correct nor sustainable. To systematically find and exploit parallelism, and to achieve forward scalability – that is, designs which efficiently scale to much larger numbers of cores -- will require re-architecting software applications such as EDA.

We believe that the key to re-architecting software is the use of design patterns and a pattern language. Furthermore, structural patterns (aka architectural styles) and computational patterns (aka the thirteen dwarfs) are the key high-level design patterns. The patterns are then used to create programming frameworks that can be used to facilitate implementation of the software architecture.

This tutorial presents the most recent research results by UC Berkeley and Intel. We will present our working pattern language and give examples on its use in EDA and other application areas.

Visit www.iccad.com for presenter bios.

Time: 10:30am to 12:00pm Room: Oak Ballroom

SESSION 5A • GLOBAL ROUTING

Moderators: Mustafa Ozdal - *Intel Corp., Hillsboro, OR*
Prashant Saxena - *Synopsys, Inc., Hillsboro, OR*

This session presents advances in global routing technology. The first paper proposes techniques for improved solution quality and fast convergence. The second paper introduces the novel concept of Virtual Capacity to guide the re-routing process. The third paper incorporates the notion of dynamic via capacity into the global routing formulation and presents novel approaches targeting multi-layer routing.

5A.1 NTHU - ROUTE 2.0: A FAST AND STABLE GLOBAL ROUTER

Yen-Jung Chang, Yu-Ting Lee, Ting-Chi Wang (tcwang@cs.nthu.edu.tw) - *National Tsing-Hua Univ., Hsinchu, Taiwan*

5A.2 FASTROUTE3.0: A FAST AND HIGH QUALITY GLOBAL ROUTER BASED ON VIRTUAL CAPACITY

Yanheng Zhang (zyh@iastate.edu), Yue Xu, Chris Chu - *Iowa State Univ., Ames, IA*

5A.3 MULTI-LAYER GLOBAL ROUTING CONSIDERING VIA AND WIRE CAPACITIES

Chin-Hsiung Hsu, Huang-Yu Chen, Yao-Wen Chang (ywchang@cc.ee.ntu.edu.tw) - *National Taiwan Univ., Taipei, Taiwan*

Time: 10:30am to 12:00pm Room: Fir Ballroom

SESSION 5B • SYSTEM-LEVEL SIMULATION

Moderator: Andreas Kuehlmann - *Cadence Research Labs, Berkeley, CA*

The ability to simulate at the system level is crucial to the development of systems on a chip. The first paper uses partial-order reduction to speed up race analysis of SystemC models. The second paper presents a simulator targeting dynamically configurable multi-core systems. The final paper addresses the problem of verifying correctness of bus-based systems in the presence of external interrupts.

5B.1 RACE ANALYSIS FOR SYSTEMC USING MODEL CHECKING

Nicolas Blanc - *ETH Zurich, Zurich, Switzerland*
Daniel Kroening (daniel.kroening@inf.ethz.ch) - *Oxford Univ., Oxford, United Kingdom*

5B.2 MC-SIM: AN EFFICIENT SIMULATION TOOL FOR MPSoC DESIGNS

Jason Cong, Karthik Gururaj (karthikg@cs.ucla.edu), **Guoling Han**, Adam Kaplan, Mishali Naik, Glenn Reinman - *Univ. of California, Los Angeles, CA*

5B.3 VERIFYING EXTERNAL INTERRUPTS OF EMBEDDED MICROPROCESSOR IN SoC WITH ON-CHIP BUS

Fu-Ching Yang (fcyang@esl.cse.nsysu.edu.tw), Jing-Kun Zhong, Ing-Jer Huang - *National Sun Yat-sen Univ., Kaohsiung, Taiwan*

Time: 10:30am to 12:00pm Room: Pine Ballroom

SESSION 5C • ANALOG AND MEMORY DESIGN ENABLERS

Moderators: Peter Feldmann - *IBM Corp., T.J. Watson Research Center, Yorktown Hts., NY*
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*

The first paper introduces tools to analyze the dynamic properties of memory circuits. The second paper generalizes the impulse sensitivity function technique to study the periodic behavior of circuits. The last two short papers propose unconventional analog design aids and methodologies.

5C.1 ß SRAM DYNAMIC STABILITY: THEORY, VARIABILITY AND ANALYSIS
Wei Dong, Peng Li (pli@neo.tamu.edu), Garng M. Huang - *Texas A&M Univ., College Station, TX*

5C.2 IMPULSE SENSITIVITY FUNCTION ANALYSIS OF PERIODIC CIRCUITS
Jaeha Kim (jaehak@rambus.com), Brian S. Leibowitz, Metha Jeeradit - *Rambus, Inc., Los Altos, CA*

5C.3S AUTOMATED EXTRACTION OF EXPERT KNOWLEDGE IN ANALOG TOPOLOGY SELECTION AND SIZING
Trent McConaghy (trent.mcconaghy@esat.kuleuven.be), Pieter Palmers, Michiel Steyaert, **Georges G. Gielen** - *Katholieke Univ., Leuven, Belgium*

5C.4S IMPORTANCE SAMPLED CIRCUIT LEARNING ENSEMBLES FOR ROBUST ANALOG IC DESIGN
Peng Gao (peng.gao@esat.kuleuven.be), Trent McConaghy, **Georges G. Gielen** - *Katholieke Univ., Leuven, Belgium*

Time: 10:30am to 12:00pm Room: Cedar Ballroom

SESSION 5D • EMBEDDED TUTORIAL: GRAPHENE ELECTRONICS: DESIGN AND CAD CHALLENGES AND OPPORTUNITIES

Moderators: Subhasish Mitra - *Stanford Univ., Stanford, CA*
R. Iris Bahar - *Brown Univ., Providence, RI*
Organizer: Kartik Mohanram - *Rice Univ., Houston, TX*

Graphene, which is a monolayer of carbon atoms packed into a two-dimensional honeycomb lattice, has emerged as a promising new electronic material because of its high mobility and saturation velocity, as well as, its potential for nearly ideal two-dimensional electrostatics. The three talks in this session will cover the latest technology and modeling advances in wafer-scale production of graphene films, engineering bandgaps, field-effect devices, graphene interconnects, and circuits exploiting graphene devices. The talks will also motivate challenges and opportunities facing the design and CAD communities.

5D.1 PHYSICAL MODELS FOR ELECTRON TRANSPORT IN GRAPHENE NANORIBBONS AND THEIR JUNCTIONS
Azad Naeemi (azad@ece.gatech.edu), James D. Meindl - *Georgia Institute of Tech., Atlanta, GA*

5D.2 GRAPHENE FIELD-EFFECT DEVICES FOR RF APPLICATIONS
Ken Shepard (shepard@ee.columbia.edu), Philip Kim, Inanc Meric - *Columbia Univ., New York, NY*

5D.3 GRAPHENE NANORIBBON FETS: TECHNOLOGY EXPLORATION AND CAD
Kartik Mohanram (kmram@rice.edu) - *Rice Univ., Houston, TX*
Jing Guo - *Univ. of Florida, Gainesville, FL*

Tuesday, November 11, 2008

Time: 12:00 to 1:15pm Room: Siskiyou Ballroom

INVITED LUNCHEON TALK: Biology and the Environment: Frontiers for EDA?

Speaker: Giovanni De Micheli - *Ecole Polytèchniquè Federale de Lausanne, Lausanne, Switzerland*

EDA has made possible the routine design of chips with billions of nano-scale devices, arguably the most complex man-made systems to date. However, improved quantitative understanding of biological and environmental systems has revealed complexities far beyond those in human-engineered systems. Prof De Micheli will show how EDA and CAD technologies are well-positioned to impact these new engineering frontiers.

Giovanni De Micheli is Professor and Director of the Institute of Electrical Engineering and of the Integrated Systems Centre at EPF Lausanne, Switzerland. He also chairs the Scientific Committee of CSEM, Neuchatel, Switzerland. Previously, he was Professor of Electrical Engineering at Stanford University. He holds a Nuclear Engineer degree (Politecnico di Milano, 1979), a M.S. and a Ph.D. degree in Electrical Engineering and Computer Science (University of California at Berkeley, 1980 and 1983.

Prof. De Micheli is the recipient of the 2003 IEEE Emanuel Piore Award for contributions to computer-aided synthesis of digital systems. He is a Fellow of ACM and IEEE. He received the Golden Jubilee Medal for outstanding contributions to the IEEE CAS Society in 2000. He received the 1987 D. Pederson Award for the best paper on the IEEE Transactions on CAD/ICAS, two Best Paper Awards at the Design Automation Conference, in 1983 and in 1993, and a Best Paper Award at the DATE Conference in 2005.

Event supporter:

CEDA
IEEE Council on Electronic Design Automation

Time: 1:30 to 3:30pm Room: Oak Ballroom

SESSION 6A • PHYSICAL DESIGN FOR PERFORMANCE IMPROVEMENT & NOISE IMMUNITY

Moderators: C. W. Jim Chang - *Synopsys, Inc., Mountain View, CA*
Shantanu Dutt - *Univ. of Illinois, Chicago, IL*

Papers in this session present advances in physical design for improving noise immunity and performance. Three of them target noise reduction in power/ground networks with the ultimate goal of performance improvement. The introduced concepts are: simultaneous assignment of clock-tree buffer polarities with clock-tree generation; consideration of density of signals rising in clock cycle time spans; and sensitivities of timing to decoupling capacitors across their physical locations and across clock cycle time spans. The fourth paper addresses post-placement rewiring of a class of multiplier circuits to improve timing. It also considers buffer insertion and can be interleaved with detailed placement.

6A.1 CLOCK BUFFER POLARITY ASSIGNMENT COMBINED WITH CLOCK TREE GENERATION FOR POWER/GROUND NOISE MINIMIZATION

Yesin Ryu, Taewhan Kim (tkim@ssl.snu.ac.kr) - *Seoul National Univ., Seoul, Republic of Korea*

6A.2 DECOUPLING CAPACITANCE ALLOCATION FOR TIMING WITH STATISTICAL NOISE MODEL AND TIMING ANALYSIS

Takashi Enami (enami.takashi@ist.osaka-u.ac.jp), Masanori Hashimoto - *Osaka Univ., Suita, Japan*
Takashi Sato - *Tokyo Institute of Tech., Yokohama, Japan*

6A.3 TRANSITION-AWARE DECOUPLING-CAPACITOR ALLOCATION IN POWER NOISE REDUCTION

Po-Yuan Chen (peter.pychen@gmail.com), Che-Yu Liu, TingTing Hwang - *National Tsing-Hua Univ., HsinChu, Taiwan*

6A.4 PLACEMENT BASED MULTIPLIER REWIRING FOR CELL-BASED DESIGNS

Fan Mo (fanmo@synplicity.com) - *Synplicity, Inc., Sunnyvale, CA*
Robert K. Brayton - *Univ. of California, Berkeley, CA*

Monday and Tuesday,
November 10 - 11
10:00am - 4:00pm
Gateway Foyer

Technology Fair

Face to face interaction builds future relationships.

The combination of technical sessions and the Technology Fair is an excellent opportunity for you to discuss the latest design challenges with key representatives from EDA companies. This intimate setting is specially designed for you to be able to create new business opportunities with top EDA technology visionaries.

Tuesday, November 11, 2008

All speakers are denoted in bold
S - denotes short paper
ß - denotes best paper candidate

Time: 1:30 to 3:30pm Room: Fir Ballroom

SESSION 6B • NOVEL DESIGN METHODOLOGIES FOR SYSTEM ARCHITECTURE

Moderators: Xiaojian Yang - *Synopsys, Inc., Sunnyvale, CA*
Helia Naeimi - *Intel Corp., Santa Clara, CA*

This session presents recent developments in design methodologies at the system level. The first paper presents a correct-by-construction method for architecture pipelining. The second paper discusses optimization issues in elastic systems. The next paper in the session presents optimization techniques for asynchronous architectures. The last paper discusses design automation issues in diastolic arrays.

6B.1 CORRECT-BY-CONSTRUCTION MICROARCHITECTURAL PIPELINING
Timothy Kam (timothy.kam@intel.com), Michael Kishinevsky - *Intel Corp., Hillsboro, OR*
Jordi Cortadella, Marc Galceran-Oms - *Universitat Politècnica de Catalunya, Barcelona, Spain*

6B.2 PERFORMANCE OPTIMIZATION OF ELASTIC SYSTEMS USING BUFFER RESIZING AND BUFFER INSERTION
Dmitry E. Bufistov, Jorge Júlvez, Jordi Cortadella - *Universitat Politècnica de Catalunya, Barcelona, Spain*

6B.3 PERFORMANCE ESTIMATION AND SLACK MATCHING FOR PIPELINED ASYNCHRONOUS ARCHITECTURES WITH CHOICE
Gennette D. Gill (gennette@gmail.com), Vishal Gupta, Montek Singh - *Univ. of North Carolina, Chapel Hill, NC*

6B.4 DIASTOLIC ARRAYS: THROUGHPUT-DRIVEN RECONFIGURABLE COMPUTING
Myong Hyon Cho (mhcho@mit.edu), Michel Kinsy, Srinivas Devadas - *Massachusetts Institute of Tech., Cambridge, MA*
Chih-Chi Cheng - *National Taiwan Univ., Taipei, Taiwan*
G. Edward Suh - *Cornell Univ., Ithaca, NY*

Time: 1:30 to 3:30pm Room: Pine Ballroom

SESSION 6C • DFM METHODS FOR ADVANCED LITHOGRAPHY

Moderators: Steffen Rochel - *Blaze DFM, Inc., Sunnyvale, CA*
Azadeh Davoodi - *Univ. of Wisconsin, Madison, WI*

This session features papers that propose novel DFM methods for advanced lithography. The first paper develops an algorithm for layout decomposition for double patterning lithography. The second paper describes an OPC algorithm targeting electrical performance. The third paper presents an efficient algorithm for inverse lithography. The fourth paper discusses the implications of double patterning on interconnect timing. The final paper proposes an exact method for shape manipulations.

6C.1 ß LAYOUT DECOMPOSITION FOR DOUBLE PATTERNING LITHOGRAPHY
Andrew B. Kahng, Chul-Hong Park (chpark@vlsicad.ucsd.edu), **Hailong Yao** - *Univ. of California, San Diego, La Jolla, CA*
Xu Xu - *Blaze DFM, Inc., Sunnyvale, CA*

6C.2 ELECTRICALLY DRIVEN OPTICAL PROXIMITY CORRECTION BASED ON LINEAR PROGRAMMING
Shayak Banerjee (shayak@mail.utexas.edu), Michael Orshansky - *Univ. of Texas, Austin, TX*
Praveen Elakkumanan, Lars W. Liebmann - *IBM Corp., Hopewell Junction, NY*

6C.3 A HIGHLY EFFICIENT OPTIMIZATION ALGORITHM FOR PIXEL MANIPULATION IN INVERSE LITHOGRAPHY TECHNIQUE
Jinyu Zhang (zhangjinyu@tsinghua.edu.cn), Wei Xiong, Yan Wang, Zhiping Yu - *Tsinghua Univ., Beijing, China*
Min-Chun Tsai - *Synopsys, Inc., Mountain View, CA*

6C.4S OVERLAY AWARE INTERCONNECT AND TIMING VARIATION MODELING FOR DOUBLE PATTERNING TECHNOLOGY
Jae-Seok Yang (jsyang74@gmail.com), David Z. Pan - *Univ. of Texas, Austin, TX*

6C.5S EXACT BASIC GEOMETRIC OPERATIONS ON ARBITRARY ANGLE POLYGONS USING ONLY FIXED SIZE INTEGER COORDINATES
Alexey Lvov (lvov@us.ibm.com), Ulrich Finkler - *IBM Corp., Yorktown Hts., NY*

Time: 1:30 to 3:30pm Room: Cedar Ballroom

SESSION 6D • DESIGNERS' PANEL: CHALLENGES AT 45NM AND BEYOND

Moderators: Mondira (Mandy) Deb Pant – *Intel Corp., Hudson, MA*
Mar Hershenson – *Magma Design Automation, Inc., San Jose, CA*

Presenters: Dan Bailey – *Advanced Micro Devices, Inc., Austin, TX*
Eric Soenen - *Taiwan Semiconductor Mfg. Co., Austin, TX*
Puneet Gupta - *Univ. of California, Los Angeles, CA*
Paul Villarrubia - *IBM Corp., Austin, TX*

Design at 45nm technologies and below is a risky proposition because of the many design challenges involved: variability, leakage, verification complexity, poor analog device performance, etc. In this panel, experienced designers coming from different backgrounds will talk about how they have overcome some of the design and CAD challenges in 45nm, what CAD challenges still exist and how the CAD community can help.

Visit www.iccad.com for presenter bios.

Time: 1:30 to 5:00pm Room: Donner Ballroom

Tutorial 3 - Embedded Software Verification: Challenges and Solutions

Organizers: Chao Wang – *NEC Labs America, Princeton, NJ*
Malay K. Ganai - *NEC Labs America, Princeton, NJ*

Presenters: Chao Wang – *NEC Labs America, Princeton, NJ*
Shuvendu Lahiri – *Microsoft Corp., Redmond, WA*
Daniel Kroening - *Oxford Univ., Oxford, United Kingdom*

Embedded software is becoming more and more pervasive in our lives, and many application domains have very high reliability requirements. Ensuring high software quality, while still maintaining software productivity, is a challenging task. In order to address this challenge, more formal analysis and automated verification techniques are needed in addition to standard software testing.

In this tutorial, we will showcase the important ideas and techniques of software formal verification, including static program analysis, program modeling and (bounded) model checking, and predicate abstraction refinement. We will emphasize some of the key techniques that have been successfully adopted by recent, industrial-strength software verification tools. We will focus on detecting bugs in sequential programs written in C/C++ for portable devices as well as for general purpose platforms.

The tutorial will be tailored to the ICCAD audience by emphasizing the use of decision procedures such as BDDs, Presburger arithmetic, bit-vector arithmetic, SAT and SMT solvers. Many of these techniques have been used in the context of analyzing, optimizing, and verifying IC designs.

By attending this tutorial, the audience will get a better understanding of the challenges and potential solutions of embedded software verification.

Time: 4:00 to 6:00pm Room: Oak Ballroom

SESSION 7A • ADVANCES IN ROUTING

Moderators: Chris Chu - *Iowa State Univ., Ames, IA*
Ting-Chi Wang - *National Tsing Hua Univ., Hsinchu, Taiwan*

This session addresses critical routing issues at various levels in modern designs. The first paper presents a general length-matching router for PCBs. The second paper considers the detailed routing problem in double patterning technology. The next two papers handle routing issues in the co-design of chip, package, and PCB. The last paper presents a new maze routing approach to construct obstacle-avoiding rectilinear Steiner trees.

7A.1 ß BSG-ROUTE: A LENGTH-MATCHING ROUTER FOR GENERAL TOPOLOGY

Tan Yan (tanyan2@uiuc.edu), Martin D.F. Wong - *Univ. of Illinois, Urbana-Champaign, IL*

7A.2 DOUBLE PATTERNING TECHNOLOGY FRIENDLY DETAILED ROUTING

Minsik Cho (thyeros@mail.cerc.utexas.edu), Yongchan Ban, David Z. Pan - *Univ. of Texas, Austin, TX*

7A.3 ROUTING FOR CHIP-PACKAGE-BOARD CO-DESIGN CONSIDERING DIFFERENTIAL PAIRS

Jia-Wei Fang, Kuan-Hsien Ho, Yao-Wen Chang (ywchang@cc.ee.ntu.edu.tw) - *National Taiwan Univ., Taipei, Taiwan*

7A.4S AREA-I/O FLIP-CHIP ROUTING FOR CHIP-PACKAGE CO-DESIGN

Jia-Wei Fang, Yao-Wen Chang (ywchang@cc.ee.ntu.edu.tw) - *National Taiwan Univ., Taipei, Taiwan*

7A.5S OBSTACLE-AVOIDING RECTILINEAR STEINER TREE CONSTRUCTION

Liang Li (lli@cse.cuhk.edu.hk), *Evangeline F. Y. Young - The Chinese Univ. of Hong Kong, Hong Kong*

Time: 4:00 to 6:00pm Room: Fir Ballroom

SESSION 7B • SYSTEM-LEVEL OPTIMIZATION ISSUES IN HIGHLY PARALLEL ARCHITECTURES

Moderators: Robert P. Dick - *Northwestern Univ., Evanston, IL*
Mike Kishinevsky - *Intel Corp., Hillsboro, OR*

The papers in this session describe optimization techniques for highly-parallel architectures. The first describes a post-fabrication technique to compensate for process variation. The second provides a formulation for multiprocessor performance optimization subject to thermal constraints. The third introduces an observability infrastructure for adaptive networks-on-chip. The fourth proposes a code compression algorithm for VLIW processors and the fifth investigates interconnection network synthesis for supercomputers.

7B.1 EVALUATION OF VOLTAGE INTERPOLATION TO ADDRESS PROCESS VARIATIONS

Kevin M. Brownell (brownell@eecs.harvard.edu), Gu-Yeon Wei, David Brooks - *Harvard/SEAS, Cambridge, MA*

7B.2 EFFICIENT ONLINE COMPUTATION OF CORE SPEEDS TO MAXIMIZE THE THROUGHPUT OF THERMALLY CONSTRAINED MULTI-CORE PROCESSORS

Ravishankar Rao (ravi.rao@asu.edu), Sarma Vrudhula - *Arizona State Univ., Tempe, AZ*

7B.3 ROADNOC: RUNTIME OBSERVABILITY FOR AN ADAPTIVE NETWORK ON CHIP ARCHITECTURE

Mohammad A. Al Faruque (alfaruque@informatik.uni-karlsruhe.de), Thomas Ebi, Jörg Henkel - *Univ. of Karlsruhe, Karlsruhe, Germany*

7B.4S FBT: FILLED BUFFER TECHNIQUE TO REDUCE CODE SIZE FOR VLIW PROCESSORS

Talal Bonny (bonny@ira.uka.de), Jörg Henkel - *Univ. of Karlsruhe, Karlsruhe, Germany*

7B.5S ADVANCING SUPERCOMPUTER PERFORMANCE THROUGH INTERCONNECTION TOPOLOGY SYNTHESIS

Yi Zhu (y2zhu@cs.ucsd.edu), Michael Taylor, Scott B. Baden, Chung-Kuan Cheng - *Univ. of California, San Diego, La Jolla, CA*

Time: 4:00 to 6:00pm Room: Pine Ballroom

SESSION 7C • ADVANCES IN EMBEDDED SYSTEMS

Moderators: James C. Hoe - *Carnegie Mellon Univ., Pittsburgh, PA*
Luca P. Carloni - *Columbia Univ., New York, NY*

This session features novel developments in embedded system design and analysis. The first paper presents a special-purpose cache architecture for texture mapping. The second paper proposes a software prefetching technique for scratch-pad memories. The third paper describes a stochastic approach to task allocation under process variations. The fourth paper applies game theory to the estimation of worst-case execution time in real-time applications. The final paper proposes a combined code and data placement algorithm for chip multiprocessors with two-dimensional mesh network-on-chip.

7C.1 TEXTURE FILTER MEMORY - A POWER-EFFICIENT AND SCALABLE TEXTURE MEMORY ARCHITECTURE FOR MOBILE GRAPHICS PROCESSORS

B.V.N. Silpa (silpa@cse.iitd.ac.in), Anjul Patney, Tushar Krishna, Preeti R. Panda, G. S. Visweswaran - *Indian Institute of Tech., New Delhi, India*

7C.2 SPM MANAGEMENT USING MARKOV CHAIN BASED DATA ACCESS PREDICTION

Taylan Yemlih - *Syracuse Univ., Syracuse, NY*
Shekhar Srikantaiah (srikanta@cse.psu.edu), Mahmut Kandemir - *Pennsylvania State Univ., University Park, PA*
Ozcan Ozturk - *Bilkent Univ., Ankara, Turkey*

7C.3 PROCESS VARIATION AWARE SYSTEM-LEVEL TASK ALLOCATION USING STOCHASTIC ORDERING OF DELAY DISTRIBUTIONS

Love Singhal (lsinghal@ics.uci.edu), Eli Bozorgzadeh - *Univ. of California, Irvine, CA*

7C.4S GAME-THEORETIC TIMING ANALYSIS

Sanjit A. Seshia (sseshia@eecs.berkeley.edu), Alexander Rakhlin - *Univ. of California, Berkeley, CA*

7C.5S INTEGRATED CODE AND DATA PLACEMENT IN TWO-DIMENSIONAL MESH BASED CHIP MULTIPROCESSORS

Taylan Yemlih - *Syracuse Univ., Syracuse, NY*
Shekhar Srikantaiah (srikanta@cse.psu.edu), Mahmut Kandemir, Mary Jane Irwin - *Pennsylvania State Univ., University Park, PA*
Mustafa Karakoy - *Imperial College, London, United Kingdom*

Time: 4:00 to5:30pm Room: Cedar Ballroom

SESSION 7D • DESIGNERS' PANEL: MIXED-SIGNAL SIMULATION CHALLENGES AND SOLUTIONS

Moderators: Mondira (Mandy) Deb Pant – *Intel Corp., Hudson, MA*
Mar Hershenson – *Magma Design Automation, Inc., San Jose, CA*

Presenters: Henry Chang – *Designer's Guide Consulting, Los Altos, CA*
William Walker - *Fujitsu Labs, Ltd., Sunnyvale, CA*
John G. Maneatis - *True Circuits, Inc., Los Altos, CA*
John Croix - *Nascentric, Inc., Austin, TX*

The design of complex mixed-signal systems-on-a-chip (SoC) poses challenging requirements on the simulation design environment. The simulation platform has to include simulations at the behavioral, gate and transistor-level which have traditionally been done in separate environments. As the scaling trend continues, the designer needs additional accuracy and capacity, new capabilities such as efficient statistical simulation that takes into account layout dependent effects. In this panel we have representatives from the CAD and design community discussing the challenges and current solutions available to the mixed-signal simulation challenge.

Visit www.iccad.com for presenter bios.

Wednesday, November 12, 2008

Time: 8:30 to 10:00am Room: Oak Ballroom

SESSION 8A • ALTERNATIVE CIRCUIT FABRICS

Moderators: Eli Bozorgzadeh - *Univ. of California, Irvine, CA*
Deming Chen - *Univ. of Illinois, Urbana, IL*

The papers in this session explore the use of emerging devices in the design of FPGAs, interconnect, and 3-D network-on-chips. The first paper proposes to combine CMOS and Spin Torque Transfer RAM (STTRAM) technology to design SRAM-based FPGAs. The second paper presents an accurate RC model for Graphene Nano-ribbon (GNR) interconnects. The third paper addresses yield issues due to the use of Through Silicon Via (TSV) based interconnects in 3-D networks-on-chip.

8A.1 HYBRID CMOS-STTRAM NON-VOLATILE FPGA: DESIGN CHALLENGES AND OPTIMIZATION APPROACHES

Somnath Paul (sxp190@case.edu), Swarup Bhunia - *Case Western Reserve Univ., Cleveland, OH*
Saibal Mukhopadhyay - *Georgia Institute of Tech., Atlanta, GA*

8A.2 ON THE MODELING OF RESISTANCE IN GRAPHENE NANORIBBON (GNR) FOR FUTURE INTERCONNECT APPLICATIONS

Tamer Ragheb, **Yehia Massoud** (massoud@rice.edu) - *Rice Univ., Houston, TX*

8A.3 A LOW-OVERHEAD FAULT TOLERANCE SCHEME FOR TSV-BASED 3-D NETWORK ON CHIP LINKS

Igor Loi (igor.loi@unibo.it), Luca Benini - *Univ. of Bologna, Bologna, Italy*
Shinobu Fujita - *Toshiba Corp., Kawasaki, Japan*
Subhasish Mitra, Thomas H. Lee - *Stanford Univ., Stanford, CA*

Time: 8:30 to 10:00am Room: Fir Ballroom

SESSION 8B • THERMAL ANALYSIS AND OPTIMIZATION

Moderators: David Atienza - *Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*
R. Iris Bahar - *Brown Univ., Providence, RI*

This session presents three papers on thermal analysis and optimization for nanoscale CMOS circuits. The first paper introduces a new multi-scale thermal analysis approach that combines Fourier and transport modeling methods. The next paper describes a parameterized transient thermal behavioral model for chip multiprocessors. The last paper proposes the use of task-sequencing as a mechanism complementary to voltage scaling for improving the thermal profile in embedded systems.

8B.1ß THERMALSCOPE: MULTI-SCALE THERMAL ANALYSIS FOR NANOMETER-SCALE INTEGRATED CIRCUITS

Nicholas Allec - *Queen's Univ., Kingston, ON, Canada*
Zyad Hassan, Li Shang (li.shang@colorado.edu), Ronggui Yang - *Univ. of Colorado, Boulder, CO*
Robert P. Dick - *Northwestern Univ., Evanston, IL*

8B.2 PARAMETERIZED TRANSIENT THERMAL BEHAVIORAL MODELING FOR CHIP MULTIPROCESSORS

Duo Li, Sheldon X.-D. Tan (stan@ee.ucr.edu) - *Univ. of California, Riverside, CA*
Eduardo Hernandez Pacheco, Murli Tirumala - *Intel Corp., Santa Clara, CA*

8B.3 TEMPERATURE AWARE TASK SEQUENCING AND VOLTAGE SCALING

Ramkumar Jayaseelan (ramkumar@comp.nus.edu.sg),
Tulika Mitra - *National Univ. of Singapore, Singapore*

Time: 8:30 to 10:00am Room: Pine Ballroom

SESSION 8C • PATH DELAY ANOMALY IDENTIFICATION FOR QUALITY AND SECURITY

Moderators: Alfred L. Crouch - *ASSET InterTech, Inc., Cedar Park, TX*
Xinli Gu - *Cisco Systems, Inc., San Jose, CA*

The trend of increasing levels of process variations challenges test methodologies designed to validate IC quality and security. The first paper proposes a novel branch-and-bound algorithm for optimally selecting paths for the detection of delay faults caused by process variations. Hardware security is addressed in the second paper where a transient power supply analysis and calibration technique is presented for identifying hardware Trojans using path delay tests. The third paper describes a ring oscillator-based approach for measuring the impact of process variations on critical path delays while calibrating for the delays of the loop-back structure.

8C.1 ß STATISTICAL PATH SELECTION FOR AT-SPEED TEST

Vladimir Zolotov, **Jinjun Xiong** (jinjun@us.ibm.com), Chandu Visweswariah - *IBM Corp., T.J. Watson Research Center, Yorktown Hts., NY*
Hanif Fatemi - *Synopsys, Inc., Mountain View, CA*

8C.2 POWER SUPPLY SIGNAL CALIBRATION TECHNIQUES FOR IMPROVING DETECTION RESOLUTION TO HARDWARE TROJANS

Reza M. Rad - *Univ. of Maryland, Baltimore, MD*
Xiaoxiao Wang, Mohammad Tehranipoor - *Univ. of Connecticut, Storrs, CT*
Jim Plusquellic (jimp@ece.unm.edu) - *Univ. of New Mexico, Albuquerque, NM*

8C.3 PATH-RO: A NOVEL ON-CHIP CRITICAL PATH DELAY MEASUREMENT UNDER PROCESS VARIATIONS

Xiaoxiao Wang, **Mohammad Tehranipoor** (tehrani@engr.uconn.edu) - *Univ. of Connecticut, Storrs, CT*
Ramyanshu Datta - *Texas Instruments, Inc., Dallas, TX*

Time: 8:30 to 10:00am Room: Cedar Ballroom

SESSION 8D • TECHNIQUES FOR NEXT GENERATION INTERCONNECT MODELING

Moderators: Peter Feldmann - *IBM Corp., T.J. Watson Research Center, Yorktown Hts., NY*
Zhenhai Zhu - *Cadence Research Labs, Berkeley, CA*

This session features techniques for enabling next generation interconnect technology. The first paper presents an efficient power grid analysis technique running on a GPU platform. The second paper describes an efficient method for predicting eye diagrams for high speed communication. The last paper presents a floating random walk method for fast incremental variational capacitance extraction.

8D.1ß MULTIGRID ON GPU: TACKLING POWER GRID ANALYSIS ON PARALLEL SIMT PLATFORMS

Zhuo Feng (fengzhuo@neo.tamu.edu), Peng Li - *Texas A&M Univ., College Station, TX*

8D.2 EFFICIENT AND ACCURATE EYE DIAGRAM PREDICTION FOR HIGH SPEED SIGNALING

Rui Shi (rshi@cs.ucsd.edu), Yi Zhu, Chung-Kuan Cheng - *Univ. of California, San Diego, La Jolla, CA*
Wenjian Yu - *Tsinghua Univ., Beijing, China*
Ernest S. Kuh - *Univ. of California, Berkeley, CA*

8D.3 A CAPACITANCE SOLVER FOR INCREMENTAL VARIATION-AWARE EXTRACTION

Tarek A. El-Moselhy (tmoselhy@mit.edu), Luca Daniel - *Massachusetts Institute of Technology, Cambridge, MA*
Abe Elfadel - *IBM Corp., Yorktown Hts., NY*

Wednesday, November 12, 2008

Time: 8:30am to 12:00pm Room: Donner Ballroom

Tutorial 4 - Nanolithography and CAD Challenges for 32nm/22nm and Beyond

Organizer: David Z. Pan - *Univ. of Texas, Austin, TX*

Presenters: Stephen Renwick - *Nikon Precision, Inc., Belmont, CA*
Vivek Singh - *Intel Corp., San Jose, CA*
Judy Huckabay - *Cadence Design Systems, Inc., San Jose, CA*

The semiconductor industry is stuck at 193nm lithography as the main workhorse for manufacturing integrated circuits of 45nm and most likely 32nm nodes. On one hand, many novel approaches are being developed to extend the 193nm lithography, including immersion, double patterning, and exotic resolution enhancement techniques. On the other hand, next generation lithography, in particular, extreme ultra violet lithography (EUVL) is projected by ITRS as the main contender for technology nodes at or below 22nm, though significant challenges still exist from both technology and economy aspects.

This tutorial will cover key nanolithography and CAD challenges with possible solutions for 32nm/22nm (and beyond?), from the underlying hardware/equipment perspectives (for double patterning, EUV, and so on), to the computational lithography aspects (extreme RET, inverse lithography, pixelated mask, etc.), and to the key EDA issues in nanolitho-friendly layouts (e.g., double patterning compliance layout, and so on).

Visit www.iccad.com for presenter bios.

Time: 10:30am to 12:00pm Room: Oak Ballroom

SESSION 9A • SECURITY ISSUES IN ICS

Moderators: Mondira (Mandy) Deb Pant - *Intel Corp., Hudson, MA*
Seda Memik - *Northwestern Univ., Evanston, IL*

This session presents three papers on piracy, authentication, cryptography, and other security related issues in integrated circuits. The first paper develops a methodology for designing physically unclonable functions (PUF) that find use in authentication of ICs. The second paper proposes the use of a smartly inserted FSM to prevent piracy of IP and ICs. The third paper exploits the availability of multiple cores to provide robustness to side-channel attacks in cryptography applications.

9A.1 LIGHTWEIGHT SECURE PUFS

Mehrdad Majzoobi (m.majzoobi@gmail.com), Farinaz Koushanfar - *Rice Univ., Houston, TX*
Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

9A.2 HARDWARE PROTECTION AND AUTHENTICATION THROUGH NETLIST LEVEL OBFUSCATION

Rajat Subhra Chakraborty (rsc22@case.edu), Swarup Bhunia - *Case Western Reserve Univ., Cleveland, OH*

9A.3 MUTE-AES: A MULTIPROCESSOR ARCHITECTURE TO PREVENT POWER ANALYSIS BASED SIDE CHANNEL ATTACK OF THE AES ALGORITHM

Jude Angelo Ambrose (ajangelo@cse.unsw.edu.au), Sridevan Parameswaran, Aleksandar Ignjatovic - *Univ. of New S. Wales, Sydney, Australia*

Time: 10:30am to 12:00pm Room: Fir Ballroom

SESSION 9B • MODELING APPROACHES FOR RELIABILITY AND STRESS ANALYSIS

Moderators: Arijit Raychowdhury - *Intel Corp., Hillsboro, OR*
Eli Bozorgzadeh - *Univ. of California, Irvine, CA*

This session covers analysis of stress, transient faults and oxide failures in nano-scale CMOS. The first paper presents a statistical framework for chip level reliability analysis. The second paper addresses the development of cell library elements in stress-enhanced silicon technologies. The third paper proposes a symbolic approach to modeling the effect of transient faults in digital circuits.

9B.1 PROCESS VARIABILITY-AWARE TRANSIENT FAULT MODELING AND ANALYSIS

Natasa Miskov-Zivanov (nmiskov@ece.cmu.edu), Kai-Chiang Wu, Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

9B.2 STEEL: A TECHNIQUE FOR STRESS-ENHANCED STANDARD CELL LIBRARY DESIGN

Brian T. Cline (btcline@umich.edu), Vivek Joshi, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

9B.3 A STATISTICAL APPROACH FOR FULL-CHIP GATE-OXIDE RELIABILITY ANALYSIS

Kaviraj Chopra, Cheng Zhuo (hzzc1012@hotmail.com), David Blaauw, Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*

Time: 10:30am to 12:00pm Room: Pine Ballroom

SESSION 9C • IMPROVING FPGA RELIABILITY

Moderators: Sherief Reda - *Brown Univ., Providence , RI*
Rajeev Jayaraman - *Xilinx, Inc., San Jose, CA*

Reliability is of rising concern in sub-100nm technologies. This session highlights new advances for improved reliability in FPGAs. The first paper uses SAT techniques for FPGA mapping to increase tolerance to permanent and transient defects in FPGA configuration cells. The second paper presents new placement techniques for more robust layouts. The last paper is concerned with analyzing the impact of temperature variations on the reliability of FPGAs.

9C.1ß ROBUST FPGA RESYNTHESIS BASED ON FAULT-TOLERANT BOOLEAN MATCHING

Yu Hu (huyu.cs@gmail.com), Zhe Feng, Lei He, Rupak Majumdar - *Univ. of California, Los Angeles, CA*

9C.2 FAULT TOLERANT PLACEMENT AND DEFECT RECONFIGURATION FOR NANO-FPGAS

Amit K. Agarwa, **Jason Cong** (cong@cs.ucla.edu), Brian Tagiku - *Univ. of California, Los Angeles, CA*

9C.3 THERMAL-AWARE RELIABILITY ANALYSIS FOR PLATFORM FPGAs

Prasanth Mangalagiri (mangalag@cse.psu.edu), Sungmin Bae, Ramakrishnan Krishnan, Yuan Xie, Vijaykrishnan Narayanan - *Pennsylvania State Univ., State College, PA*

Time: 10:30am to 12:00pm Room: Cedar Ballroom

SESSION 9D • ADVANCES IN MODEL ORDER REDUCTION

Moderators: Yaping Zhan - *Advanced Micro Devices, Inc., Austin, TX*
Amith Singhee - *IBM Corp., T.J. Watson Research Center, Yorktown Hts., NY*

The three papers in this session introduce efficient model order reduction techniques for solving large linear systems arising from common industrial size problems. The first paper uses linear projection matrix constraints to guarantee stability in an efficient manner. The second paper employs the Sparse Implicit Projection method to greatly speed up reduction of general many terminal networks. The third paper introduces a novel use of inputs and outputs to identify locally dominant Krylov subspaces.

9D.1ß GUARANTEED STABLE PROJECTION-BASED MODEL REDUCTION FOR INDEFINITE AND UNSTABLE LINEAR SYSTEMS

Bradley N. Bond (bnbond@mit.edu), Luca Daniel - *Massachusetts Institute of Tech., Cambridge, MA*

9D.2 SPARSE IMPLICIT PROJECTION (SIP) FOR REDUCTION OF GENERAL MANY-TERMINAL NETWORKS

Zuochang Ye, Zhenhai Zhu (zhzhu@cadence.com), Joel R. Phillips - *Cadence Research Labs, Inc., Berkeley, CA*
Dmitry Vasilyev - *Massachusetts Institute of Tech., MA*

9D.3 MODELING AND SIMULATION FOR ON-CHIP POWER GRID NETWORKS BY LOCALLY DOMINANT KRYLOV SUBSPACE METHOD

Boyuan Yan (byan@ee.ucr.edu), Sheldon X. -D. Tan - *Univ. of California, Riverside, CA*
Gengsheng Chen - *Fudan Univ., Shanghai, China*
Lifeng Wu - *Cadence Design Systems, Inc., San Jose, CA*

12:45 - 1:30pm • Oak Ballroom

What Can Brain Researchers Learn from Computer Engineers and Vice Versa?

Dmitri "Mitya" Chklovskii - *Janelia Farm, Howard Hughes Medical Institute, Ashburn, VA*

The human brain is a network containing a hundred billion neurons, each communicating with several thousand others. As the wiring for neuronal communication draws on limited space and energy resources, evolution had to optimize their use. This principle of minimizing wiring costs, similar to that in computer design, explains many features of brain architecture, including placement and shape of many neurons. However, the shape of some neurons and their synaptic properties remained unexplained. This led us to the principle of maximization of brain's ability to store information. Combination of the two principles provides a systematic view of brain architecture, necessary to explain brain function. It would be interesting to see whether advances in understanding brain function will make impact on computer design.

Dmitri "Mitya" Chklovskii earned his PhD in Theoretical Physics from MIT in 1994. While being a Junior Fellow of the Harvard Society of Fellows, he got fascinated by the enigma of the human brain. In 1999, after being a Sloan Fellow at the Salk Institute, he founded a Theoretical Neuroscience group at Cold Spring Harbor Laboratory. In 2007, he became a group leader at Janelia Farm, a new interdisciplinary campus of the Howard Hughes Medical Institute in the suburbs of Washington DC. He is known for pioneering application of engineering principles to understand brain design.

Time: 2:00 to 3:30pm Room: Oak Ballroom

SESSION 10A • DESIGN TECHNIQUES FOR EMERGING TECHNOLOGIES

Moderators: Jaeha Kim - *Rambus, Inc., Los Altos, CA*
Ken Shepard - *Columbia Univ., New York, NY*

This session presents novel ideas in circuits and nano/bio systems. The first paper demonstrates the use of nano-mechanical relay devices to achieve order of magnitude improvements in energy-efficiency over conventional CMOS. The second paper introduces novel hand-shaking mechanisms for synthetic biochemical circuits. The third paper applies process-aware optimization techniques to design reconfigurable RF filters.

10A.1 INTEGRATED CIRCUIT DESIGN WITH NEM RELAYS

Fred Chen (fredchen@mit.edu), Vladimir Stojanović - *Massachusetts Institute of Tech., Cambridge, MA*
Hei Kam, Tsu-Jae King Liu, Elad Alon - *Univ. of California, Berkeley, CA*
Dejan Marković - *Univ. of California, Los Angeles, CA*

10A.2 MODULE LOCKING IN BIOCHEMICAL SYNTHESIS

Brian D. Fett (fett@umn.edu), **Marc D. Riedel** - *Univ. of Minnesota, Minneapolis, MN*

10A.3 ROBUST RECONFIGURABLE FILTER DESIGN USING ANALYTIC VARIABILITY QUANTIFICATION TECHNIQUES

Arthur Nieuwoudt, Yehia Massoud (massoud@rice.edu) - *Rice Univ., Houston, TX*
Jamil Kawa - *Synopsys, Inc., Mountain View, CA*

Time: 2:00 to 3:30pm Room: Fir Ballroom

SESSION 10B • EMBEDDED TUTORIAL: LEARNING FROM SILICON: CORRELATING MEASUREMENTS, MODELS AND DESIGN

Moderator: Eli Chiprout - *Intel Corp., Hillsboro, OR*

This tutorial will describe the thinking and methods of how to get silicon measured feedback back into the design and test tools, algorithms and flows. The first talk will address how electrical test data can be fed back to the design process to improve manufacturability. It will focus on data from product-level test and scribe-line or on-product test structures and will address both defect-related and parametric/variability yield issues. The second talk will detail modeling and analysis of systematic manufacturing variations induced by lithography. The variability analysis of layout dependent impact on design parametric behavior enables designers to make layout and circuit modifications to ensure robustness of cells and design through process window and pattern-dependent variation. The third talk will feature the process by which one can identify speed-limiting paths on silicon and capture their main electrical effects in order to deduce some features of the design as silicon technology.

10B.1 USING TEST DATA TO IMPROVE IC QUALITY AND YIELD

Anne Gattiker - *IBM Corp., Austin, TX*

10B.2 MODELING AND ANALYSIS OF SYSTEMATIC VARIATIONS FOR ROBUST DESIGNS

Arjun Rajagopal, Mark Terry, Aniket Saha - *Texas Instruments, Inc., Dallas, TX*
Nishath Verghese - *Cadence Design Systems, Inc., San Jose, CA*

10B.3 SILICON FEEDBACK TO IMPROVE FREQUENCY OF HIGH-PERFORMANCE MICROPROCESSORS - AN OVERVIEW

Chandramouli Kashyap, Kip Killpack, Chirayu S. Amin - *Intel Corp., Hillsboro, OR*
Pouria Bastani - *Univ. of California, Santa Barbara, CA*

Time: 2:00 to 3:30pm Room: Pine Ballroom

SESSION 10C • EXPLOITING LOGIC CONSTRAINTS FOR NOISE ANALYSIS

Moderators: Sheldon Tan - *Univ. of California, Riverside, CA*
Zhenhai Zhu - *Cadence Research Labs, Berkeley, CA*

This session brings together different techniques to exploit logic constraints in efficient noise analysis and simulation. The first paper uses a gain guided backtrack search technique for logic exclusivity. The second paper maximizes crosstalk noise on a coupled victim net under logical constraints. The third paper introduces a novel static transistor-level IR drop analysis flow.

10C.1 INCORPORATING LOGIC EXCLUSIVITY (LE) CONSTRAINTS IN NOISE ANALYSIS USING GAIN GUIDED BACKTRACKING METHOD

Ruiming Li (Ruiming.Li@sun.com), An-Jui Shey, Michel Laudes - *Sun Microsystems, Inc., Santa Clara, CA*

10C.2 CONSTRAINED AGGRESSOR SET SELECTION FOR MAXIMUM COUPLING NOISE

Debjit Sinha (debjitsinha@yahoo.com), Gregory Schaeffer, Soroush Abbaspour - *IBM Corp., Hopewell Jct., NY*
Frank Borkam - *BM Corp., San Mateo, CA*
Alex Rubin - *IBM Corp., San Jose, CA*

10C.3 CONTEXT-SENSITIVE STATIC TRANSISTOR-LEVEL IR ANALYSIS

Weiqing Guo (weiqing.guo@amd.com), Tom Burd - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Yu Zhong - *Univ. of Illinois, Urbana, IL*

Time: 2:00 to 3:30pm Room: Cedar Ballroom

SESSION 10D • ADVANCES IN OSCILLATOR MACROMODELING

Moderators: Saurabh Tiwary - *Cadence Research Labs, Berkeley, CA*
Peng Li - *Texas A&M Univ., College Station , TX*

The first two papers improve and extend existing oscillator macromodeling techniques for phase noise analysis. The last paper applies oscillator macromodeling to the analysis of large coupled networks including biological systems.

10D.1 FREQUENCY-AWARE PPV: A ROBUST PHASE MACROMODEL FOR ACCURATE OSCILLATOR NOISE ANALYSIS

Xiaolue Lai (laizl@umn.edu) - *Cadence Design Systems, Inc., San Jose, CA*

10D.2 SMOOTHED FORM OF NONLINEAR PHASE MACROMODEL FOR OSCILLATORS

Mark M. Gourary, Sergey G. Rusakov (ulyas@ippm.ru), Sergey L. Ulyanov, Michael M. Zharov - *IPPM RAS, Moscow, Russian Federation*
Brian Mulvaney, Kiran K. Gullapalli - *Freescale Semiconductor, Inc., Austin, TX*

10D.3 COMPREHENSIVE PROCEDURE FOR FAST AND ACCURATE COUPLED OSCILLATOR NETWORK SIMULATION

Prateek Bhansali (bhansali@umn.edu), Shweta Srivastava, Xiaolue Lai, Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*

Time: 4:00 to 5:30pm Room: Oak Ballroom

SPECIAL SESSION 11A - VLSI-DAT

Moderators: Cheng-Wen Wu - *National Tsing-Hua Univ., Hsinchu, Taiwan*
Tim Cheng - *Univ. of California, Santa Barbara, CA*

Speakers: Yuan-Chuan Steven Chen - *Intel Corp., Hillsboro, OR*
Alex Chow - *Sun Microsystems, Inc., San Jose, CA*
Koushik K. Das - *IBM Corp., T.J. Watson Research Center, Yorktown Hts., NY*
Akria Ohchi - *Waseda Univ., Tokyo, Japan*

This session features four interesting papers from the 2008 IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT; http://vlsidat.itri.org.tw). The topics include novel techniques for nodal observability and controllability improvement, capacitance exploration for high-performance computer systems, nanometer design for ultra-low leakage MTCMOS circuits, and high-level syntheses with floorplanning for distributed/shared-register architectures.

11A.1 IS4 INCREASING THE NODAL OBSERVABILITY AND CONTROLLABILITY BY USING DESIGN FOR DEBUG CIRCUITS AND ADVANCED OPTICAL PROBING TECHNIQUES
Yuan-Chuan Steven Chen, Dan Bockelman - *Intel Corp., Hillsboro, OR*

11A.2 EXPLOITING CAPACITANCE IN HIGH-PERFORMANCE COMPUTER SYSTEMS
Alex Chow, David Hopkins, Robert Drost, Ron Ho - *Sun Microsystems, Inc., San Jose, CA*

11A.3 ULTRA-LOW LEAKAGE MTCMOS CIRCUITS WITH REGULAR-VT LONG CHANNEL STACKED FOOTERS FOR DEEP SUB-100NM TECHNOLOGIES
Koushik K. Das, Ching-Te Chuang - *IBM Corp., T.J. Watson Research Center, Yorktown Hts., NY*

11A.4 HIGH-LEVEL SYNTHESIS ALGORITHMS WITH FLOORPLANNING FOR DISTRIBUTED/SHARED-REGISTER ARCHITECTURES
Akria Ohchi, Nozomu Togawa, Masao Yanagisawa, Tatsuo Ohtsuki - *Waseda Univ., Tokyo, Japan*

4:00 - 5:30pm • Siskiyou Ballroom

EDA Bloggers' "Birds of a Feather" Meeting sponsored by CEDA

IEEE Council on Electronic Design Automation

Organizer: Juan-Antonio Carballo - *IBM Venture Capital Group, San Mateo, CA*

Blogging has become one of the fastest growing forms of publishing on the planet, making it difficult to neglect even by small industries like EDA. The purpose of this meeting is to promote blogging in EDA/ASIC Design Industry, provide tools for bloggers to aid each other, and educate readers and other interested parties in the EDA industry on this topic.

During this session, we will debate ways in which blogging can help EDA companies and designers -- potentially filling the void left by other media -- hear about the experiences and role analysis of bloggers, and discuss actions that should be pursued to specifically foster this space in our industry.

IEEE DATC Annual Meeting

DATC

Wednesday, November 12
6:00 - 7:30pm
Donner Ballroom

Join us for the Annual Meeting of the IEEE Technical Committee on Design Automation (DATC), IEEE's committee focused on EDA.

We will start with a brief introduction to the Committee's activities by our Chair Juan-Antonio Carballo from IBM Corporation, followed by brief descriptions of the Committee's activities by the Chairs of its respective sections. We will end with a talk and discussion on the future of EDA start-up investment and its impact on EDA technical leaders around the world.

You will be able to meet in person the leaders of this IEEE committee and discuss the future of EDA and how you would like to shape it.

AGENDA

Introduction – Juan-Antonio Carballo
Committee activities – DATC section chairs

Talk and panel discussion – "Design Globalization: impact on start-up investments and technical leaders"

Moderated by Juan-Antonio Carballo, IBM Venture Capital Group

Open to all!

Technology Fair

Participating companies are located in the Gateway Foyer
Monday & Tuesday, November 10 - 11, 10:00am - 4:00pm

Library Technologies, Inc.

19959 Lanark Ln.
Saratoga, CA 95070
408-741-1214
www.libtech.com

Exhibiting ChipTimer, Timing Closure Tool, 20-200% speed-up, 10% area reduction using special techniques and custom CellOpt generated libraries; SolutionWare, Cell, IO and Memory Characterization-Modeling; CellOpt, timing and power Optimizer for cells, adders and multipliers; YieldOpt, one step wc/bc corner model generator under process variation; PowerTeam: dynamic gate level power simulation.

Micro Magic, Inc.

1025 Heatherstone Way
Sunnyvale, CA 94087
408-414-7647
www.micromagic.com

Micro Magic provides chip design services, specializing in high-speed memories and high-speed datapath designs. Micro Magic provides professional EDA tools for high performance layout and datapath designs.

Technology Fair

Participating companies are located in the Gateway Foyer
Monday & Tuesday, November 10 - 11, 10:00am - 4:00pm

Springer

233 Spring St.
New York, NY 10013
212-460-1600
www.springer.com

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3333 Bowers Ave., Ste. 130
Santa Clara, CA 95054
408-748-1105
www.stonepillar.com

Stone Pillar Technologies is the leading provider of software tools supporting the development and characterization of semiconductor technologies. These include:

* DesignRuleBuilder for automating the calculation, documentation, and runset generation of design rules including the effects of process variabilities and considerations such as breakdown voltage or registration
* TestChipBuilder for automating test chip creation including the ability to rapidly modify parametric test chips in response to design rule or geometric changes
* TestPlanManager for automating parametric test creation
* DataAnalyzer and ReportGenerator for interactive or automated data analysis

Stone Pillar Suite integrates these tools to provide improved efficiency, maximum IP re-usability and to reduce errors in technology development.

Participating companies are located in the Gateway Foyer
Monday & Tuesday, November 10 - 11, 10:00am - 4:00pm

Technology Fair

UCSC Extension

10420 Bubb Rd.
Cupertino, CA 95014
408-861-3700
www.ucsc-extension.edu

UCSC Extension offers courses for Silicon Valley professionals in the fields of Integrated Circuits, ASIC, SoC, and EDA. A VLSI lab onsite allows students to experience hands-on training using state-of-the-art EDA tools. The VLSI Engineering certificate program has courses on logic, verification, physical and circuit designs.

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Virage Logic is a leading provider of semiconductor intellectual property (IP) for the design of complex integrated circuits. The company's highly differentiated product portfolio of Physical and Application Specific IP includes embedded SRAMs, embedded NVMs, logic libraries, I/Os and DDR memory controller subsystems. As the industry's trusted semiconductor IP partner, foundries, IDMs and fabless customers rely on Virage Logic to achieve higher performance, lower power, higher density and optimal yield, as well as shorten time-to-market and time-to-volume. For more information, visit www.viragelogic.com.

Thursday, November 13, 2008

Compact Variability Modeling (CVM) - Colocated Workshop

Thursday, November 13, 8:25am - 5:10pm Fir Ballroom

Workshop Organizers: Frank Liu - *IBM Austin Research Lab, Austin, TX*
Yu (Kevin) Cao - *Arizona State Univ., Tempe, AZ*

It is widely recognized that process variation is emerging as a fundamental challenge to IC design with scaled CMOS technology; and that it will have profound impact on nearly all aspects of circuit performance. While some of the negative effects of variability can be handled with improvements in the manufacturing process, the industry is starting to accept the fact that some of the effects are better mitigated during the design process. Handling variability in the design process will require accurate and appropriate models of variability and its dependence on designable parameters (i.e. layout), and its spatial and temporal distribution. Such models are quite different from the "corner" models deployed thus far to model manufacturing variability. As a consequence, the compact modeling of systematic, spatial, and random variations is essential to abstract the physical level variations into a format the designers (and –importantly- the tools that they use) can utilize. This IEEE/ACM workshop provides a forum to discuss current practice as well as near future research needs in the compact variation modeling.

Key Topics

Physics mechanisms and technology trends of device-level variations
First-principles simulation methods for predicting variability
Compact modeling of variations in devices and interconnect
Novel implementation and simulation techniques for dealing with variability
Variability bounding, characterization and extraction
Device and circuit level modeling techniques

OPENING REMARKS: *8:25 - 8:30am*

SESSION I: THE NEEDS OF VARIATIONAL COMPACT MODELS - *8:30 - 9:50am*

Managed Variability: Present and Future of Design-Process Integration from 45nm, and 32nm, to 22nm and Beyond
Luigi Capodieci - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Variability in Scaled CMOS Technology and Modeling Approaches for Circuit Simulation
Samar Saha - *SilTerra, Inc., San Jose, CA*

MORNING BREAK/DISCUSSION: *9:50 - 10:20am*

SESSION II: CURRENT STATISTICAL DEVICE MODEL - *10:20 - 11:40am*

Backward Propagation of Variance: You Measure it, BPV can Model it!
Colin McAndrew - *Freescale Semiconductor, Inc., Tempe, AZ*
Statistical Transistor SPICE Modeling in Advanced CMOS Technologies
John Krick - *Texas Instruments, Inc., Dallas, TX*

LUNCH BREAK: *11:40am - 1:00pm, Cedar Ballroom*

SESSION III: PRACTICE ON VARIATION MODELING - *1:00 - 3:00pm*

Compact Models of Some MOSFET Variations
Chenming Hu - *Univ. of California, Berkeley, CA*
A Multilevel Approach to Statistical Compact Modeling
Josef Watts - *IBM Corp., Bangalore, India*
Modeling of Proximity Effects in Nanometer MOSFET
Xi-Wei Lin - *Synopsys, Inc., Mountain View, CA*

AFTERNOON BREAK/DISCUSSION: *3:00-3:30pm*

SESSION IV: STATISTICAL CHARACTERIZATION AND SIMULATION MODEL - *3:30 - 4:50pm*

Model Extraction and Simulation Challenges for Process Variations in 45nm and Below
Bruce W. McGaughy - *ProPlus Design Solutions, San Jose, CA*
Display and Analysis of Variability Simulation Results
Kishore Singhal - *Synopsys, Inc., Mountain View, CA*

CLOSING REMARKS: *4:50 - 5:10pm*

Sponsored by:

Workshop on Test Structure Design for Variability Characterization (TSD) - Colocated Workshop

8:30am - 6:00pm • Pine Ballroom

Organizers: Hidetoshi Onodera - *Kyoto Univ., Kyoto, Japan*
Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*

PROGRAM OPENING: *8:30 - 9:15am* sponsored by VERIGY acm sigda

KEYNOTE ADDRESS:

Test Structures for Variability Characterization and Management
Mark B. Ketchen - *IBM T J Watson Research Center, Yorktown Hts., NY*

SESSION 1: TEST STRUCTURE DESIGN FOR VARIABILITY MODELING - *9:15 - 10:15am*

1.1 Characterization of CMOS Variability Utilizing 1M-DMA and Takeuchi Plot, 9:15am
Toshiro Hiramoto - *Univ. of Tokyo, MIRAI-Selete, Tokyo, Japan*
1.2 Variability Characterization in Logic and SRAM, 9:45am
Borivoje Nikolic - *Univ. of California, Berkeley, CA*

COFFEE BREAK: *10:15 - 10:30am*

SESSION 2: TEST STRUCTURES FOR VARIABILITY AND RELIABILITY MODELING - *10:30am - 12:00pm*

2.1 A Test Structure for Systematic Variation Measurement in Whole Shot at 45nm Process Node, 10:30am
Jingo Nakanishi, Hiromi Notani, Yasunobu Nakase, Hirofumi Shinohara - *Renesas Technology Corp., Itami, Japan*
2.2 A Ring-Oscillator Array Circuit for Measurement and Modeling of Gate Delay Variability, 10:45am
Haruhiko Terada, Akira Tsuchiy, Kazutoshi Kobayashi, Hidetoshi Onodera - *Kyoto Univ., Kyoto, Japan*
2.3 Silicon Odometers: On-chip Test Structures for Monitoring Reliability Mechanisms and Sources of Variation, 11:00am
John Keane, Tae-Hyoung Kim, Chris H. Kim - *Univ. of Minnesota, Minneapolis, MN*
2.4 Test Structures for SRAM Cell and Device Variability and the Statistics of NBTI Degradation, 11:15am
Thomas Fischer, Coris Schmitt-Landsiedel - *Technical Univ. Munich, Munich Germany*
Ettore Amirante, Karl Hofmann, Martin Ostermayr, Peter Huber - *Infineon Technologies*

POSTER DISCUSSION: *11:30am - 12:00pm*

LUNCH BREAK: *12:00 - 1:00pm, Cedar Ballroom*

SESSION 3: TEST STRUCTURES FOR PROCESS AND PERFORMANCE MODELING - *1:00 - 3:30pm*

3.1 Measuring and Modeling IC Variability at the Process, Device, and Circuit Levels (Invited), 1:00pm
Nigel Drego - *Massachusetts Institute of Tech., Cambridge, MA*
3.2 Ring Oscillators for Single Process-parameter Monitoring (Invited), 1:30pm
Jian Wang - *Carnegie Mellon Univ., Pittsburgh, PA*
3.3 Methodology of Separating Process Variation from Measurement Result, 2:00pm
Michio Komoda, Issei Kashima - *Renesas Technology Corp. Itami, Japan*
3.4 Parameter-specific Ring Oscillators for Quantifying Sources of Variability, 2:15pm
Lynn T.-N. Wang, L.-T. Pang, A.R. Neureuther, Borivoje Nikolic - *Univ. of California, Berkeley, CA*
3.5 Performace Variability of On-chip Noise Monitor Circuits, 2:30pm
Yoji Bando, Takushi Hashida, Makoto Nagata - *Kobe Univ., Kobe, Japan*
3.6 Vth Variation Modeling and Its Validation with Ring Oscillation Frequencies for Body-based Circuits and Subthreshold Circuits, 2:45pm
Hiroshi Fuketa, Masanori Hashimoto, Yukio Mitsuyama, Takao Onoye - *Osaka Univ., Suita, Japan*

POSTER DISCUSSION: *3:00 - 3:30pm*

COFFEE BREAK: *3:30 - 3:45pm*

SESSION 4: CHALLENGES FOR TECHNOLOGY CHARACTERIZATION - *3:45 - 6:00pm*

4.1 Statistical Technology Characterization (Invited), 3:45pm
Kanak Agarwal - *IBM Corp., Austin, TX*
4.2 Efficient Usage of Test Structures (Invited), 4:15pm
Christopher Hess - *PDF Solutions, San Jose, CA*
4.3 Utilizing a New, Highly Parallel, Per-pin Precision pA, uA, and Digital Measurement System for Testing Wafer Test Structures, 4:45pm
Robert J. Smith - *Verigy, Inc., Totowa, NJ*
4.4 An Efficient Extraction of Random and Systematic Gate-length Variation through Poly-si Resistor Measurement, 5:00pm
Noriaki Nakayama, Takashi Sato, Hiroyuki Ueyama, Kazuya Masu - *Tokyo Institute of Tech., Yokohama, Japan*
4.5 MOSFET-array for Extracting Parameters Expressing SPICE-parameter Variation, 5:15pm
Kazuo Terada, Koichiro Ueda, Katuhiro Tsuji - *Hiroshima City Univ., Hiroshima, Japan*
Takaaki Tsunomura, Akio Nishida - *MIRAI-Selete, Tokyo, Japan*

POSTER DISCUSSION: *5:30 - 6:00pm*

Thursday, November 13, 2008

Electrical-level Modeling for Timing, Noise, and Power Analysis (ECM) - Colocated Workshop

8:30am - 5:30pm • Oak Ballroom

Organizers: **Massoud Pedram** – *Univ. Southern California, Los Angeles, CA*
Noel Menezes – *Intel Corp., Hillsboro, OR*
Peter Feldmann – *IBM Corp., Yorktown Hts., NY*
Igor Keller – *Cadence Design Systems, Inc., San Jose, CA*

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Electrical-level modeling of library cells, for delay, noise, and power calculation is an important developing area across the EDA community. It is an essential step in the evolution of cell modeling as it addresses the challenging demands for higher accuracy, handling of variability, and improved product performance for large-scale analysis applications at current and future process technology nodes. In particular, controlled-current source models have emerged as the industry wide standardized solution for delay computation under cross-talk and process variations. This workshop will cover such topics as (i) motivation for moving to current-source modeling technologies in delay calculation, (ii) comparative analysis of existing current-source models including their abilities to address complexities of the 45nm era and beyond, (iii) the impact of new modeling technologies on delay calculation in variation-aware static timing and noise analysis flows, (iv) challenges and trends in library characterization, and (v) algorithmic advances required in the driving analysis applications for effective model usage. This workshop is also targeted at methodology changes related to usage of these models and practical deployment issues in actual design flows.

OPENING REMARKS: *8:30 - 8:40am*

KEYNOTE: MODELING IMPLICATIONS OF IP BASED DESIGN: *8:40 - 9:20am*
Leon Stock - *IBM Corp., Hopewell Junction, NY*

MORNING SESSION: ADVANCES IN CELL-LEVEL MODELING TECHNOLOGIES - *9:20 - 12:10pm*

Abstract Electrical Modeling for High Bandwidth IO Link
Chirayu Amin, Chandramouli Kashyap - *Intel Corp., Hillsboro, OR*
Prateek Bhansali - *Univ. of Minnesota, Minneapolis, MN*

Parametric Cell Delay Models and their Applications in 65/45nm Digital Designs
Jiayong Le - *ExtremeDA, Palto Alto, CA*

MORNING BREAK/DISCUSSION: *10:20 - 10:40am*

Trajectory Based Models And Their Applications To Standard Cell Modeling
Saurabh Tiwary - *Cadence Design Systems, Berkeley, CA*

Transistor Level Gate Modeling for Accurate and Fast Timing, Noise, and Power Analysis
Shiva Raja, Ferenc Faradi, Murat Becer, Joao Geada - *CLK Design Automation, Inc., Littleton, MA*

Cell-level Robust Electrical Analysis Model for Timing and SI Analysis
Igor Keller, King Ho Tam, Vinod Kariat - *Cadence Design Systems, Inc., San Jose, CA*

LUNCH BREAK: *12:10 - 2:00pm Cedar Ballroom*

AFTERNOON SESSION: PRACTICES ON CELL-LEVEL MODELING - *2:00 - 4:45pm*

Practical Experience of Deployment of CCSM-Based Delay Calculator
Alexander Korshak - *Magma Design Automation, Inc., San Jose, CA*

Incorporating Controlled-Current Models into Modern Design Flows
John Croix - *Nascentric, Inc., Austin, TX*

An Efficient Current-Based Logic Cell Model for Crosstalk Delay Analysis
Debasish Das, Hai Zhou - *Northwestern Univ., Evanston, IL*
William Scott, Shahin Nazarian - *Magma Design Automation, San Jose, CA*

AFTERNOON BREAK/DISCUSSION: *3:30 - 3:45*

Library Characterization for the Next Decade
Ken Tseng, Paul Osepa - *Altos Design Automation, Santa Clara, CA*

Efficient Compression and Handling of Current Source Model Library Waveforms
Safar Hatemi - *Univ. of Southern California and IBM Corp., Los Angeles, CA*
Peter Feldmann - *IBM Corp., Yorktown Hts., NY*
Soroush Abbaspour - *IBM Corp., Hopewell Junction, NY*
Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

PANEL & DISCUSSION: *4:50 - 6:00pm*

Challenges and Promises in Cell-level Modeling in 65nm and Beyond
Moderator: Vladimir Zolotov - *IBM Corp., Yorktown Hts., NY (Panelists: TBD)*

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