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Monday Sessions

1D.1 SCHEDULING WITH SOFT CONSTRAINTS
Jason Cong, Bin Liu - *Univ. of California, Los Angeles*
Zhiru Zhang - *AutoESL Design Technologies, Inc.*

2B.1 IN-PLACE RECONFIGURATION FOR FPGA FAULT TOLERANCE
Zhe Feng, Yu Hu, Lei He, Rupak Majumdar - *Univ. of California, Los Angeles*

2C.1 SAT-BASED PROTEIN DESIGN
Noah Ollikainen - *Univ. of California, San Francisco*
Ellen Sentovich - *Consultant*
Carlos Coelho - *Cadence Design Systems, Inc.*
Tanja Kortemme - *Univ. of California, San Francisco*
Andreas Kuehlmann - *Cadence Design Systems, Inc.*

3A.1 PRE-BOND TESTABLE LOW-POWER CLOCK TREE DESIGN FOR 3-D STACKED ICS
Xin Zhao, Dean L. Lewis, Hsien-Hsin S. Lee, Sung Kyu Lim - *Georgia Institute of Technology*

3C.1 EXACT ROUTE MATCHING ALGORITHMS FOR ANALOG AND MIXED SIGNAL INTEGRATED CIRCUITS
Mustafa Ozdal, Renato Hentschke - *Intel Corp.*

3D.1 THERMAL MODELING FOR 3-D-ICS WITH INTEGRATED MICROCHANNEL COOLING
Hitoshi Mizunuma, Chia-Lin Yang, Yi-Chang Lu - *National Taiwan Univ.*

Tuesday Sessions

4B.1 THE EPSILON-APPROXIMATION TO DISCRETE VT ASSIGNMENT FOR LEAKAGE POWER MINIMIZATION
Yujia Feng, Shiyan Hu - *Michigan Technological Univ.*

4C.1 TAPE: THERMAL-AWARE AGENT-BASED POWER ECONOMY FOR MULTI/MANY-CORE ARCHITECTURES
Thomas Ebi, Mohammad Abdullah Al Faruque, Jörg Henkel - *Univ. Karlsruhe*

5A.1 A HIERARCHY OF SUBGRAPHS UNDERLYING A TIMING GRAPH AND ITS USE IN CAPTURING TOPOLOGICAL CORRELATION IN SSTA
Jaeyong Chung, Jacob A. Abraham - *Univ. of Texas, Austin*

5C.1 THE SYNTHESIS OF COMBINATIONAL LOGIC TO GENERATE PROBABILITIES
Weikang Qian, Marc D. Riedel, Kia Bazargan, David J. Lilja - *Univ. of Minnesota*

7A.1 AN ELEGANT HARDWARE-CORROBORATED STATISTICAL REPAIR AND TEST METHODOLOGY FOR CONQUERING AGING EFFECTS
Rouwaida Kanj, Rajiv Joshi, Chad Adams, James Warnock, Sani Nassif - *IBM Corp.*

7C.1 FROM 2-D TO 3-D NOCS: A CASE STUDY ON WORST-CASE COMMUNICATION PERFORMANCE
Yue Qian - *National Univ. of Defense Technology*
Zhonghai Lu - *Royal Institute of Technology*
Wenhua Dou - *National Univ. of Defense Technology*

Wednesday Sessions

8C.1 VOLTAGE-DROP AWARE ANALYTICAL PLACEMENT BY GLOBAL POWER SPREADING FOR MIXED-SIZE CIRCUIT DESIGNS
Yi-Lin Chuang, Po-Wei Lee, Yao-Wen Chang - *National Taiwan Univ.*

9B.2 A HIERARCHICAL FLOATING RANDOM WALK ALGORITHM FOR FABRIC-AWARE 3-D CAPACITANCE EXTRACTION
Tarek A. El-Moselhy - *Massachusetts Institute of Technology*
Ibrahim M. Elfadel - *IBM Corp.*
Luca Daniel - *Massachusetts Institute of Technology*